

## Article

# Novel Three-Phase Nine-Level Inverter and Its Control Strategies

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**Abstract:** In this paper, the authors propose a new three-phase, nine-level inverter with self-balancing of capacitor voltages. The proposed inverter is the result of a serial connection of the SPUC topology and the NPC converter. A single DC source is used, and each phase is made up of nine power switches and three capacitors. Two control techniques are proposed to maintain the voltage of the capacitors to the desired values, the first of which is a PWM technique that ensures the self-balancing of capacitor voltages in open loops without using any filters or PI regulators, and the second is based on the hysteresis control which offers a nearly sinusoidal waveform of the load current without using any voltage sensors. The authors make use of the Matlab Simulink environment to perform the simulation of the proposed concept. The dynamics of the latter was verified against load change.

**Keywords:** PUC; NPC; PWM technique; hysteresis control; THD; multilevel inverter

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## 1. Introduction

In recent years, multilevel inverters have attracted considerable attention because of their advantages, including low electromagnetic interference (EMI), reduced voltage stress (dv/dt), low total harmonics distortion (THD), and high power conversion.

Many three-phase inverters were proposed over the years. Most of them are based on the three basic topologies, which are the neutral point clamped (NPC) [1], the cascaded H-bridge (CHB) [2], and the flying capacitor (FC) [3]. However, their power quality remains fairly low. The authors propose a solution by optimizing the number of active and passive devices. The proposed converter overcomes the serious drawback of the NPC by permitting a natural self-balancing of capacitors voltages when the number of the desired voltage levels is greater than three.

In this paper, we propose an advanced three-phase, nine-level inverter which is derived from the series connection of the SPUC [4] converter that allows a load voltage with high level number while using an optimized count of active and passive components and NPC topology that has the advantage of joining capacitors together. The proposed inverter uses the benefit of redundant states to perform the self-balancing of capacitor voltages in open loops without using any filters or PI regulators [5–7].

Firstly, a PWM technique is applied to the proposed inverter, as a result the system offering nine levels in output voltage without using any closed loop regulation [8–19]; because the latter is not suitable for some industrial applications, this allows a low cost of inverter and installation. Secondly, a hysteresis control is used to provide a near sinusoidal without the use of a voltage sensor or PI controllers.

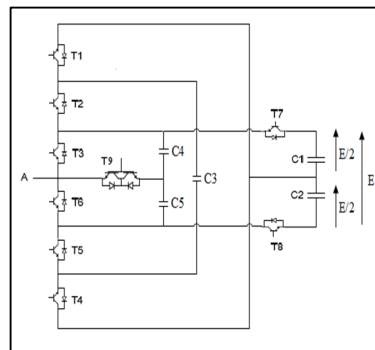
## 2. Methods

Firstly, the proposed inverter topology, which is based on PUC and NPC converters, is presented in single- and three-phase versions, and then capacitor balancing techniques are detailed, which are PWM techniques and hysteresis controls.

### 2.1. Presentation the Proposed Three-Phase Inverter Topology and Switching States

The proposed inverter is derived from a series connection of SPUC and NPC converters, and this connection was used between PUC and NPC converters [20]. As a result, it can provide a maximum of levels using a single DC source because a closed loop is used to keep voltage values of the desired capacitors.

The proposed topology has a new advantage, which is the ability to maintain capacitor voltage at desired values in open loops without any PI regulators and with two different methods of control, which are PWM techniques and hysteresis control. The proposed nine-level inverter is constituted from nine power switches and three capacitors per phase. Those capacitors, which are C3, C4, and C5 should be balanced respectively to  $E/2$ ,  $E/8$ , and  $E/8$ . However, C1 and C2 should be maintained in the half of the DC source. Figure 1 represents the single phase of the nine-level inverter proposed.

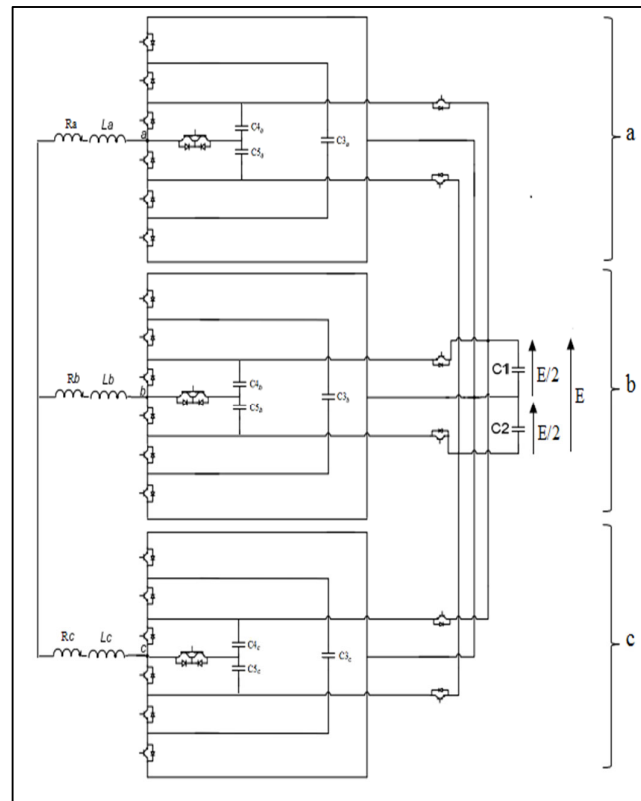


**Figure 1.** Proposed inverter single phase.

In order to generate a nine level output voltage, we assume that  $V_{c1} = V_{c2} = V_{c3i} = E/2$  and  $V_{c4i} = V_{c5i} = E/8$  ( $i = a, b, c$ ). Table 1 represents the nine required levels with redundant states (1', 3', 5', 7', 9'). Figure 2 represents the three-phase, nine-level inverter proposed.

**Table 1.** Switching sequence for the three-phase 9-level inverter proposed.

State	Interconnection	Voltage(V)	T1i	T2i	T3i	T4i	T5i	T6i	T7i	T8i	T9i
9	$V_{c2}$	400	0	0	0	0	0	1	0	1	0
9'	$V_{c3i}$	400	1	0	0	0	1	1	0	0	0
8	$V_{c3i} - V_{c5i}$	300	1	0	0	0	1	0	0	0	1
7	$V_{c3i} - (V_{c4i} + V_{c5i})$	200	1	0	1	0	1	0	0	0	0
7'	$V_{c4i} + V_{c5i}$	200	1	1	0	0	0	1	0	0	0
6	$V_{c4i}$	100	1	1	0	0	0	0	0	0	1
5	0	0	1	1	1	0	0	0	0	0	0
5'	0	0	0	0	0	1	1	1	0	0	0
4	$-V_{c5i}$	-100	0	0	0	1	1	0	0	0	1
3	$-V_{c4i} - V_{c5i}$	-200	0	0	1	1	1	0	0	0	0
3'	$(V_{c4i} + V_{c5i}) - V_{c3i}$	-200	0	1	0	1	0	1	0	0	0
2	$V_{c4i} - V_{c3i}$	-300	0	1	0	1	0	0	0	0	1
1'	$-V_{c3i}$	-400	0	1	1	1	0	0	0	0	0
1	$-V_{c1}$	-400	0	0	1	0	0	0	1	0	0



**Figure 2.** Proposed three-phase SPUC-NPC inverter.

The nine levels were generated as follows.

In state 9, in which the load voltage is equal to  $V_{c2}$ , switches S6 and S8 are “ON”. Capacitor C2 is discharging since it is connected only to the load.

In state 8, in which the load voltage is equal to  $V_{c3i} - V_{c5i}$ , switches S1, S5, and S9 are “ON”. Capacitor C2 has a serial connection with capacitor C3, thus Capacitor 5 is charging. However, Capacitor 3 is discharging.

In state 7', in which the load voltage is equal to  $V_{c4i} + V_{c5i}$ , switches S1, S2, and S6 are “ON”. Capacitors are connected directly to the load, so they are discharging.

In state 6, in which the load voltage is equal to  $V_{c4i}$ , switches S1, S2, and S9 are “ON”. Capacitor C4 is discharging since it is connected only to the load.

In state 5, in which the load voltage is equal to zero, switches S1, S2, and S3 are “ON”. There is no effect to capacitors since none is connected to the DC source.

In state 4, in which the load voltage is equal to  $-V_{c5i}$ , switches S4, S5, and S9 are “ON”. Capacitor C5 is discharging since it is connected only to the load.

In state 3, in which the load voltage is equal to  $-V_{c4i} - V_{c5i}$ , switches S3, S4, and S5 are “ON”. Capacitors are connected directly to the load, thus, they are discharging.

In state 2, in which the load voltage is equal to  $V_{c4i} - V_{c3i}$ , switches S2, S4, and S9 are “ON”. Capacitor C4 has a serial connection with capacitor C3, thus, Capacitor 4 is charging. However, Capacitor 3 is discharging.

In state 1, in which the load voltage is equal to  $-V_{c1}$ , switches S3 and S7 are “ON”. Capacitor C1 is discharging since it is connected only to the load.

The number of voltage levels should be decreased in order to create several redundant states. The ability of choosing among them is one of the major advantages. Indeed, a state can be chosen according to the desired charging or discharging capacitor behavior while keeping the same output voltage value. As shown in Table 1, states (3 and 3') allow the same output voltage, which is equal to  $-200$  V. One can proceed by the same manner to determine the other redundant states.

## 2.2. Proposed Nine-Level Inverter Using PWM Technique

In order to generate the gate pulses, one has to design a modulation technique. Consequently, in this paper, the authors propose the following procedure in which a sign function of the reference voltage is used to determine  $S_1$ .

$$\text{Sign}(v_r) = \begin{cases} 1, v_r \geq 0 \\ 0, v_r < 0 \end{cases} \quad (1)$$

$$S_1 = \text{Sign}(v_r) \quad (2)$$

Eight equal amplitude triangular carriers which are indicated by the letter  $C_{ri}$  ( $i = 1 \dots 8$ ) are compared with the sinusoidal reference, the carriers arrangements for PWM strategy are shown in Figure 3, and each comparison generates a new signal indicated by the letter  $Z_i$  ( $i = 1 \dots 8$ ).

$$Z_1 = \begin{cases} 1, C_{r1} \geq v_r \\ 0, C_{r1} < v_r \end{cases} \quad (3)$$

$$Z_2 = \begin{cases} 1, C_{r2} \geq v_r \\ 0, C_{r2} < v_r \end{cases} \quad (4)$$

$$Z_3 = \begin{cases} 1, C_{r3} \geq v_r \\ 0, C_{r3} < v_r \end{cases} \quad (5)$$

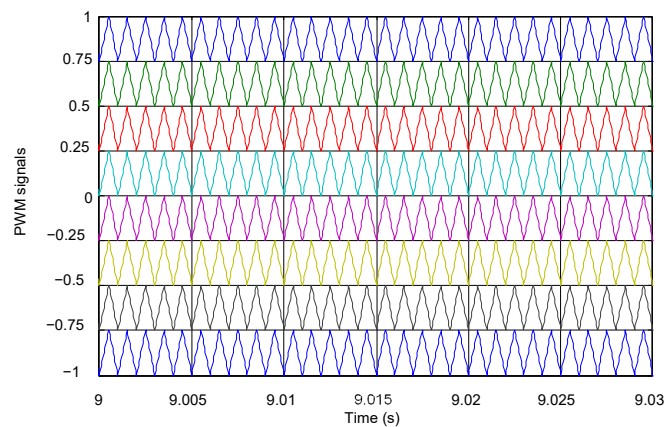
$$Z_4 = \begin{cases} 1, C_{r4} \geq v_r \\ 0, C_{r4} < v_r \end{cases} \quad (6)$$

$$Z_5 = \begin{cases} 1, C_{r5} \geq v_r \\ 0, C_{r5} < v_r \end{cases} \quad (7)$$

$$Z_6 = \begin{cases} 1, C_{r6} \geq v_r \\ 0, C_{r6} < v_r \end{cases} \quad (8)$$

$$Z_7 = \begin{cases} 1, C_{r7} \geq v_r \\ 0, C_{r7} < v_r \end{cases} \quad (9)$$

$$Z_8 = \begin{cases} 1, C_{r8} \geq v_r \\ 0, C_{r8} < v_r \end{cases} \quad (10)$$



**Figure 3.** Carrier arrangements for PWM strategy.

A staircase signal which the image of the voltage load can then be generated by summing these equations is as follows.

$$S = Z_1 + Z_2 + Z_3 + Z_4 + Z_5 + Z_6 + Z_7 + Z_8 \quad (11)$$

The remaining gate pulses can then be expressed as follows.

$$S_2 = \overline{S_5} \quad (12)$$

$$S_3 = \overline{Z_6} + \overline{Z_8} \quad (13)$$

$$S_4 = 1 - \text{sign}(v_r) \quad (14)$$

$$S_5 = (Z_1 Z_2 \oplus Z_3 Z_4) + (Z_1 Z_2 \oplus Z_3 Z_4) \quad (15)$$

$$S_6 = Z_1 + Z_3 + (Z_4 \oplus Z_5) \quad (16)$$

$$S_7 = (Z_1 \oplus Z_2) + (Z_3 \oplus Z_4) + (Z_5 \oplus Z_6) + (Z_7 \oplus Z_8) \quad (17)$$

$$S_8 = Z_1 \quad (18)$$

$$S_9 = Z_8 \quad (19)$$

Finally, the proposed control technique is depicted in Figure 4. It permits the self-balancing of capacitor voltages in open loop operation.

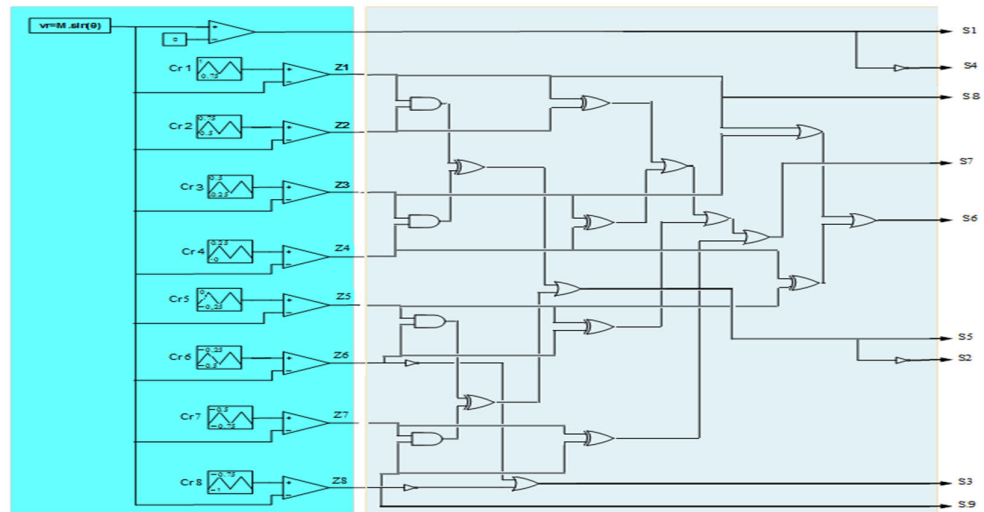


Figure 4. The proposed control technique.

### 2.3. Proposed Nine-Level Inverter Using Hysteresis Control

The proposed control technique is based on the eight band hysteresis approach, when the current error  $\Delta i$  is negative. The positive voltages (sector A in Figure 5) are applied. Inversely, the negative voltages (sector B) are applied when the current error is positive.  $\Delta i$  is the difference between actual load current and its reference.

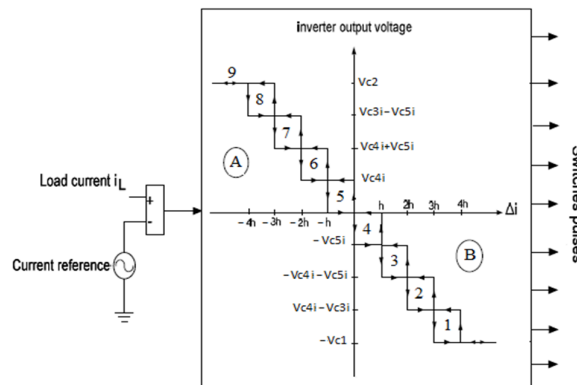


Figure 5. Proposed capacitor voltages balancing technique.

The nine states and their transition conditions are depicted in Figure 6. Switch pulses are presented in the following order T1i. T2i. T3i. T4i. T5i. T6i. T7i. T8i. T9i ( $i = a, b, c$ ).

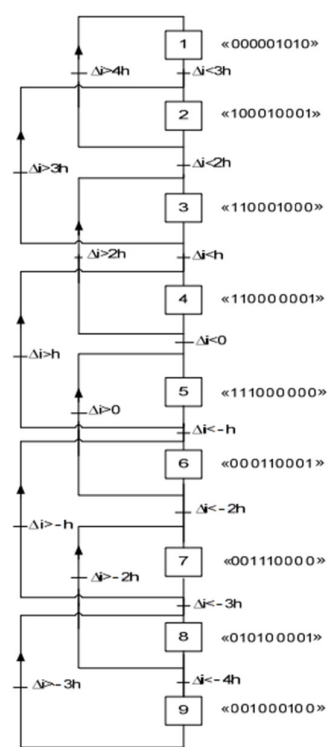


Figure 6. Switch gate pulse generation.

### 3. Results

Simulation of the proposed SPUC-NPC three-phase, nine-level inverter was carried out in the MATLAB/SIMULINK environment.

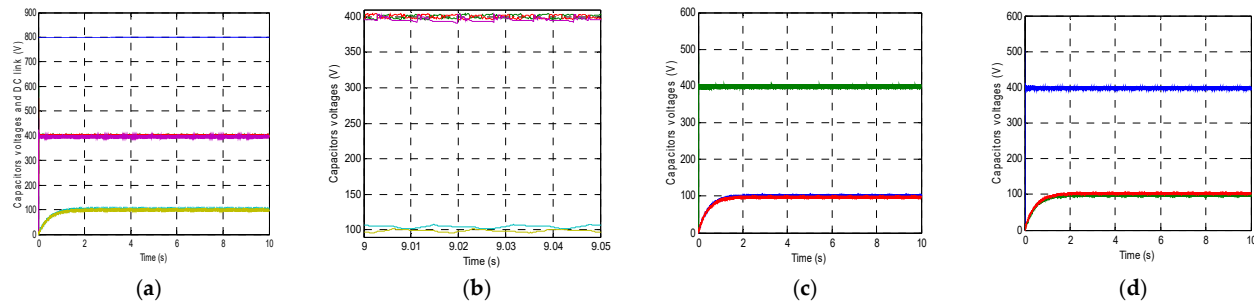
#### 3.1. Using PWM Technique

The parameters used for the simulation are presented in Table 2:

Table 2. Simulation parameters.

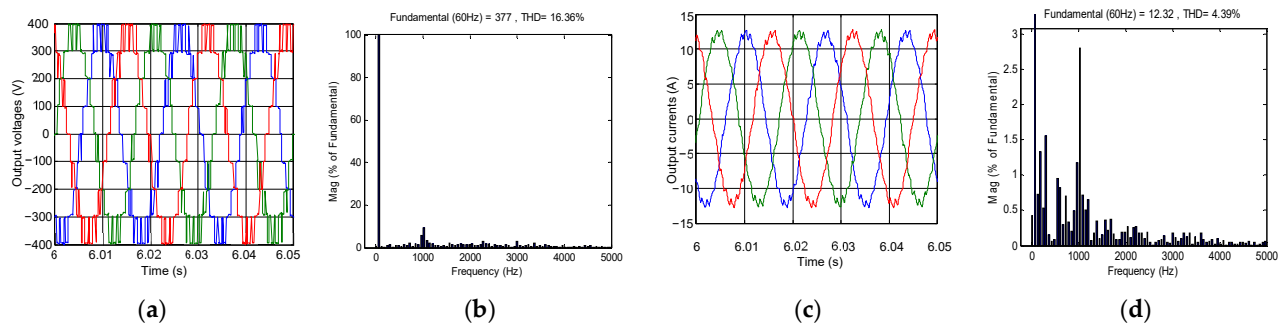
Parameter	Value
Switching frequency	1000 Hz
E (DC source voltage)	800 V
Load resistor	30 $\Omega$
Load inductance	15 mH
Auxiliary DC bus capacitor	4000 $\mu$ F
Amplitude modulation index	$m = 0.75$

As shown in Figure 7, capacitor voltages are respectively well balanced and remain in steady state around the half of the DC source voltage for Vc1 and Vc2. However capacitor voltages of the three phases (a, b, and c) which are Vc3i, Vc4i, and Vc5i ( $i = a, b, c$ ) are maintained in  $E/2$  for capacitor 3 and the eighth of the DC source for capacitors 4 and 5.



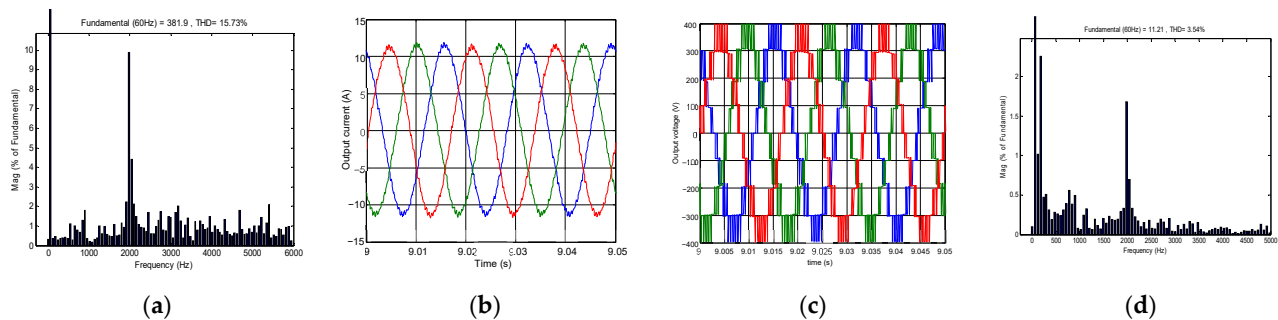
**Figure 7.** (a) Capacitor voltages of the phase b, Vc1, Vc2, and DC source; (b) zoom on (a) at  $t = 9$  s; (c) capacitor voltages of the phase a; and (d) capacitor voltages of the phase c.

Figure 8a shows the inverter output voltage waveform. The latter is constituted of nine voltage levels, which are {400 V; 300 V; 200 V; 100 V; 0; −100 V; −200 V; −300 V; −400 V}. However, the load current is nearly sinusoidal as is presented in Figure 8c. This waveform is obtained without using any active or reactive filter. Moreover, no sensor or closed loop is used, which permits a low inverter and installation cost.



**Figure 8.** (a) Load voltage output; (b) harmonics spectrum of inverter output voltage; (c) load current output; and (d) zoom on harmonics spectrum of load current.

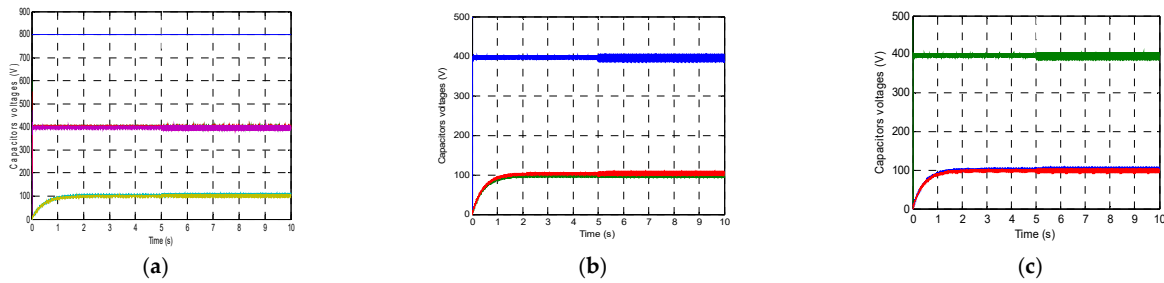
A very low THD is achieved. The THD level of the proposed three-phase, nine-level inverter is 16.36% for output voltages (Figure 8b) and 4.39% for output current waveform (Figure 8d). Although this value fulfills standards, it can be reduced by increasing the modulating signal frequency or amplitude modulation index, and to prove this, another simulation is done using 2000 Hz as the switching frequency, with the other parameters kept at the same values; Figure 9 shows simulation results.



**Figure 9.** (a) Harmonics spectrum of load voltage; (b) load current output; (c) load voltage; (d) zoom on harmonics spectrum of load current.

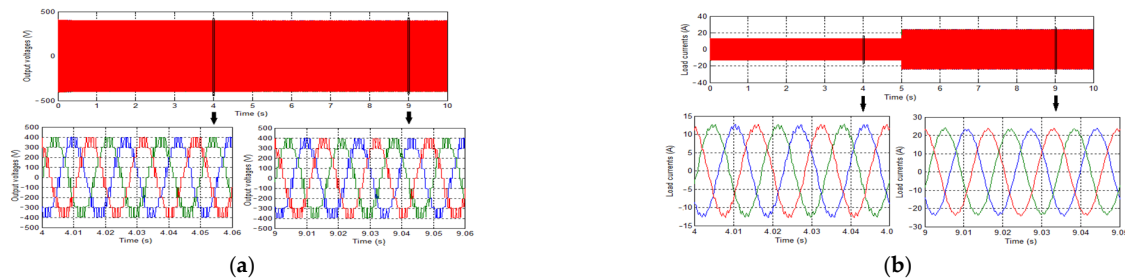
The proposed concept is verified against a load resistance change. Therefore, at  $t = 5$  s, load resistance changes from  $30\ \Omega$  to  $15\ \Omega$ . Other parameters keep the same values, which are 800 V for DC link and 15 mH for load inductance.

Simulation results show that capacitor voltages keep the same values, even after a severe load change. In fact,  $V_{c1}$  and  $V_{c2}$  are fixed in the half of the DC source. However, others capacitors remain well maintained around the half of the DC link for  $V_{c3i}$  and the eighth of the DC source for  $V_{c4i}$  and  $V_{c5i}$  ( $i = a, b, c$ ). Figure 10 shows the capacitor voltages against step load change.



**Figure 10.** (a) Capacitors voltages of the phase b; (b) capacitors voltages of the phase a and; (c) capacitors voltages of the phase c.

The load voltage behavior before and after load change is depicted in Figure 11a. The balancing technique operates very well even during load change. Figure 11b shows load current behavior before and after load change. The current remains nearly sinusoidal even during load change, which reflects the high dynamics of the proposed algorithm.



**Figure 11.** (a) Output voltages response against step load change; (b) output currents response against step load change.

### 3.2. Using Hysteresis Control

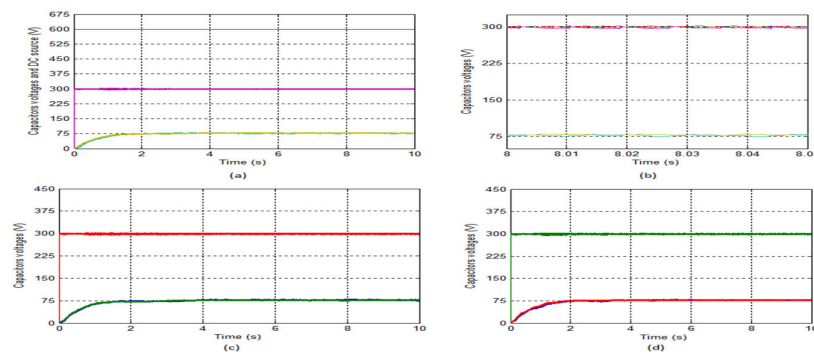
Simulation was performed using parameters depicted in Table 3.

**Table 3.** Simulation parameters.

Parameters	Value
Hysteresis bandwidth	0.25
E (DC source voltage)	600V
Load resistor	$30\ \Omega$
Load inductance	15 mH
Auxiliary DC bus capacitor	4000 $\mu$ F

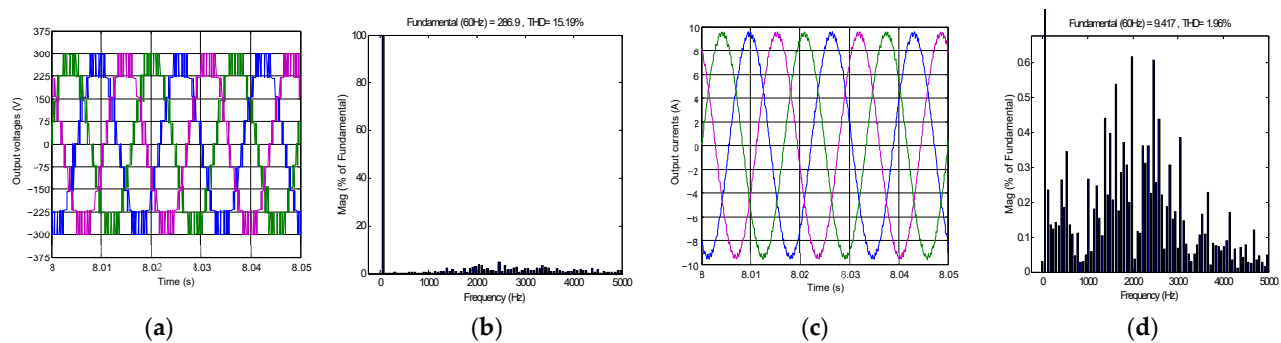
As shown in Figure 12, the capacitors are seen to have reached their desired voltage values, thus  $V_{c1}$  and  $V_{c2}$  are fixed around the half of the DC source. However,  $V_{c3i}$ ,  $V_{c4i}$ , and  $V_{c5i}$  ( $i = a, b, c$ ) are balanced, respectively, to  $E/2$ ,  $E/8$ , and  $E/8$ . The same results are obtained for the three phases. No voltage sensor or closed loop is needed.



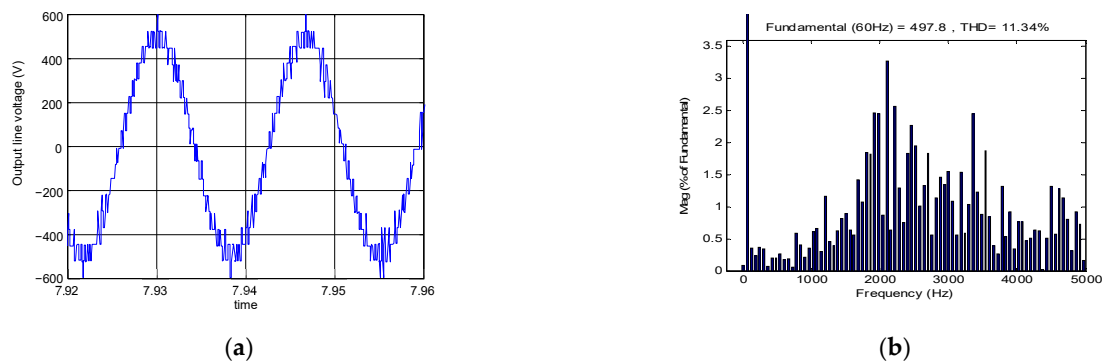


**Figure 12.** (a) Capacitors voltages of the phase b, Vc1, Vc2, and DC source; (b) zoom on (a) at  $t = 9$  s; (c) capacitors voltages of the phase a; and (d) capacitors voltages of the phase c.

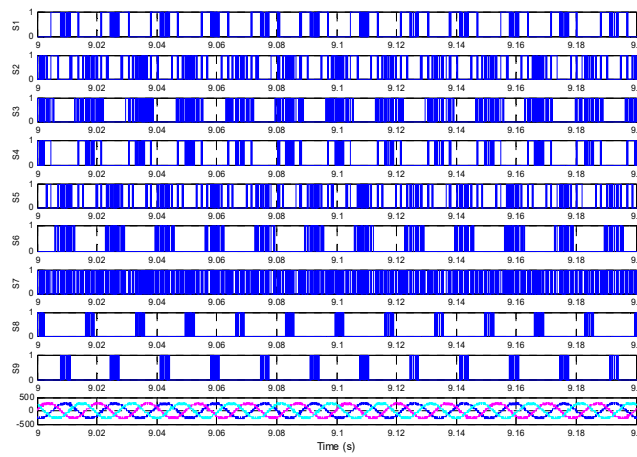
As shown in Figure 13a, the output voltage consists of nine voltage levels, and 15.19% is the THD level detected as being presented in Figure 13b. However, the load current is nearly sinusoidal as is presented in Figure 13c, with 1.96% as THD level (Figure 13d), the output line-to-line voltage and its THD level are presented in Figure 14. These waveforms are obtained without using any active or reactive filter. Moreover, no voltage sensor or PI regulator is used which permits a low inverter and installation cost. The THD level can be reduced by reducing the hysteresis bandwidth. The nine switching patterns are presented in Figure 15.



**Figure 13.** (a) Load voltage output; (b) harmonics spectrum of inverter output voltage; (c) load current output; and (d) zoom on harmonics spectrum of load current.



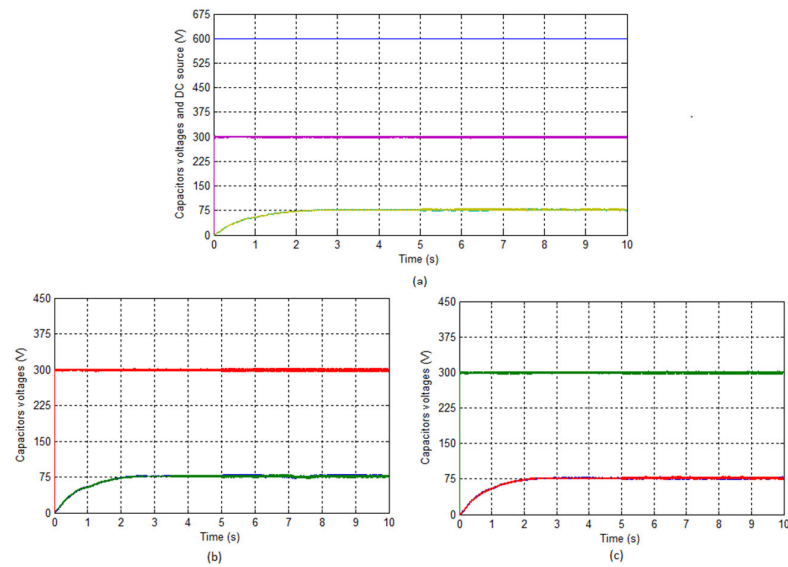
**Figure 14.** (a) Output line-to-line voltage; (b) harmonics spectrum of inverter output voltage line-to-line.



**Figure 15.** Switching patterns.

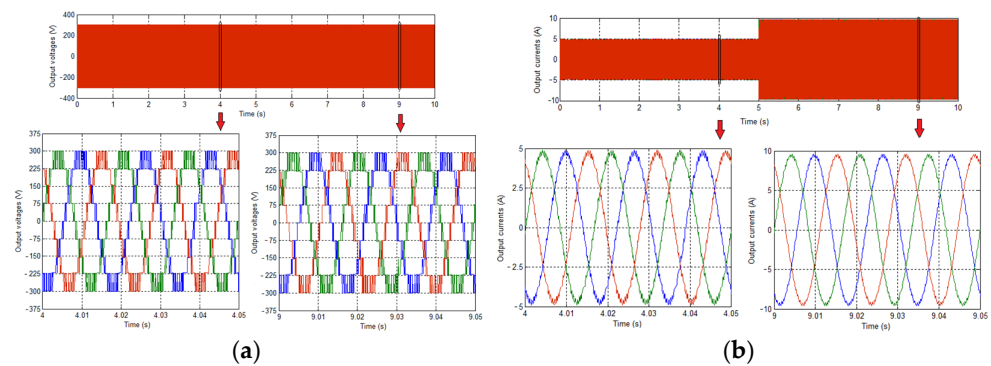
In order to verify the high dynamics of the proposed system, a load resistance change is applied at  $t = 5$  s. In fact, resistance is changed from  $60 \Omega$  to  $30 \Omega$ . Other parameters keep the same values.

Capacitor voltages are well maintained around the desired value, even after a severe load change. In fact  $V_{c1}$  and  $V_{c2}$  are fixed in the half of the DC source. However, other capacitors are maintained around the half of the DC link for  $V_{c3i}$  and the eighth of the DC source for  $V_{c4i}$  and  $V_{c5i}$  ( $i = a, b, c$ ). Figure 16 shows the capacitor voltages against step load change.



**Figure 16.** (a) Capacitor voltages of the phase b; (b) capacitor voltages of the phase a; and (c) capacitor voltages of the phase c.

As shown in Figure 17, before and after the change, the load voltage is constituted of nine levels with the same step, which is  $75 \text{ V}$ . By the same way, load current is nearly sinusoidal before and after the change, which reflects the high dynamics of the proposed system.



**Figure 17.** (a) Output voltages response against step load change; (b) output currents response against step load change.

#### 4. Comparative Study

Table 4 compares the THD level of output voltage with other topologies by varying the switching frequency and amplitude modulation index, and we observe that the proposed topology has a low THD level without the need of any filters; however, Table 5 presents a comparison of switching components, and the comparison includes basic topologies and the PUC inverter, as can be seen, the SPUC-NPC three-phase, nine-level inverter has a significant advantage other than the use of a limited number of power components, which is the implementation of one DC source, and other capacitor voltages are balanced without the use of any closed loop regulation and with two control methods, which are PWM techniques and hysteresis control.

**Table 4.** Comparison of switching components.

Inverters	Switches	Clamping Diodes	Capacitors	DC Source
Diode clamped	48	168	NA	8
Flying capacitor	48	NA	84	8
H-Bridge	48	NA	NA	12
PUC	24	NA	6	3
Proposed inverter	27	NA	11	1

**Table 5.** THD level voltage comparison.

Amplitude Modulation Index	Inverters	THD Level %		
		1000 Hz	2000 Hz	5000 Hz
m = 1.15	Proposed Inverter	14.05	13.32	13.27
	Proposed Inverter	14.27	13.51	13.4
	9-Level, Three-Phase Reversing Voltage [21]	N.C	N.C	16.30
m = 1	Three-Phase, 9-Level Inverter with Reduced Switching Devices [22]	14.35	N.C	N.C
	Three-Phase, 9-level Cascaded MLI with less switches [23]	N.C	N.C	13.72
	Proposed Inverter	15.12	14.02	13.8
m = 0.9	3-Phase, Nine-Level Diode Clamped Inverter [24]	14.32	14.09	N.C
	Asymmetric Three-Phase Cascading Trinary-DC Source [25]	N.C	16.06	N.C

m = 0.85	Three-Phase, 9-Level Inverter with Reduced Switching Devices	15.27	N.C	N.C
	Proposed Inverter	15.41	14.60	14.22
	Asymmetric Three-Phase Cascading Trinary-DC Source	N.C	17.39	N.C
m = 0.75	Proposed Inverter	16.36	15.73	15.17

N.C = Not calculated.

## 5. Conclusions

A novel three-phase inverter using only nine power switches and three capacitors per phase has been presented in this paper. The proposed topology is able to generate nine levels at the output voltages while using a single DC source. The self-balancing of capacitor voltages is achieved with two control methods, which are PMM techniques and hysteresis control. No filters or PI regulators are used, which permits a low inverter and installation cost. The high dynamics of the proposed inverter was verified by simulation.

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