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High PSRR Wide Supply Range Dual-Voltage Reference Circuit for Bio-Implantable Applications

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Abstract: On-chip systems are challenging owing to the limited size of the components, such as the capacitor bank in the rectifier. With a small on-chip capacitor, the output voltage of the rectifier might ring if the circuit experiences significant changes in current. The reference circuit is the first block after the rectifier, and the entire system relies on its robustness. A fully integrated dual-voltage reference circuit for bio-implantable applications is presented. The proposed circuit utilizes nonlinear current compensation techniques that significantly decrease supply variations and reject high-supply ripples for various frequencies. The reference circuit was verified using a 0.35 μm complementary metal-oxide semiconductor (CMOS) process. Maximum PSRR values of −112 dB and −128 dB were obtained. With a supply range from 2.8 to 12 V, the proposed design achieves 0.916 and 1.5 mV/V line regulation for the positive and negative reference circuits, respectively.

Keywords: dual-voltage reference circuit; bio-implantable; wide supply range; high PSRR

Citation: Zawawi, R.B.A.; Choi, H.; Kim, J. High PSRR Wide Supply Range Dual-Voltage Reference Circuit for Bio-Implantable Applications. *Electronics* **2021**, *10*, 2024. https://doi.org/10.3390/electronics10162024

Academic Editors: S. Abdollah Mirbozorgi and Nima TaheriNejad

Received: 31 July 2021
Accepted: 19 August 2021
Published: 21 August 2021

1. Introduction

A block diagram of the bio-implantable system is shown in Figure 1. The external system comprises a coil driver, which wirelessly transmits power to the implanted system. The transmitted power enables the operation of an implantable system comprising a rectifier, reference circuit, low dropout regulator (LDO), digital controllers, analog circuits, and stimulators. The reference circuit is the first block after the rectifier, and the entire system relies on the robustness of the reference circuit. The DC voltage is generated by passing through a rectifier and LDO from an AC power signal, which is wirelessly transmitted via an inductive link [1,2] or infrared radiation [3]. However, the misalignment of the inductively coupled coils or the infrared source sometimes reduces the power transmission efficiency. Consequently, the implanted rectifier produces an unstable output voltage ripple, which is then fed to the input terminal of the reference circuit. Therefore, the voltage reference circuit must provide a stable output over the device process, power supply, and temperature variations. Significant works on reference circuit design have been reported in the literature [4–9], where attempts were made to reduce the variations in the voltage owing to temperature variations. In detail, the prior methods were based on compensating the negative temperature coefficient of a diode-connected bipolar junction transistor (BJT) or complementary metal-oxide semiconductor (CMOS) with a positive temperature coefficient thermal voltage.

The temperature compensation, termed the curvature-compensation technique, of a first-order or higher-order nonlinear voltage or current is often limited by the operating supply voltage. Channel length modulation also occurs in the transistor when the supply voltage increases. A cascode current mirror, which enables high output impedance, was

commonly used in earlier studies to suppress the channel length modulation effect. However, at high supply voltages, a phenomenon called impact ionization in metal-oxide semiconductor (MOS) transistors creates a leakage current to the substrate that causes problems in the cascode current mirror [10].

The voltage across the drain-depletion region and drain current change the magnitude of the substrate current. This is because the drain to the substrate parasitic resistance is created (for the NMOS) in parallel with the output impedance of the MOS transistor. Thus, as the supply increases, the parasitic resistance dominates and significantly reduces the total impedance of the cascode current mirror. This effect produces a significant error in the distributing current to all branches, including the temperature compensation circuits. Consequently, the temperature compensation circuits depend on the supply voltage. Increasing the supply voltage could produce errors in the voltage or current that severely impact the line sensitivity of the reference circuit. Furthermore, these conventional methods require additional circuitry to sink the undesirable current out of the output branch or to add current to the output to compensate for the output voltage variations [11–14], resulting in an expansive layout footprint and higher power consumption. Accordingly, the typical compensation technique for voltage reference is unsuitable for implantable devices. Since our body maintains a constant temperature of 37 °C, it is essential for bio-implantable applications to increase the line regulation efficiency and decrease power dissipation rather than temperature compensation.

Motivated by this, we propose a novel reference circuit optimized for implantable devices that uses nonlinear current compensation circuits to increase the power line regulation performance and power supply rejection ratio (PSRR). The proposed reference circuit was designed using a standard SK-Hynix 0.35 µm CMOS standard process.

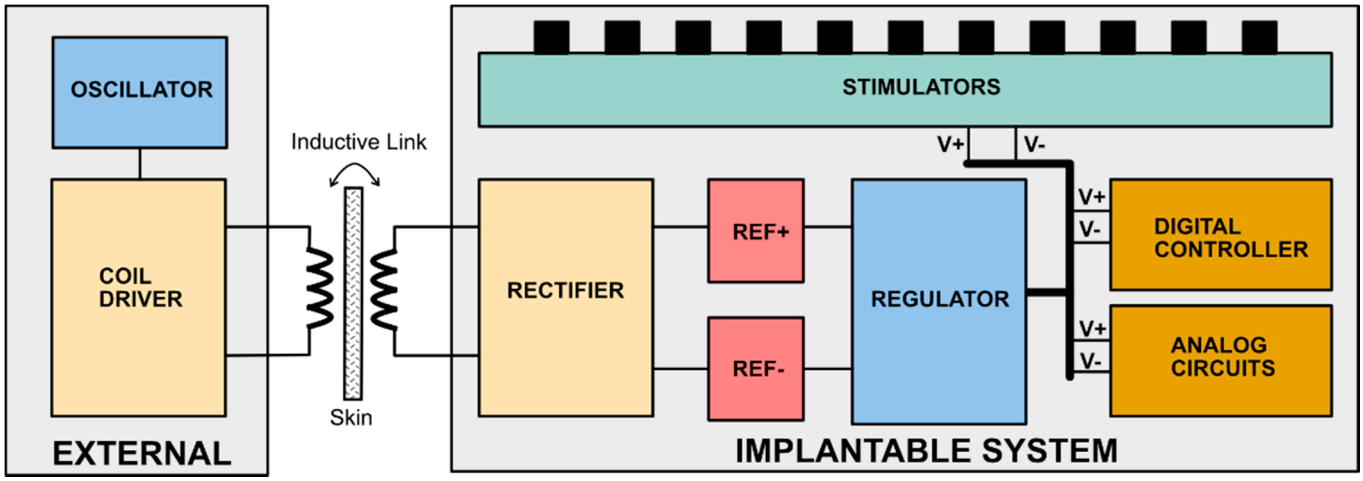

Figure 1. Bio-implantable system diagram.

The current paper extends our previous work in [15]. Our previous work focused on a positive reference only, which was used in LDO to generate a positive supply voltage. However, a negative supply in the stimulators (shown in Figure 1) is also needed to generate balanced biphasic pulses. Therefore, additional circuits, such as a charge pump circuit or inverting voltage circuit, were required in the previous work to generate the negative voltage, increasing the design's total area, due to additional components such as capacitors. The new circuit in this paper fulfils this requirement by having positive and negative references. Furthermore, it utilizes simple compensation circuits to produce excellent performance in PSRR and line regulation for positive and negative reference voltages.

2. Methods

The proposed reference circuit diagram is illustrated in Figure 2. The core circuit is based on a self-biasing gate-source voltage reference [6]. The positive reference voltage, V_{REFP}, is the established voltage across the current source circuit when both the current mirror and current source in the core circuit reach the desired operating point, as shown in Figure 2. However, an undesired operating point should be avoided because $I_1 = I_2 = 0$, a start-up circuit guarantees that the proposed circuit is not trapped in the zero-current state by initiating a current in the core circuit. The summation of V_{GS1} and V_{GS2} from $V_{GS} = V_{DS,SAT} + V_{TH}$ produces V_{REFP}. The negative reference voltage, V_{REFN}, indicates the voltage generated when I_R flows into the resistor, R. The three compensation circuits devised in this work are designated as Comp-A, Comp-B, and Comp-C in Figure 2.

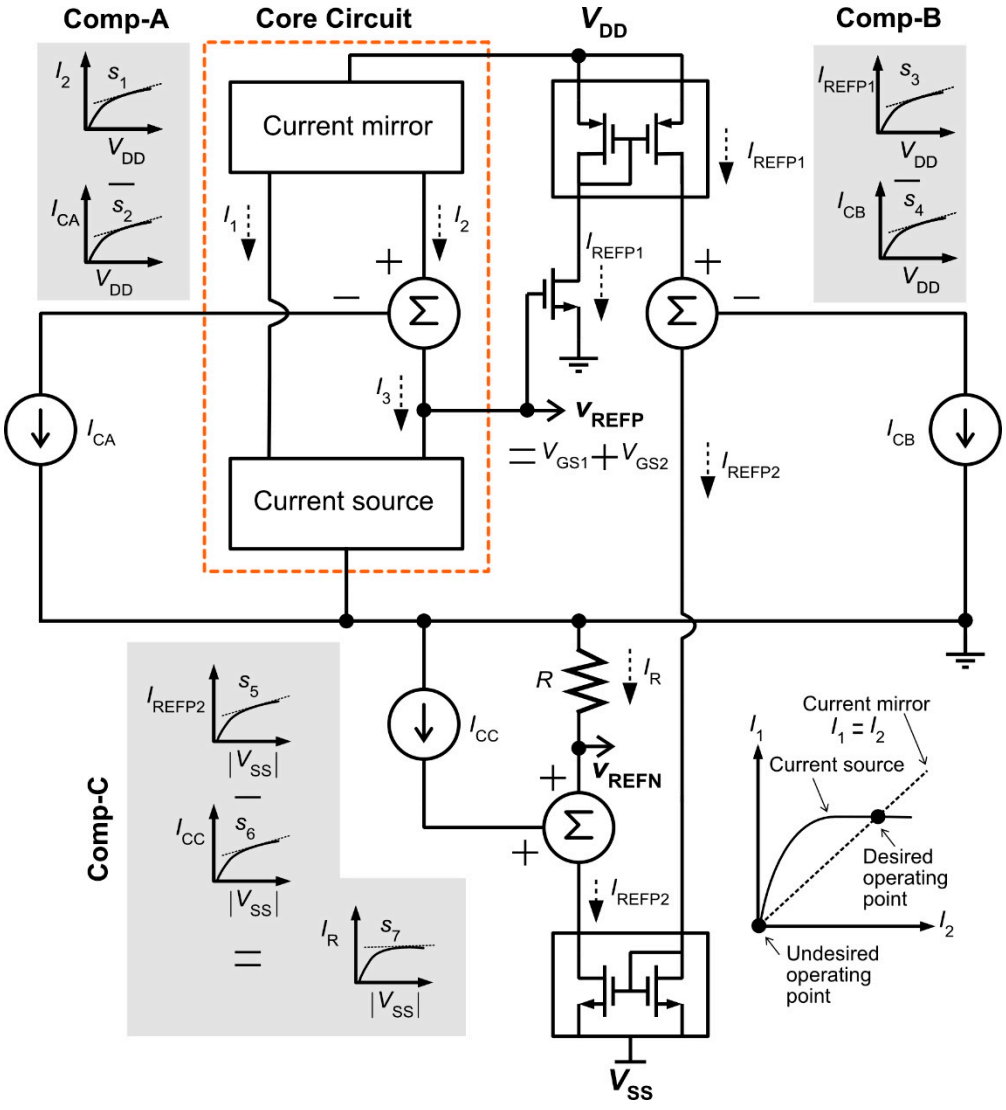

Figure 2. The proposed reference circuit diagram.

Comp-A and Comp-B aim at alleviating the supply-dependent current in I_2 and I_{REFP1}, leaving a constant current in the core and current mirror circuits. A constant current can be achieved by equalizing the slopes of S_1 and S_2, as well as those of S_3 and S_4, respectively, for Comp-A and Comp-B. Comp-C generates the current I_{CC}, which is added to the current mirror circuit. Assuming that I_{CC} and I_{REFP2} are linear currents, they may be written as

$$I_{CC} = s_6 V_{SS} + I_{CC\_DC} \quad (1)$$

$$I_{REFP2} = s_5 V_{SS} + I_{REFP2\_DC}. \quad (2)$$

where I_{CC_DC} and I_{REFP2_DC} are the DC currents of I_{CC} and I_{REFP2}, respectively. If $S_5 = S_6$, I_{CC} in Equation (1) can be written as

$$I_{CC} = s_5 V_{SS} + I_{CC\_DC}. \quad (3)$$

The current through resistor the R is given by

$$I_R = -I_{CC} + I_{REFP2} \quad (4)$$

Substituting Equations (2) and (3) into Equation (4) gives:

$$I_R = -I_{CC\_DC} + I_{REFP2\_DC} \quad (5)$$

Equation (5) suggests that an independent supply current I_R ($S_7 = 0$) is obtained if $S_5 = S_6$ (the detailed equations are provided in Appendix A). The PSRR performance is also increased by incorporating Comp-A, Comp-B, and Comp-C into the proposed circuit. The small-signal analysis that proves this idea will be presented later.

Figure 3 illustrates the proposed dual-voltage reference circuit based on the circuit diagram shown in Figure 2. When the supply is powered up, the start-up circuit sinks some current through M_{N2}, denoted as I_{SA}, which then initiates a voltage at the gate terminals of M_{P3} and M_{P4}. The current starts flowing through M_{P3} and M_{P4}, thereby establishing V_{REFP}. When V_{REFP} exceeds the threshold voltage of M_{N1}, current flows through M_{P1} and M_{P2}. The decrease in voltage at the drain terminal of M_{N1} moves M_{N1} into a deep triode region and eventually leads M_{N2} to operate in a cut-off region. M_{P6}, M_{P5}, M_{P12}, M_{N7}, and M_{P13} are newly added to the proposed reference circuit that consists of the Comp-A, Comp-B, and Comp-C circuits presented in Figure 2. The slopes of S_2, S_4, and S_6 shown in Figure 2 can be adjusted by varying the size of transistors M_{P6}, M_{N7}, and M_{P13}, respectively, as shown in Figure 3. V_{REFP} can be obtained from the circuit as:

$$V_{REFP} = V_{GS,N3} + V_{GS,N4}. \quad (6)$$

M_{N6}, M_{P7}, and M_{P9} form a current reference circuit, providing I_{REFP1} to M_{P8}. The nonlinear current in I_{REFP1} is compensated by Comp-B, resulting in I_{REFP2}, which is mirrored by M_{N10}. The constant current I_R produces V_{REFN} across R_2, given as:

$$V_{REFN} = -I_R \times R_2. \quad (7)$$

Since V_{REFN} becomes more negative if I_R increases, the source-gate voltage of M_{P13} increases and more current flows into M_{P13}. According to Equation (5), the increment in I_{CC} decreases I_R. Thus, the negative feedback loop returns V_{REFN} back to its initial value.

Figure 4a shows the equivalent circuit for the positive reference (V_{REFP}) small-signal analysis. v_{R1} can be approximately equal to v_{refp} because it is the output of the source follower circuit formed by M_{N3} and R_1 in Figure 3. Therefore, $v_{g,P2}$ can be obtained by letting

$$(v_{dd} - v_{g,P2}) g_{m,P3} = \frac{v_{g,P2}}{r_{o,N3} + R_1}. \quad (8)$$

After rearranging Equation (8) for $v_{g,P2}$, we obtain $v_{g,P2} \approx v_{dd}$, resulting in $g_{m,P4}(v_{dd} - v_{g,P2}) \approx 0$. Applying nodal analysis at the node of v_m, the following equation can be derived:

$$\frac{v_{dd} - v_m}{r_{o.P4}} = g_{m,P6}(v_m - v_{refp}) + \frac{v_m - v_n}{r_{o,P6}} + g_{m,N4}(v_{R1}) + \frac{v_{refp}}{r_{o,N4}}. \quad (9)$$

Assuming that $r_{o,P6}$ and $r_{o,N4}$ are large, Equation (9) can be simplified as

$$\frac{v_{dd} - v_m}{r_{o,P4}} \approx g_{m,P6}(v_m - v_{refp}) + g_{m,N4}(v_{R1}). \quad (10)$$

Here, v_m can be derived from the circuit written as

$$v_m \approx v_{refp}\left(\frac{g_{m,N4}}{g_{m,P5}} + 1\right). \tag{11}$$

Substituting Equation (11) into Equation (10), v_{refp}/v_{dd} can be obtained as follows:

$$\frac{v_{refp}}{v_{dd}} \approx \frac{1}{r_{o,P4}}\left(\frac{g_{m,P5}}{g_{m,P6}\cdot g_{m,N4} + g_{m,N4}\cdot g_{m,P5}}\right). \tag{12}$$

Mathematical analysis shows that v_{refp} exhibits small variations with v_{dd}. $r_{o,P4}$ in Equation (12) ensures that the ratio of v_{refp}/v_{dd} is nearly zero. The proposed Comp-A contributes $g_{m,P6}$ in Equation (12), and hence increases the PSRR performance.

A small-signal analysis of the negative reference is illustrated in Figure 4b. The signal path through M_{P10} and M_{P8} is ignored because I_{REFP1} is assumed to be an ideal current source. Assuming $g_{m,P13}, g_{m,N8} \gg \frac{1}{r_{o,P13}}, \frac{1}{r_{o,N8}}$, respectively, the r_o of M_{P13} and M_{N8} can be neglected. From Figure 4b, the total resistance, R_{TOT}, is extremely high, owing to $r_{o,N7}$; hence, we can assume that $v_x \approx v_y \approx -v_{ss}$, resulting in $g_{m,N10}(v_y + v_{ss}) \approx 0$. Applying nodal analysis at the node of v_Z, the following equation is obtained:

$$g_{m,P13}v_{refn} + g_{m,N8}(v_{ss} - v_z) = \frac{v_z + v_{ss}}{r_{o,N10}}. \tag{13}$$

and

$$v_z = \frac{v_{refn}}{g_{m,N8}R_2} - v_{ss}. \tag{14}$$

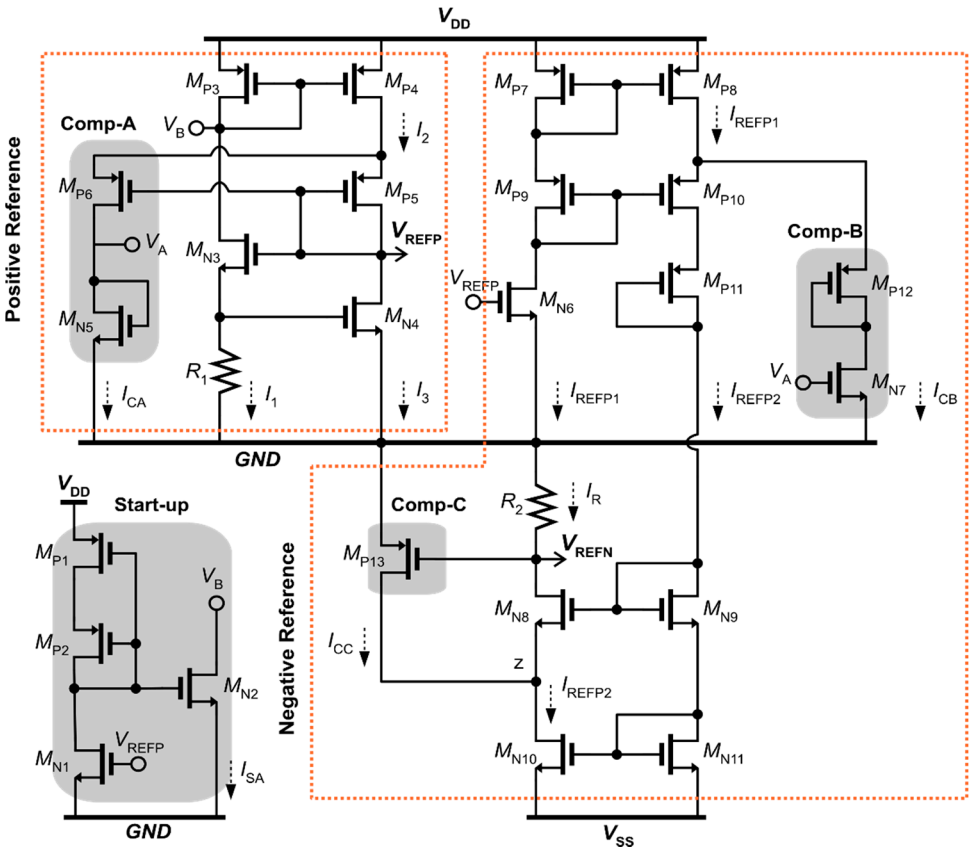

Figure 3. The circuit diagram of the proposed dual-voltage reference circuit.

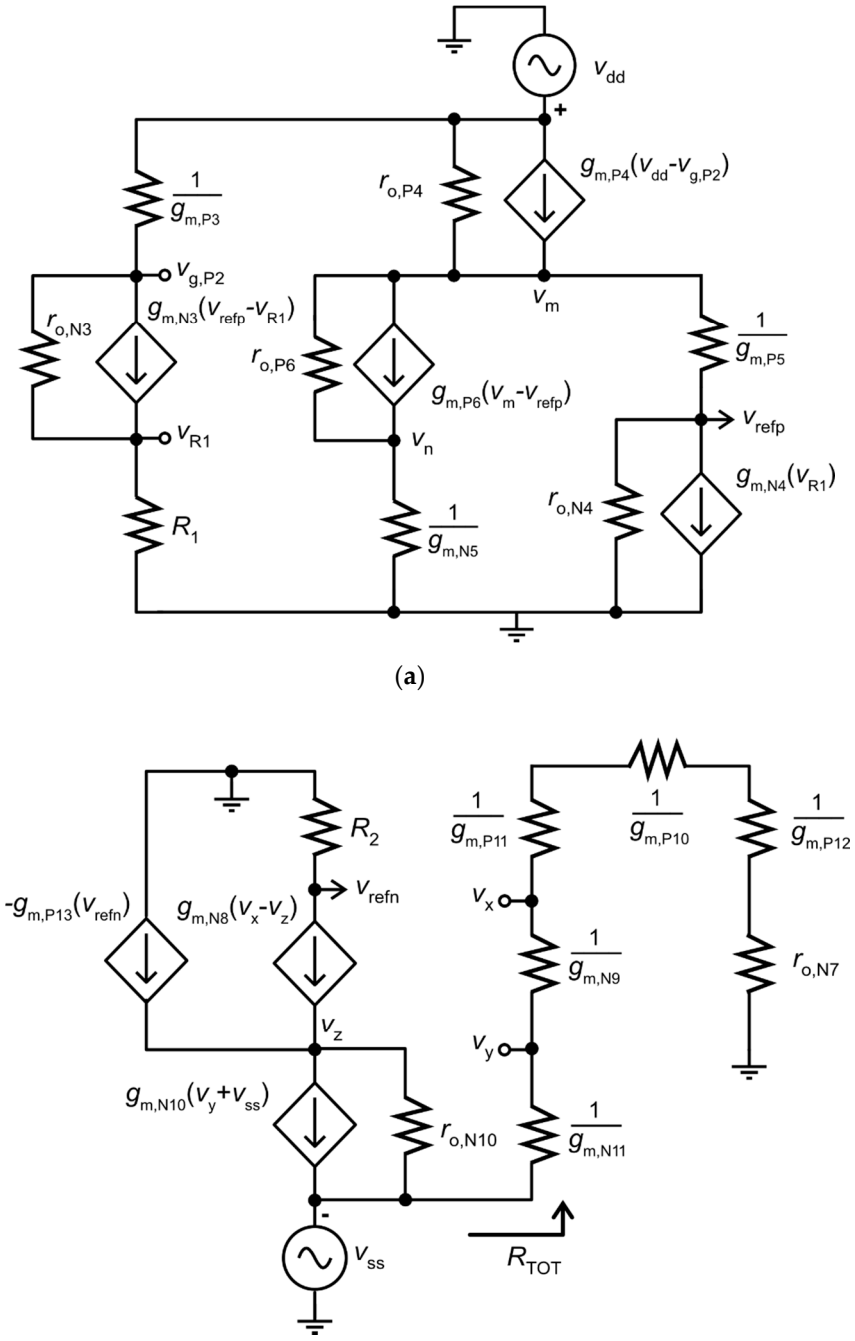

Figure 4. Small-signal equivalent circuits of the proposed circuit. (**a**) Positive reference circuit and (**b**) negative reference circuit.

Substituting Equation (14) into Equation (13) and rearranging for v_{refn}/v_{ss}, we can obtain Equation (15).

$$\frac{v_{refn}}{v_{ss}} \approx \frac{g_{m,N8}R_2}{g_{m,P13}r_{o,N10}g_{m,N8}R_2 + g_{m,N8}r_{o,N10} + 1} \approx \frac{R_2}{r_{o,N10}\left(g_{m,P13}R_2 + 1\right)}. \quad (15)$$

Equation (15) indicates that v_{refn}/v_{ss} is inversely proportional to $r_{o,N10}$. In addition, $r_{o,N10}$ is increased by a factor of $g_{m,p13}R_2$, introduced by Comp-C, which decreases the ratio v_{refn}/v_{ss}. $g_{m,p13}$ can be further increased by increasing I_{CC}; however, I_R will be reduced slightly, causing V_{REFN} to become more positive. Hence, the PSRR is limited by the minimum value of V_{REFN}.

The positive and negative reference voltages are fed into the LDO. Thus, PSRR in the LDO is influenced by the reference circuit. The PSRR performance of the LDO also includes an open-loop gain of the error amplifier and output capacitor. In practice, the reference voltage rejects supply noise at a low-frequency region only; hence a high PSRR reference at low frequency is required. The error amplifier maintains a high PSRR in the middle region until it reaches a 3-dB roll-off frequency. The output capacitor of the LDO determines the high-frequency PSRR performance. Table 1 tabulates the component parameters used for the proposed dual-voltage reference circuit.

Table 1. Parameters of the transistors and resistors used for the proposed reference circuit.

Component	Parameters	Component	Parameters
M_{P1}, M_{P2}	W = 0.5 μm, L = 25 μm	M_{N1}	W = 80 μm, L = 1 μm
M_{P3}, M_{P4}	W = 4 μm, L = 1 μm, m = 50	M_{N2}	W = 10 μm, L = 1 μm
M_{P5}	W = 1.15 μm, L = 1 μm	M_{N3}	W = 4 μm, L = 1 μm, m = 10
M_{P6}	W = 4 μm, L = 1 μm, m = 9	M_{N4}	W = 100 μm, L = 3 μm
M_{P7}, M_{P8}	W = 4 μm, L = 1 μm, m = 4	M_{N5}	W = 4 μm, L = 1 μm, m = 20
M_{P9}, M_{P10}	W = 16 μm, L = 1 μm	M_{N6}	W = 1 μm, L = 10 μm
M_{P11}	W = 4 μm, L = 1 μm	M_{N7}	W = 4 μm, L = 2 μm, m = 3
M_{P12}	W = 1 μm, L = 50 μm	M_{N8}, M_{N9}	W = 5 μm, L = 10 μm
M_{P13}	W = 4 μm, L = 1 μm, m = 62	M_{N10}, M_{N11}	W = 1 μm, L = 10 μm
R_1	70 kΩ	R_2	150 kΩ

3. Results

The proposed reference circuit was verified using a Hynix 0.35 μm CMOS standard process. As shown in Figure 5a, $V_{GS,N4}$ decreases, whereas $V_{GS,N3}$ increases with increasing V_{DD}. As I_{CA} in Comp-A increases rapidly at higher V_{DD}, V_{REFP} decreases. Thus, the slope of $V_{GS,N3}$ is assigned to be more positive than 3.5 mV/V to compensate for the variations at higher V_{DD}. M_{N7} in Comp-B senses the variations in V_{DD} and produces I_{CB}, as shown in Figure 5a, which compensates for the current variation in I_{REFP1}. The slope of I_{CB} (S_4 in Figure 2) can be adjusted by varying the size of M_{N7}. Comp-C tracks the changes in voltage at node z, as shown in Figure 3, and produces I_{CC}, which varies in the same manner as I_{REFP2}, owing to channel-length modulation. I_{CC} and I_{REFP2} vary from 10 μA to 19 μA and 15.7 μA to 24.7 μA, respectively, and consequently, a stable I_R of 5.7 μA is obtained when V_{SS} ranges from 2.8 to 12 V.

The variations in output voltage with respect to V_{DD} and V_{SS} are presented in Figure 5b. For bio-implantable applications, that is, retinal prosthetics, it is crucial to generate a negative supply voltage for producing a cathodic waveform in a biphasic pulse [14]. Accordingly, we observed a negative output reference voltage with a supply dependency of 1.583 mV/V. As shown in Figure 5a, the nonlinear I_{CC} increases in a similar fashion to I_{CA}; however, $V_{GS,N3}$ compensates for the V_{REFP} variation caused by I_{CA}. Conversely, V_{REFN} varies at a high supply voltage owing to unmatched current rate changes in I_{CC} and I_{REFP2}. Thus, the negative reference line regulation is larger than the positive reference line regulation (0.916 mV/V).

The elaborate corner results for line regulation are shown in Figure 5c, according to which the compensation circuits proposed in this work can generate stable reference voltages in various environments. Furthermore, the positive and negative PSRR results with respect to V_{DD} and V_{SS} are plotted in Figure 5d, where the maximum PSRRs of −112 and −128 dB were obtained for V_{REFP} and V_{REFN}, respectively. The PSRR difference between V_{REFP} and V_{REFN} arises from the different factors in the denominator; $r_{o,P4}$ in Equation (12) increases by a factor of $g_{m,N4}(g_{m,p5} + g_{m,p6})$, while $r_{o,N10}$ in Equation (15) increases by approximately $g_{m,P13}$.

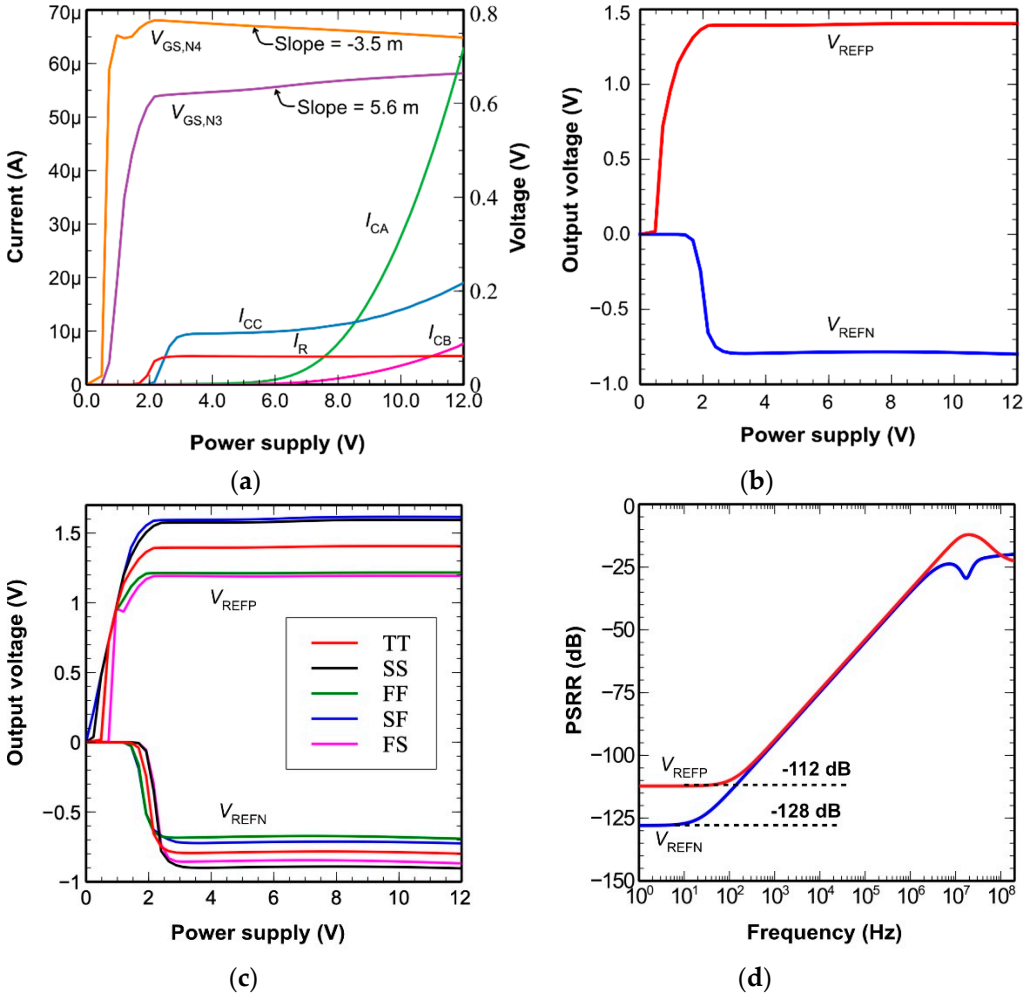

Figure 5. Results of (**a**) DC responses of $V_{GS,N3}$, $V_{GS,N4}$, I_{CA}, I_{CB}, I_{CC}, and I_R, (**b**) line regulation at typical condition ($0\ V \le V_{DD} \le 12\ V$ and $-12\ V \le V_{SS} \le 0$), (**c**) line regulation in different corners, and (**d**) PSRR.

Finally, the overall performance of the proposed reference is tabulated in Table 2 and compared with the previous voltage reference circuits presented in [12,13,16]. The line regulation obtained was higher than those in [13,16], but lower than that in [12]. However, the proposed reference circuit exhibits excellent PSRR compared with [12,13,16]. The voltage range was 9.2 V, close to [13], while the corresponding quantities for [12,16] were 3 V and 0.5 V, respectively, indicating that the proposed work is robust to wide supply changes. Considering the accuracy and stability, the proposed reference circuit with excellent line regulation and PSRR is suitable for a wide supply and high precision LDO. In addition, the proposed negative reference could possibly replace the charge pump circuit, which is typically used to generate negative voltage.

Table 2. Overall performance and comparison.

Parameter	This Work	[12]	[13]	[16]
Technology (μm)	0.35	0.35	1.6	0.18
Supply voltage (V)	2.8~12	2~5	2.6~12	1.3~1.8
V_{REF} (V)	1.4 (V_{REFP}) −0.8 (V_{REFN})	1.14	1.6	1.17

Line regulation (mV/V)	0.916 (V_{REFP}) 1.583 (V_{REFN})	2	0.511	0.35
PSRR (dB)	−112 (V_{REFP}) −128 (V_{REFN})	−61	−59.2	−52

4. Conclusions

A high-PSRR wide-supply range dual-voltage reference circuit was proposed. In practice, the reference circuit needs to reject power supply noise only at low frequencies (usually a few tens of Hz), because the LDO error amplifier feedback ensures high PSRR for the remaining frequencies. Hence, the PSRR of −112 and −128 dB obtained from the positive and negative references, respectively, minimize the supply noise from the implanted LDO at low frequencies. When the supply ranged from 2.8 to 12 V, line regulation performances of 0.916 and 1.583 mV/V were obtained for the positive and negative references, respectively. The proposed circuit is suitable for retinal prosthetic applications because balanced biphasic pulses in the stimulators can be generated by supplying stable positive and negative voltages, thereby avoiding damage to body tissues. Presently, a back telemetry digital controller and a dual-voltage LDO that incorporates the proposed reference circuit are under development. These designs will be fully integrated with 256-pixel stimulators and implanted in a pig's eyeball after in vitro testing.

Author Contributions: Conceptualization, R.B.A.Z., and J.K.; methodology, R.B.A.Z., H.C. and J.K.; writing—original draft preparation, R.B.A.Z., H.C. and J.K. Supervision, H.C. and J.K.; funding acquisition, H.C. and J.K. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Korea Medical Device Development Fund grant funded by the Korea government (the Ministry of Science and ICT, the Ministry of Trade, Industry and Energy, the Ministry of Health & Welfare, the Ministry of Food and Drug Safety) (Project Number: 202017D01). This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (No. 2020R1A2C4001606).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are included in the article.

Acknowledgments: The authors would like to express their sincere appreciation to the IC Design Education Center for chip fabrication.

Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

PSRR	Power supply rejection ratio
LDO	Low-voltage drop regulator
BJT	Bipolar junction transistor
CMOS	Complementary metal-oxide semiconductor
MOS	Metal-oxide semiconductor
NMOS	N-channel metal-oxide semiconductor

Appendix A

From the proposed circuit in Figure 3, we have

$$I_{CC} = I_{D_{P13}}(1 + \lambda_p V_{SD_{P13}}). \quad \text{(A1)}$$

We can write the slope of S_6 in Figure 2 as

$$\frac{\delta I_{CC}}{\delta_{|V_{SS}|}} = \frac{\delta I_{CC}}{\delta_{V_{SD\_P13}}} . \frac{\delta V_{SD\_P13}}{\delta_{|V_{SS}|}} = S_6 \tag{A2}$$

where $\frac{\delta I_{CC}}{\delta_{V_{SD\_P13}}} = I_{D\_P13}.\lambda_p$ obtained from Equation (A1). For simplification $\frac{\delta V_{SD\_P13}}{\delta_{|V_{SS}|}}$ is approximated 1, hence

$$S_6 = I_{D\_P13}.\lambda_p. \tag{A3}$$

From Figure 3, we know

$$I_{REFP2} = I_{REFP1} - I_{CB} \text{ and} \tag{A4}$$

$$I_{REFP1} = I_{D\_N6}\left(1 + \lambda_n V_{DS_{N6}}\right). \tag{A5}$$

The slope of S_3 is obtained as follows

$$\frac{\delta I_{REFP1}}{\delta_{V_{DD}}} = \frac{\delta I_{REFP1}}{\delta_{V_{DS\_N6}}} . \frac{\delta V_{DS\_N6}}{\delta_{V_{DD}}} = S_3. \tag{A6}$$

By assuming $\frac{\delta V_{DS\_N6}}{\delta_{V_{DD}}} = 1$, hence

$$S_3 = I_{D\_N6}.\lambda_n. \tag{A7}$$

The variation of I_{REFP2} with respect to V_{DD} can be written as

$$\frac{\delta I_{REFP2}}{\delta_{V_{DD}}} = S_3 - S_4 \tag{A8}$$

or

$$\frac{\delta I_{REFP2}}{\delta_{|V_{SS}|}} = I_{D\_N6}.\lambda_n - S_4 = S_5. \tag{A9}$$

S_7 equal to 0 if $S_5 = S_6$, therefore

$$I_{D\_N6}.\lambda_n - S_4 = I_{D\_P13}.\lambda_p. \tag{A10}$$

The slope of S_5 can be controlled by adjusting S_4. The following derivation is for obtaining S_4. First, I_{CB} is assumed in the saturation region,

$$I_{CB} = \frac{1}{2} K_n \left(\frac{W}{L}\right)_{N7} (V_A - V_{TH})^2. \tag{A11}$$

S_4 is obtained from the following equation:

$$\frac{\delta I_{CB}}{\delta_{V_{DD}}} = \frac{\delta I_{CB}}{\delta_{V_A}} . \frac{\delta V_A}{\delta_{V_{DD}}} = S_4. \tag{A12}$$

By assuming $\frac{\delta V_A}{\delta_{V_{DD}}} = 1$, hence

$$\frac{\delta I_{CB}}{\delta_{V_{DD}}} = K_n \left(\frac{W}{L}\right)_{N7} (V_A - V_{TH}) = S_4. \tag{A13}$$

Equation (A13) suggests that the size of M_{N7} adjusts the slope of S_4.

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