coatings

MDPI

Project Report

A Study on the Gap-Fill Process Deposited by the Deposition/Etch/Deposition Method in the Space-Divided PE-ALD System

Baek-Ju Lee *, Dong-Won Seo and Jae-Wook Choi

Vacuum Equipment R&D Division, Advanced Technology TF, Hanwha Corporation, 305, Pangyo-ro, Seongnam 13488, Republic of Korea
* Correspondence: baekju.lee@hanwha.com

Abstract: This study concerns the development of a gap-fill process technology for isolating trench patterns. There are various gap-filling techniques in the case of trench patterns; nevertheless, a processing technology adopting the DED (deposition/etch/deposition) method was developed in this study. After the etch step, an Ar/O_2 (1:2) plasma treatment technology reduced the residual amount of F in the films to 0.05%. By improving the etch uniformity, the deposition uniformity after the DED process on a 12-inch flat wafer was secured within <1%, and a high-quality SiO_2 thin film with a dielectric constant of 3.97 and a breakdown field of 11.41 MV/cm was fabricated. The DED method can be used for gap-filling even in patterns with a high aspect ratio by changing process parameters, such as RF power and division of etch steps, according to the shape, depth, and CD size of the pattern. This study confirmed that a void-free gap-fill process can be developed in a trench pattern with a maximum aspect ratio of 40:1.

Keywords: PE-ALD; deposition/etch/deposition; shallow trench isolation; fluorine concentration; gap-fill

Citation: Lee, B.-J.; Seo, D.-W.; Choi, J.-W. A Study on the Gap-Fill Process Deposited by the Deposition/Etch/Deposition Method in the Space-Divided PE-ALD System. *Coatings* **2023**, *13*, 48. https://doi.org/10.3390/coatings13010048

Academic Editor: Amin Bahrami

Received: 1 December 2022
Revised: 19 December 2022
Accepted: 21 December 2022
Published: 27 December 2022

1. Introduction

As the integration degree of the semiconductor device increases, the line width and spacing between the components of the semiconductor device gradually become finer, including the width and interval of the device isolation layer. Thus, instead of the conventional local oxidation of silicon processes for the device isolation layer, a shallow trench isolation technique, in which a narrow and deep trench is formed in a semiconductor substrate and then gap-fills with insulating materials, is mainly used. However, although the gap-filling process fills the trench with an insulating film by sequentially depositing an insulating film from the bottom of the trench, due to an overhang phenomenon that occurs when an insulating film is simultaneously deposited on the entrance, sidewalls, or the bottom surface of trenches, the top of the trench could be blocked before the trench is completely gap-filled, generating voids or seams inside the trench. Such voids occur more frequently as the aspect ratio of the trench increases, causing these voids to deteriorate the device's characteristics. Therefore, one of the important process goals in trench gap-filling processes is to suppress the generation of voids. Since the gap-filling process is a deposition process, the conventional chemical vapor deposition (CVD) method is primarily used. However, the CVD method cannot be used as the integration degree of semiconductor devices and the aspect ratio of the trench increase. Hence, trenches have recently been gap-filled using the plasma-enhanced atomic layer deposition (PE-ALD) method using plasma, where particularly generating high-density plasma under a low-pressure atmosphere is a core element of the gap-filling process. However, the PE-ALD method also has limitations in its gap-fill capability due to the high integration

of semiconductor devices. Besides, as the width of the trench becomes narrow, an overhang is generated at the entrance to the trench, resulting in a void inside the trench even when the trench gap-fill process is performed using the PE-ALD method. Thus, a novel deposition/etch/deposition (DED) process has been proposed to address this problem, where deposition and etching of an insulating film are repeated using the PE-ALD method [1,2]. It is a process of etching the overhang generated from the PE-ALD method and redepositing it via the PE-ALD method. Still, if the etching uniformity is poor and the opening size varies, the gap fill would not be uniform throughout the trench. Furthermore, as the gap-filling space becomes smaller, the three-step DED process becomes increasingly impossible, thereby requiring five or more steps [3,4]. As a result, since the deposition and etching uniformities must be met for an effective deposition/etch/deposition process, while the single/batch type is excellent in terms of deposition uniformity or particle size, the space-divided type, which has a greater advantage in terms of productivity, has also been actively researched. Additionally, in the case of the existing space-divided PE-ALD systems, only the disk, not the wafer, rotates, causing the process gas stream to be formed toward the chamber wall due to the centrifugal force generated by the rotation of the disk, which results in poor deposition uniformity. In this condition, during the DED process, the etch uniformity in all areas of the wafer is also poor, resulting in reduced device yield. Based on the above facts, this study developed an independent rotational device disk, which rotates its disks and wafers simultaneously, to solve the problem with space-divided PE-ALD systems and improve the implementation of a silicon oxide circular map without deposition uniformity. This model was proposed because since the shape of the deposition map could be controlled when the disks and wafers are rotated simultaneously, the disk rotation, which enables control of the deposition speed per cycle, was utilized as a controlling factor for thin-film quality and step coverage, causing the rotation of the wafer to be utilized as a controlling factor for deposition thickness in the outermost edge area. Alternately, since factors that can control the deposition thickness of the outermost edge area could also be utilized to control the etching speed not only in the deposition process but also in the etching process, a silicon-insulating film was primarily used as an oxide film in a semiconductor device. However, although the silicon-insulating layer was easily etched in an acid-based chemical solution, controlling the thickness of the insulating layer during the etching process remained challenging. In such cases, the insulating film is penetrated when the silicon is wet-chemical-etched in an acid-based chemical solution, causing the insulating film to fail in its function as an insulating film. To solve this problem, this study also describes a semiconductor device capable of gap-filling without voids while forming an insulating layer on the semiconductor substrate with a trench, thereby preventing the insulating layer from being easily etched in an acid-based chemical solution.

2. Experiments and Discussion

2.1. Experimental Method

2.1.1. Development of the Experimental Equipment

Existing ALD equipment are single/batch or space division types. While the single/batch type is excellent in terms of deposition uniformity and defects, research on the space division type is still being actively conducted [5,6] because of its productivity. Moreover, findings have revealed that with the space division type, the physical and chemical properties of the deposited film could be improved by strengthening the upper lead plasma system. Therefore, this study installed a self-developed dual-plasma system to investigate its improvement in gap filling. The PE-ALD space division system used in this study was equipped with eight shower heads on the top lid, after which precursor, purge, and reactant gases were continuously sprayed in each area. Particularly, since the purge gas separated the precursor from the reactant regions, deposition and treatment functions were performed through plasma discharge in the reactant region. Then, while six wafers

were arranged on a disk that rotated and passed through each space-divided area, the precursors repeated chemical adsorption and desorption reactions to form thin films. We also observed that since the existing space division PE-ALD system was designed to rotate only the disk, the uniformity of the deposited thin film was poor. As a result, while the pumping port inside the chamber was located in the precursor and reactant regions, the gas stream was formed toward the chamber wall via the centrifugal force generated during the disk rotation. Hence, this study solved these complexities by designing the disk and wafer to simultaneously rotate. Consequently, the wafer rotation speed was up to 10 rpm, and the disk was up to 200 rpm. The wafer rotation also controlled the deposition thickness of the outermost region, increasing the disk rotation speed and productivity. The disk rpm refers to the number of ALD depositions per minute. In addition, while 60 cycles per minute were performed at 60 rpm, the wafer was rotated at 5 rpm to evaluate one second per ALD cycle (Figure 1).

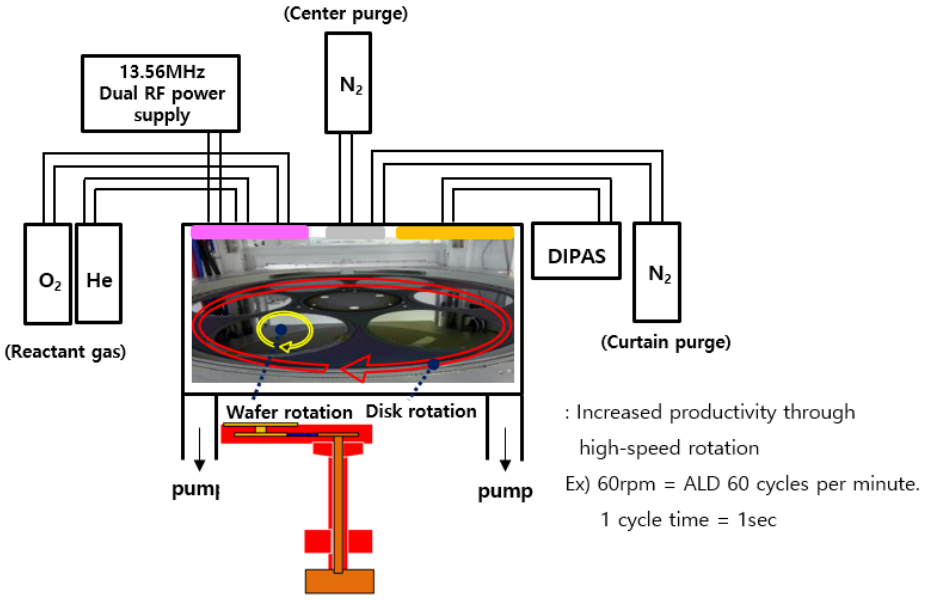

Figure 1. The DED process system development.

2.1.2. Deposition Process

This study was conducted using a space-divided PE-ALD facility, where diisoprophylaminosilane (DIPAS) was the precursor to form a silicon oxide thin film on the 12-inch Si (100) wafer, O_2/He was used as the reaction gas, N_2 was the purge gas, and the gas flow rate of O_2/He was adjusted to 3:2. Meanwhile, for plasma formation, while an RF voltage of 13.56 MHz was dually applied to the upper chamber, 300 w/300 w was applied, respectively, at a process pressure of 0.6 torr. Typically, increasing the deposition temperature increased the density of the deposited film (Figure 2); thus, an appropriate temperature of 500 °C was applied to ensure that the DIPAS precursor did not thermally decompose [7,8]. Furthermore, the distance between the disk and showerhead was set to 7 mm, and the disk and wafer rotation speeds were set to 60 and 5 rpm, respectively, for depositing the silicon oxide thin film. While the space division-type atomic layer deposition comprised six steps, adopting the same principle as shown in Figure 3, on the substrate, the precursors were deposited via continuous chemical adsorption and desorption. When depositing a thin film, the aspect ratio was crucial because the higher the aspect ratio, the more complex the process was due to the deterioration of step coverage characteristics. As the aspect ratio increased, the pattern inside adopted the shape of a curved jar, causing voids or seams to appear inside the pattern during the gap-filling process. Notably, the sticking coefficient and arrival angle are two factors for improving step coverage. The

sticking coefficient denotes the probability of chemical adsorption to the substrate in a single collision. As the sticking coefficient increases, the surface mobility decreases, thereby deteriorating the coating ability. Therefore, while the sticking coefficient should be small, the arrival angle depends on the pressure. Moreover, the higher the pressure, the smaller the mean free path; thus, the randomness of the particles increases. As a result, atoms tended to cluster at the side with a greater arrival angle, forming an overhang. When the overhang was formed, voids were also formed, causing the covering ability to be greatly reduced.

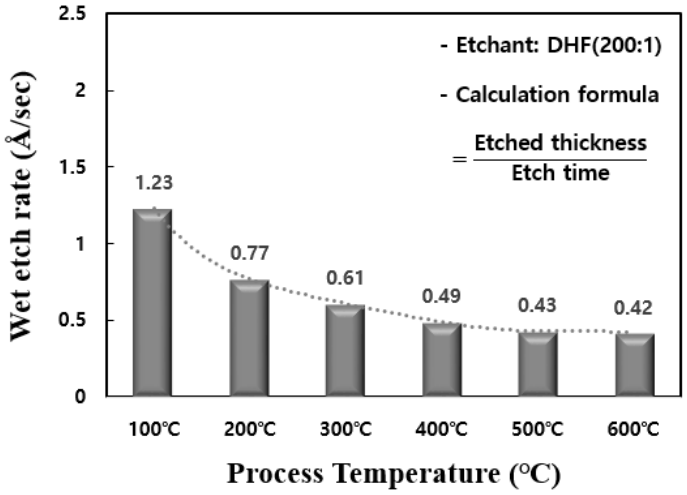

Figure 2. Wet etch rate characteristics of SiO_2 thin film at various process temperatures.

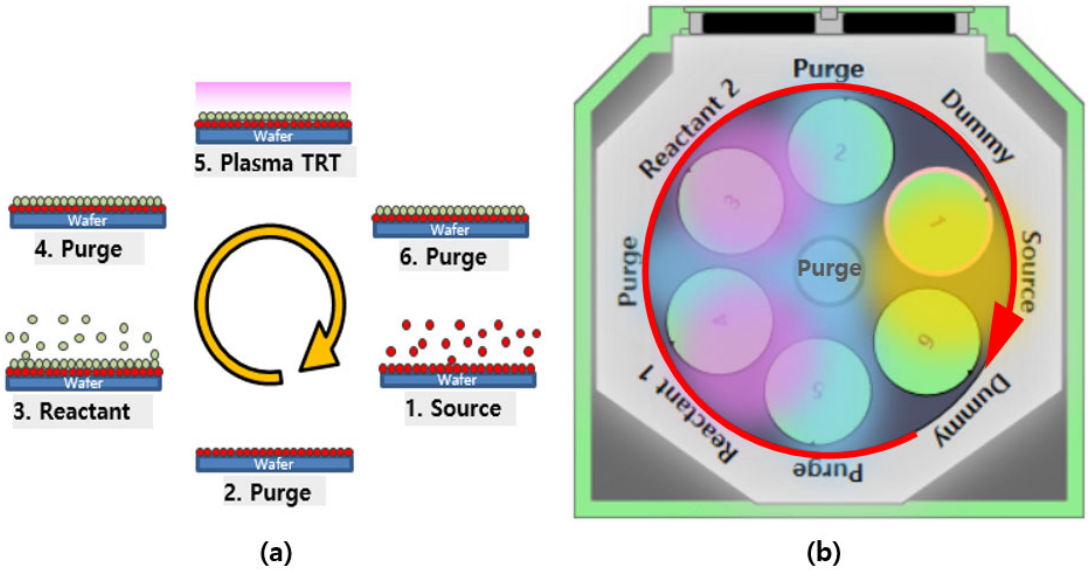

Figure 3. (**a**) Principle of PE-ALD. (**b**) The space division PE-ALD sequence.

2.1.3. Etch Process

In this study, an etch step was added in the middle of the deposition process to solve the overhang problem and improve the gap-fill performance. The etch step was configured in the same manner as in the deposition conditions with a dual-RF voltage of 13.56 MHz, and 500 w/500 w were applied to each. After the source injector was turned off, NF_3 gas was injected into the reactant injector (1 and 2) to perform the etch process. At this time, the plasma discharge area was increased by turning off the curtain purge between reactant injector 1 and reactant injector 2. In the etch step, the most important issues are

increasing productivity by increasing the etch rate and increasing the yield by improving etch uniformity over the entire wafer area. Etch uniformity refers to the consistency of the etch rate across all regions of a wafer. The difference between the most advanced and least advanced etch sites can be calculated by dividing it by the sum. The calculation (Formula (1)) is as follows:

$$\text{Etch uniformity (\%)} = (\text{max E.R.} - \text{min E.R.})/(\text{max E.R.} + \text{min E.R.}) \times 100\% \quad (1)$$

(E.R. = etch rate)

In the case of bad etch uniformity, a difference in the thickness of the film at the center and the edge will be noticed after etching, resulting in a difference in the characteristics of a device and ultimately leading to a lower yield in the manufacturing process. In this experiment, etch uniformity was calculated by averaging the etch rate of 49 points across all regions of a 12-inch wafer. Figure 4a is a graph showing etch uniformity and the etch rate according to the NF_3 flow rate, and Figure 4b is a graph showing etch uniformity according to wafer rpm. In Figure 4a, it can be seen that the etch rate increases as the NF_3 flow rate increases from 2500 to 5000 sccm. However, a tendency of etch uniformity to deteriorate from 0.4% to 1.1% was confirmed. Applying NF_3 4000 sccm was expected to be most suitable in terms of etch rate and etch uniformity, so it was applied to this evaluation. In the Figure 4b, it can be seen that the etch uniformity improves from 1.1% to 0.5% as the wafer rpm increases. As the wafer rotates, the high and low etch rates intersect, and the etch uniformity improves as the rpm increases. From the time of the 5 rpm application, it was confirmed that the uniformity tendency was saturated, and thus the etch process was performed at 5 rpm.

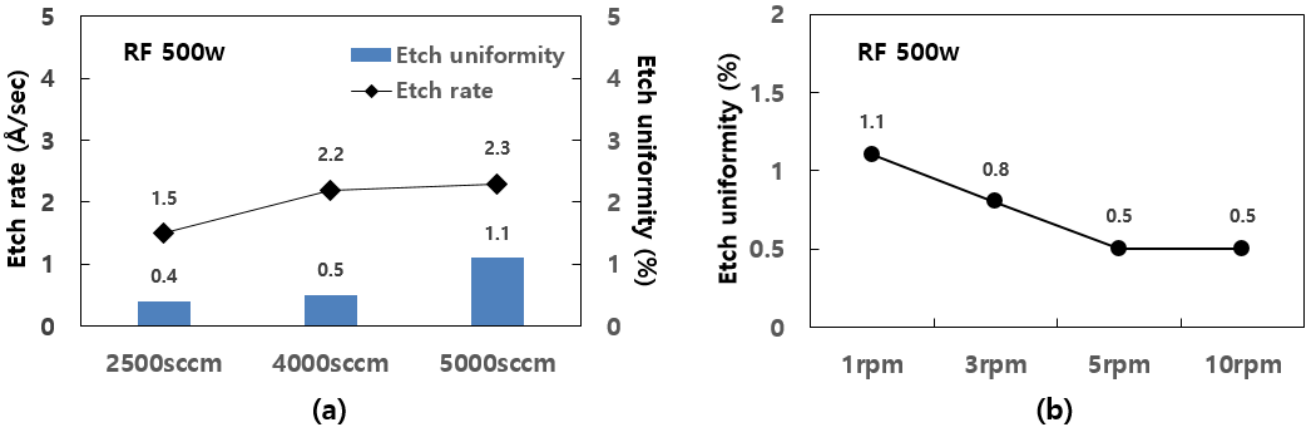

Figure 4. (**a**) Trend of etch rate and etch uniformity according to NF_3 flow rate. (**b**) Trend of etch uniformity with increasing wafer rpm.

2.1.4. Analysis Method

The thickness of the thin film deposited on the flat plate was measured using the Elli-SE-Uam12 model ellipsometer manufactured by Ellipso Technology (Suwon, Korea). The deposition thickness on the flat plate was measured as the average value and uniformity in the 49-point area measured on a 12-inch wafer. For component analysis of the deposited thin film, XPS (TFS K-Alpha+, Rigaku, Kyoto, Japan) and SIMS (CAMECA IMS 7f magnetic sector SIMS, JEOL, Tokyo, Japan) analyses were performed, and C-V and I-V characteristic analyses were performed using MS Tech's MST 8000 CHC model. To confirm the gap-fill image, a pattern with an aspect ratio of 40:1 was used, and FIB (Focused Ion Beam) sampling was performed on the central part of the 12-inch wafer to analyze the thin-film growth rate through transmission electron microscopy (TEM) (JEM-2100F HR, JEOL, Tokyo, Japan) analysis.

2.2. The Deposition/Etch/Deposition Process Development

2.2.1. Silicon Oxide Thin Film Deposited by the PE-ALD Method

As a result, a thin layer of silicon oxide is deposited on the substrate via the reaction of the adsorbed molecules with the oxygen plasma formed in the chamber. During this process, He/O_2 was also used as a reactant gas since adding inert gases, such as He or Ne, to O_2 could result in the formation of an oxygen-based plasma with an increased population density of reactive species (atomic oxygen, oxygen radicals, or excited oxygen species). Furthermore, when plasma was generated from the gas mixture comprising an oxygen precursor and additional gas, the pressure in the reaction chamber was more than that during the conventional PE-ALD processes, indicating that an increase in the population density of reactive species was possible [9–11]. Subsequently, XPS analysis was performed to confirm whether a normal silicon oxide thin film was deposited. As a result of XPS analysis, an O_{1s} peak was found in the 532.6 eV binding energy section, and a $Si_{2}p$ peak was found in the 103 eV binding energy section; thus, the silicon oxide thin film was determined to have been properly deposited (Figure 5a,b). According to the composition analysis results (Figure 5c), the concentrations of C and N were measured to be <1% and the concentration ratios of Si and O were determined to be 1:2. Figure 6 presents a graph showing the tendency of the deposition rate according to the reactant gas O_2 and He flow rates. The deposition rate is confirmed to increase when He is added compared to when only O_2 is used. In general, the deposition rate per cycle of the silicon oxide thin film deposited by the normal ALD reaction is less than 1 Å, and it can be confirmed that the ALD reaction normally occurs up to an O_2:He ratio of 3:2 [12–14].

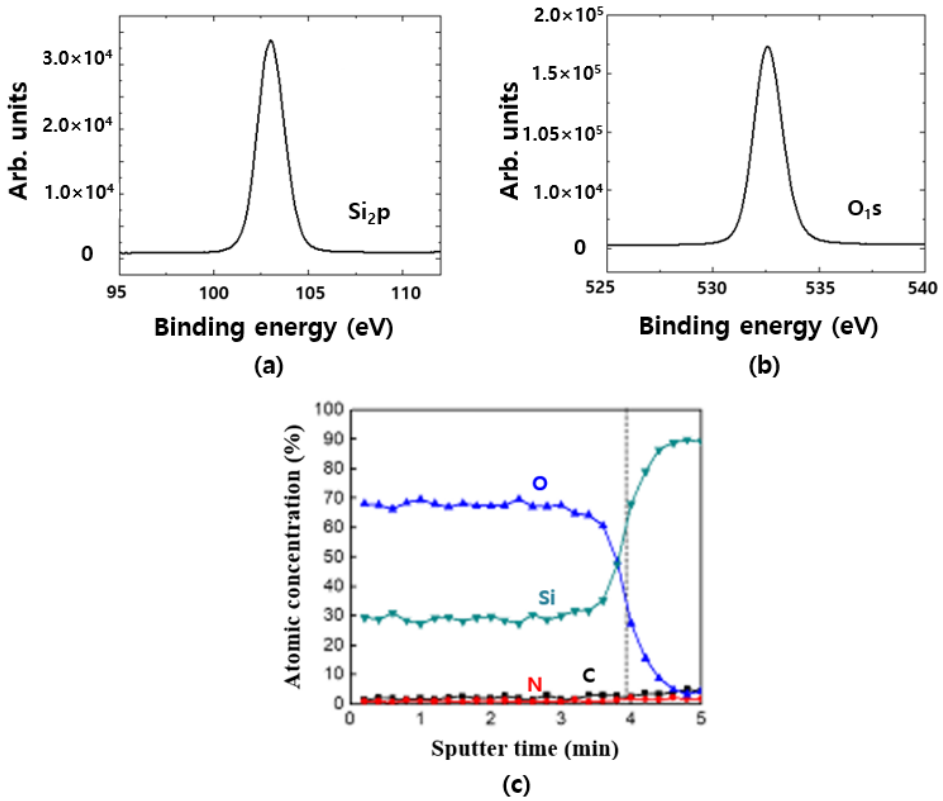

Figure 5. XPS spectra of SiO_2 are also shown: (**a**) $Si_{2}p$ and (**b**) O_{1s}. (**c**) Deposited thin-film composition analysis.

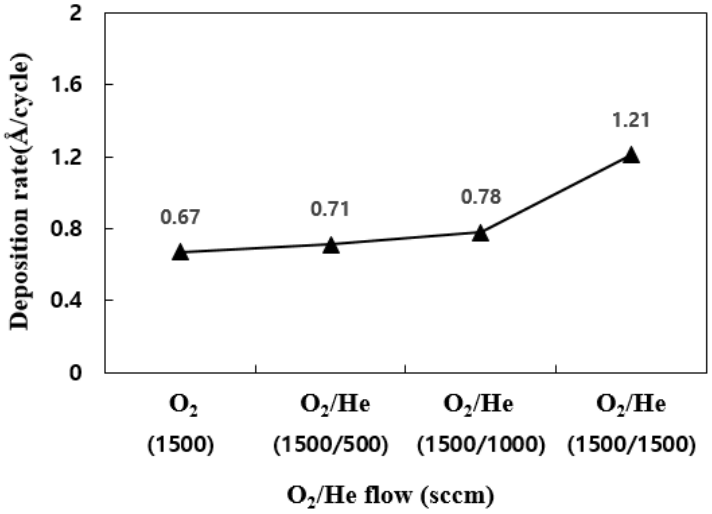

Figure 6. Reactant gas O_2: deposition rate trend according to He flow rate.

2.2.2. DED Process Method

In this study, an etching step was added to the middle of the silicon oxide thin-film deposition to remove the overhang, causing the silicon oxide thin film to be redeposited. First, the thickness and uniformity of the flat wafers were compared under the aforementioned deposition conditions with and without the etch step (Figure 7). After the etch step was performed at 10 and 30 s, the effect of an increased etching time was then investigated. We observed that as the etching time increased, the deposition thickness decreased from 200.4 to 172.5 Å, improving the deposition uniformity from 0.96% to 0.75%. The chemical reaction (Formula (2)) of the silicon oxide thin film and the NF_3 gas is as follows:

$$SiO_2(s) + NF_3(g) \rightarrow SiF_3(g) + NO_2(g) \quad (2)$$

SiF_3 generated in the reaction step vaporizes and is eliminated from the substrate surface. At this time, the fluorine ions mainly participate in the elimination reaction of SiO_2, and the NF_3 gas is ionized in the plasma state. The degree of ionization depends on the flow rate of NF_3 and the plasma power [15,16]. The results of this study showed that the elimination rate of the silicon oxide thin film was high when the flow rate of the NF_3 gas was 4000 sccm and the plasma power was 500 w. In addition, Figure 8 describes the aforementioned elimination reaction, and the chemical species participating in this reaction is the fluorine ion. Fluorine ions interpose between Si and O and break the Si-O bond, and this reaction is highly exothermic (Figure 8a). Additionally, recombination occurs with fairly low activation energy, leaving Si-F bonds by coulomb attraction (Figure 8b). Here, since Si-N binding energy is 4 eV and that of Si-F is 6 eV, Si-F is more thermodynamically stable [17–19]. However, after NF etching, the wafer is terminated with the nitrogen remaining after the reaction. As the difference in electronegativity between Si and F (Si: 1.8, F: 3.9) is too large, the Si-F bond causes polarization, in which NF breaks the Si-Si bond by back-bonding (Figure 8c). This reaction terminates nitrogen on the surface by releasing SiFx and leaving O-N (Figure 8d). This reaction was obtained by molecular orbital calculation of the activation energy [20–23]. It is known that trace amounts of nitrogen in the silicon oxide thin films do not deteriorate film properties, and this nitrogen termination phenomenon on the wafer is used as an inhibitor in other research activities as a gap-fill process [15].

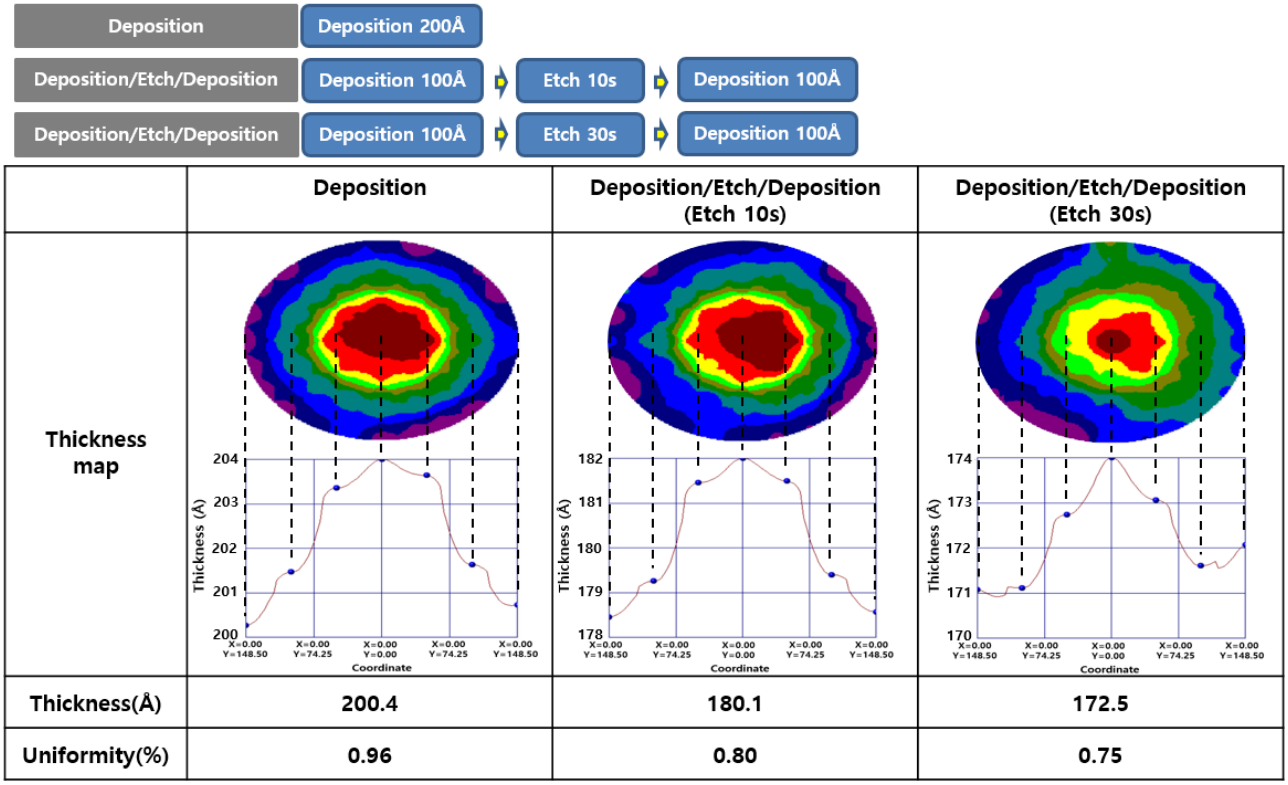

Figure 7. The thickness and uniformity of the silicon oxide thin film deposited via the DED method on a flat plate.

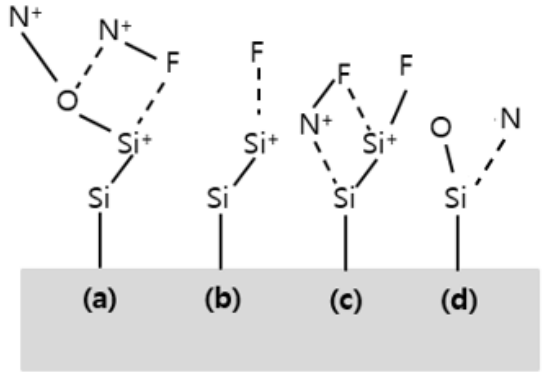

Figure 8. Etching mechanism of the silicon oxide thin film using NF_3. (**a**) Fluorine ions interpose between Si and O and break the Si-O bond. (**b**) leaves a Si-F bond. (**c**) NF breaks Si-Si bonds by back bonding. (**d**) Releases SiFx and leaves O-N

2.2.3. Fluorine Analysis of SiO_2 Thin Film Deposited by the DED Process

In general, the byproducts of fluorine atoms that are involved in the silicon oxide elimination reaction during dry etching are well-adsorbed on the surface of the Si wafer due to the high electronegativity of fluorine atoms [24,25]. Additionally, it is known that the amount of fluorine remaining on the wafer surface after etching is higher than that of wet etching [26]. Figure 9 is the result of the SIMS analysis of the thin film to which the DED process was applied to. After dry etching, the concentration of fluorine incorporation in the film was confirmed at 0.18%. The fluorine remaining on the surface after etching in this way makes the wafer surface hydrophilic and has high electronegativity, which can cause other contaminants to be adsorbed well to the wafer, thereby lowering the interface properties, and lowering the quality of the device [27,28]. Therefore, to remove fluorine

remaining on the surface after dry etching, surface treatment was performed using Ar and O_2 plasma after NF_3 plasma etching. The O_2 plasma process, which is mainly used to remove etch residues, is also called the ashing process, and has a mechanism to remove etch residues by converting them into volatile substances such as OF_2 and O_2F_2 [29]. After the etch step during the DED process, plasma treatment was used on the surface with an Ar and O_2 ratio of 1:2 and RF of 500 w/500 w. It was confirmed that the concentration of fluorine incorporation in the membrane decreased by 0.05% (Figure 9). Although Ar and O_2 plasma did not completely eliminate the remaining fluorine on the substrate, it was confirmed that the amount of fluorine was reduced compared to the case where only dry etching was performed. This suggests that Ar and O_2 energy may play a role in breaking the bonds of Si-F and Si-OF present on the surface of the oxide film and terminating with Si-O [30].

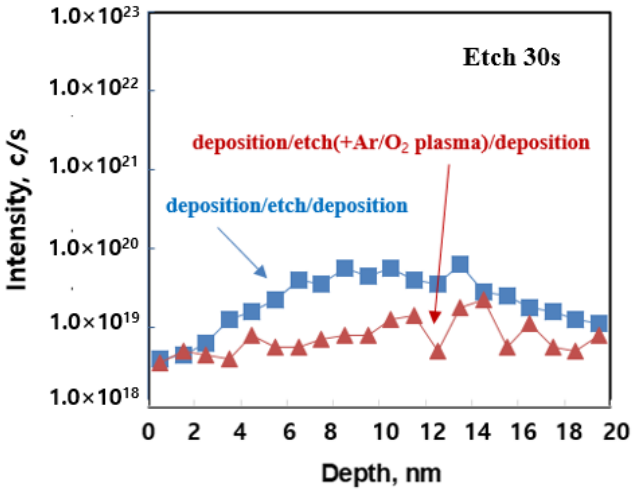

Figure 9. Fluorine concentration of thin film applied by the DED process (SIMS analysis).

2.2.4. Electrical Characteristics' Analysis of SiO_2 Thin Film Deposited by the DED Process

To investigate the electrical characteristics of the silicon oxide thin film deposited by the DED method, a MOSCAP (metal-oxide semiconductor capacitor) device was manufactured (Figure 10a). MIS (metal-insulator silicon) stack devices were manufactured through photo/etch and sputter TiN deposition and lift-off, and C-V and I-V characteristics were analyzed using a Cu bottom contact and probe station. Figure 10b shows the dielectric constant and breakdown voltage measurement results measured at a frequency of 1 MHz. The dielectric constant was obtained using the following Formula (3):

$$\text{Capacitance} = \text{area} \times (k \times \varepsilon_o / T_{ox}) \quad (3)$$

- area = 100 × 100 (μm^2)
- $\varepsilon_o = 8.8542 \times 10^{-12}$ F/m
- k = dielectric constant

Although the residual amount of fluorine generated from the etch step in the DED process is insignificant, dielectric constants were extracted and breakdown voltages were compared through C-V and I-V analysis to identify its impact during device manufacturing. The dielectric constant of the SiO_2 thin film deposited using the general method was 4.00 and the breakdown field was 11.89 MV/cm, whereas the dielectric constant of the SiO_2 thin film deposited by the DED method was 3.97 and the breakdown field was 11.41 MV/cm. The dielectric constant and breakdown field for both methods were at a similar level, confirming that the DED process did not affect the electrical properties of the films.

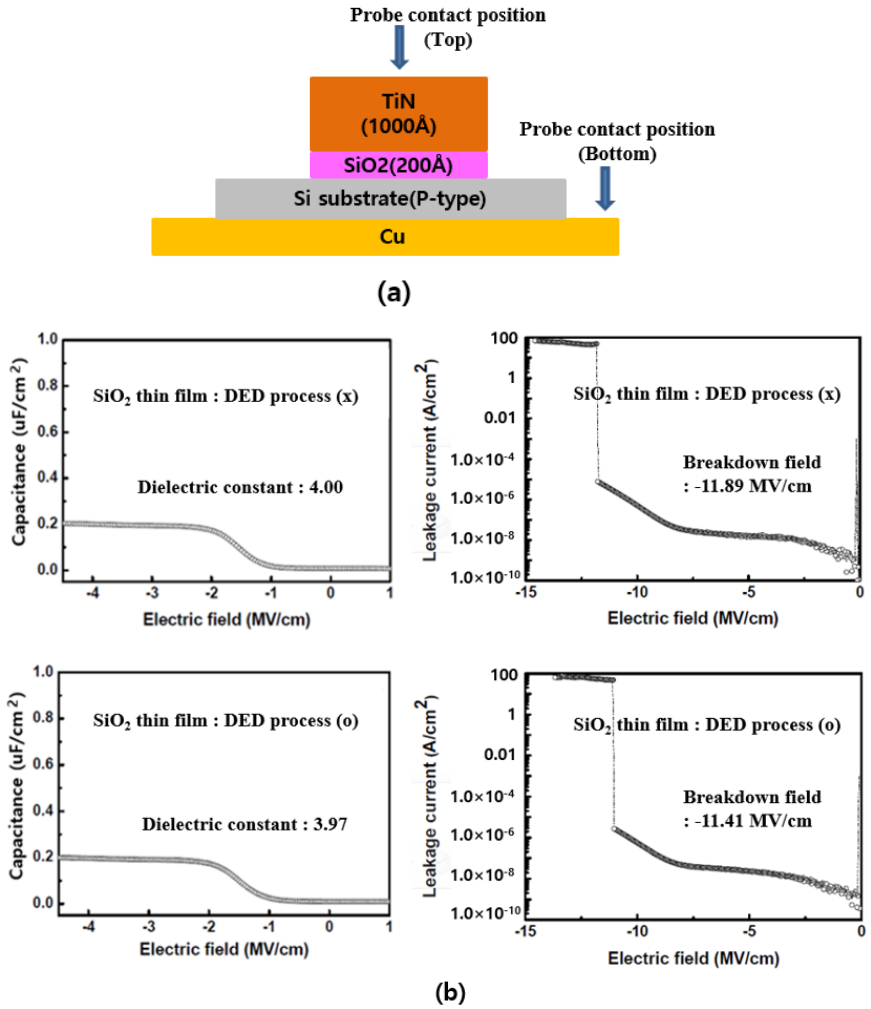

Figure 10. (**a**) Fabrication of a MOCAP device for C-V and I-V characterization and (**b**) dielectric constant and breakdown field of the deposited SiO_2 thin films.

2.3. Deposition/Etch/Deposition Process in the Pattern

2.3.1. Evaluation of Etch Influence in the Pattern

Figure 11 is a TEM analysis image of a silicon oxide thin film deposited on the pattern and etched after deposition. Figure 11a is an image deposited with 200 Å of silicon oxide. Figure 11b,c are TEM results analyzed by changing only the RF power to 500 and 700 w after fixing the etch time to 30 s, respectively. It can be seen that the etch rate increases when the RF power is increased from 500 to 700 w in the etch step. Additionally, it can be seen that the open area of the pattern top increases when the RF power is increased. The DED process can be used for the gap-fill process, in which the inside is a jar-shaped pattern. If the inside of the pattern is jar-shaped, even if the step coverage is adjusted, the top open area will close before gap-fill is completed [31,32]. Eventually, voids are formed inside the pattern and the quality of the film is deteriorated. The DED process prevents the pattern open area from closing before gap-filling by etching the pattern top open area in the middle of the process. At this time, by adjusting the RF power of the etch step, the open size of the pattern top area can be adjusted, so even if the aspect ratio of the pattern increases or the shape changes, the void-free gap-fill process can be performed.

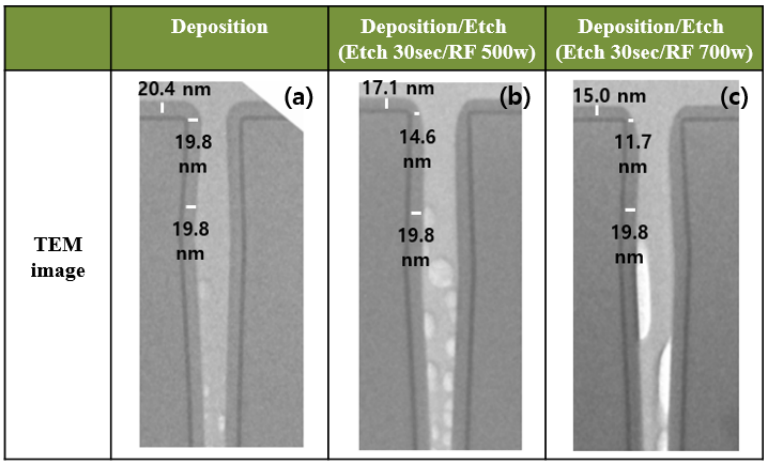

Figure 11. Analysis of the influence of etching in the pattern. (**a**) Pattern image when deposited only. (**b**) Pattern image when deposited by increasing RF power (500 w). (**c**) Pattern image when deposited by increasing RF power (700 w)

2.3.2. Gap-fill Evaluation in High Aspect Ratio Pattern

As semiconductor performance improves, the demand for a process to gap-fill high aspect ratio patterns is increasing [33–36]. In this study, the gap-fill process of the silicon oxide thin film was performed using the DED method using a 2400 nm depth and a CD 170 nm/60 nm pattern. In Figure 12a, the deposition/etch/deposition/etch/deposition 5-step DED method was applied by applying the etch step twice with an aspect ratio of a 14:1 pattern. If the CD size is large, it is difficult to secure a sufficient open area before gap-filling with the three-step DED method. Considering the CD size, the deposition thickness was divided into three parts to 600 Å, and an intermediate etch step was added twice. Etch time was 30 s, RF power was 700 w, and the NF_3 flow rate was 4000 sccm to complete the void-free gap-fill process. In Figure 12b, the deposition/etch/deposition 3-step DED method was used by applying one etch step with an aspect ratio of a 40:1 pattern. Considering the CD size of 600 nm, the deposition thickness was divided into two parts with 320 Å, and an intermediate etch step was performed once. Etch time was 30 s, RF power was 500 w, and the NF_3 flow rate was 4000 sccm. The process conditions of the etch step can be adjusted according to the pattern's shape, CD size, and depth.

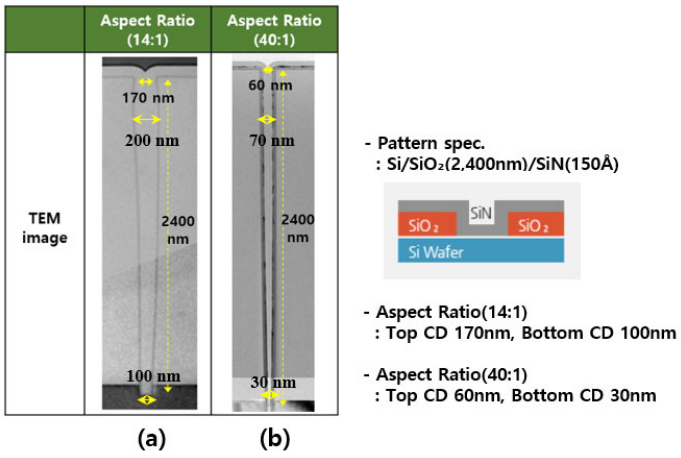

Figure 12. Gap-fill images of the silicon oxide thin film deposited by the DED method. (**a**) Aspect Ratio 14:1. (**b**) Aspect Ratio 40:1

3. Conclusions

In this study, a processing technology for depositing and gap-filling a SiO_2 thin film using the DED method was investigated. The gap-filling process was conducted by developing a space-divided PE-ALD facility, and a gap-filling process was developed to deposit void-free, insulating material in a trench pattern with an aspect ratio of 40:1 after confirming the basic characteristics of the DED process in a flat wafer. To reduce the in-film F concentration that may increase during the application of the DED process, an Ar/O_2 plasma treatment technology was developed, and the F concentration was reduced to 0.05%. An increase in the concentration of impurities such as F in films reduces various properties of the device. A MOCAP device was fabricated to identify potential reduction of electrical characteristics that may occur during the device manufacturing process. Under the DED application conditions, the dielectric constant and breakdown field of the fabricated thin film were 3.97 and 11.89 MV/cm, respectively, similar to the SiO_2 thin films deposited using the conventional method. Since the DED processing technology can be adjusted according to the shape, CD size, and depth of the pattern to be gap-filled, void-free gap-filling was achieved through RF power use and division of etch steps, even for patterns with a high aspect ratio. This study highlights the importance of applying appropriate solutions as the types of materials used and the required process development technologies are becoming increasingly diversified.

Author Contributions: Conceptualization, B.-J.L.; data curation, B.-J.L.; writing—review & editing, B.-J.L.; formal analysis, D.-W.S.; investigation, D.-W.S.; software, D.-W.S. and J.-W.C.; project administration, J.-W.C.**;** methodology, J.-W.C. All authors have read and agreed to the published version of the manuscript.

Funding: This study was conducted with Hanwha Corporation's own funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Trade secret.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Lee, B.; Hwang, J.; Seo, D.; Choi, J. Development of space divided PE-ALD system and process design for gap-fill process in advanced memory devices. *J. Korean Inst. Surf. Eng.* **2020**, *53*, 124–129.
2. Grillo, F.; Soethoudt, J.; Marques, E.A. Area-selective deposition of ruthenium by area-dependent surface diffusion. *Chem. Mat.* **2020**, *32*, 9560–9572.
3. Khan, R.; Shong, B.; Ko, B.G.; Lee, J.K.; Lee, H.; Park, J.Y.; Oh, I.-K.; Raya, S.S.; Hong, H.M.; Chung, K.-B.; et al. Area-selective atomic layer deposition using Si precursors as inhibitors. *Chem. Mater*. **2018**, *30*, 7603–7610.
4. Nam, T.; Lee, H.; Choi, T. Low-temperature, high-growth-rate ALD of SiO_2 using aminodisilane precursor. *Appl. Surf. Sci.* **2019**, *485*, 381–390.
5. Jeong, S.H.; Kim, J.K.; Kim, B.S.; Shim, S.H.; Lee, B.T. Characterization of SiO_2 and TiO_2 films prepared using rf magnetron sputtering and their application to anti-reflection coating. *Vacuum* **2004**, *76*, 507–515.
6. Gabriel, N.T.; Kim, S.S.; Talghader, J.J. Control of thermal deformation in dielectric mirrors using mechanical design and atomic layer deposition. *Opt. Lett*. **2009**, *34*, 1958–1960.
7. Lee, B.-J.; Seo, D.-W.; Choi, J.-W. Analysis of the influence of disk and wafer rotation speed on the SiO_2 thin-film characteristics in a space-divided PE-ALD system. *J. Korean Phys. Soc*. **2021**, *79*, 638–647.
8. Lee, B.; Seo, D.; Choi, J.-W. Effect of reactive gases (NH_3/N_2) on silicon–nitride thin films deposited with diiodosilane (SiH_2I_2) precursors. *JKPS*. **2022**, *80*, 311–319.
9. Sneh, O.; Wise, M.; Ott, A.; Okada, L.; George, S. Atomic layer growth of SiO_2 on Si(100) using $SiCl_4$ and H_2O in a binary reaction sequence. *Surf. Sci*. **1995**, *334*, 135–152.
10. Degai, M.; Kanomata, K.; Momiyama, K.; Kubota, S.; Hirahara, K.; Hirose, F. Non-heating atomic layer deposition of SiO_2 using tris(dimethylamino)silane and plasma-excited water vapor. *Thin Solid Film.* **2012**, *525*, 73–76.
11. Kamiyama, S.; Miura, T.; Nara, Y. Comparison between SiO_2 films deposited by atomic layer deposition with $SiH_2[N(CH_3)_2]_2$ and $SiH[N(CH_3)_2]_3$ precursors. *Thin Solid Film.* **2006**, *515*, 1517–1521.

12. Miikkulainen, V.; Leskela, M.; Ritala, M.; Puurunen, R.L. Crystallinity of inorganic films grown by atomic layer deposition: Overview and general trends. *J. Appl. Phys*. **2013**, *113*, 21301.
13. Burton, B.B.; Kang, S.W.; Rhee, S.W.; George, S.M. SiO_2 Atomic layer deposition using tris(dimethylamino)silane and hydrogen peroxide studied by in situ transmission FTIR spectroscopy. *J. Phys. Chem. C* **2009**, *113*, 8249–8257
14. Kobayashi, A.; Tsuji, N.; Fukazawa, A.; Kobayashi, N. Temperature dependence of SiO_2 film growth with plasma-enhanced atomic layer deposition. *Thin Solid Film.* **2012**, *520*, 3994–3998.
15. Dingemans, G.; van Helvoirt, C.A.A.; Pierreux, D.; Keuning, W.; Kessels, W.M.M. Plasma-assisted ALD for the conformal deposition of SiO_2: Process, material and electronic propertie. *J. Electrochem. Soc*. **2012**, *159*, 277–285.
16. Choi, J.S.; Yang, B.S.; Won, S.J.; Kim, J.R.; Suh, S.; Park, H.K.; Heo, J.; Kim, H.J. Low temperature formation of silicon oxide thin films by atomic layer deposition using NH_3/O_2-plasma. *Electrochem. Solid St*. **2013**, *2*, 114–116.
17. Putkonen, M.; Bosund, M.; Ylivaara, O.M.; Puurunen, R.L.; Kilpi, L.; Ronkainen, H.; Sintonen, S.; Ali, S.; Lipsanen, H.; Liu, X.; et al. Thermal and plasma enhanced atomic layer deposition of SiO_2 using commercial silicon precursors. *Thin Solid Film.* **2014**, *558*, 93–98.
18. Schmidt, J.; Merkle, A.; Brendel, R.; Hoex, B.; van de Sanden, M.C.M.; Kessels, W.M.M. Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited Al_2O_3 *Prog. Photovolt. Res. Appl*. **2008**, *16*, 461–466.
19. Ratzsch, S.; Kley, E.-B.; Tünnermann, A.; Szeghalmi, A. Inhibition of crystal growth during plasma enhanced atomic layer deposition by applying BIAS. *Materials* **2015**, *8*, 7805–7812.
20. Song, S.J.; Lee, S.W.; Kim, G.-H.; Seok, J.Y.; Yoon, K.J.; Yoon, J.H.; Hwang, C.S.; Gatineau, J.; Ko, C. Substrate dependent growth behaviors of plasma-enhanced atomic layer deposited nickel oxide films for resistive switching application. *Chem. Mater*. **2012**, *24*, 4675–4685.
21. Xie, J.; Yang, X.; Han, B.; Shao-Horn, Y.; Wang, D. Site-selective deposition of twinned Pt nanoparticles on $TiSi_2$ nanonets by atomic layer deposition and their oxygen reduction activities. *ACS Nano*. **2013**, *7*, 6337– 6345.
22. Lee, H.-B.; Baeck, S.H.; Jaramillo, T.F.; Bent, S.F. Growth of Pt nanowires by atomic layer deposition on highly ordered pyrolytic graphite. *Nano Lett*. **2013**, *13*, 457–463.
23. Chen, R.; Bent, S.F. Chemistry for positive pattern transfer using area-selective atomic layer deposition. *Adv. Mater*. **2006**, *18*, 1086–1090.
24. Watanabe, T.; Goto, N.; Yasuhisa, N.; Yanase, T.; Tanaka, T.; Shinozaki, S. Highly reliable trench capacitor with $SiO_2/Si_3N_4/SiO_2$ stacked film. In Proceedings of the 25th International Reliability Physics Symposium, San Diego, CA, USA, 7–9 April 1987; pp. 50–54.
25. Robertson, J.; Wallace, R. M. High-K materials and metal gates for CMOS applications. *Mater. Sci. Eng. R Rep*. **2015**, *88*, 1–41.
26. Endo, K.; Ishikawa, Y.; Matsukawa, T.; Liu, Y.; O'Uchi, S.-I.; Sakamoto, K.; Tsukada, J.; Yamauchi, H.; Masahara, M. Atomic layer deposition of SiO_2 for the performance enhancement of fin field effect transistors. *Jpn. J. Appl. Phys.* **2013**, 52. 116503.
27. Won, S.-J.; Suh, S.; Huh, M.S.; Kim, H.J. High-quality low-temperature silicon oxide by plasma-enhanced atomic layer deposition using a metal–organic silicon precursor and oxygen radical. *IEEE Electron Device Lett.* **2010**, *31*, 857–859.
28. Han, B.; Zhang, Q.; Wu, J.; Han, B.; Karwacki, E.J.; Derecskei, A.; Xiao, M.; Lei, X.; O'Neill, M.L.; Cheng, H. On the mechanisms of SiO_2 thin-film growth by the full atomic layer deposition process using bis(t-butylamino)silane on the hydroxylated SiO_2(001) Surface. *J. Phys. Chem. C* **2012**, *116*, 947–952.
29. Huang, L.; Han, B.; Han, B.; Derecskei-Kovacs, A.; Xiao, M.; Lei, X.; O'Neill, M.L.; Pearlstein, R.M.; Chandra, H.; Cheng, H. First-principles study of a full cycle of atomic layer deposition of SiO_2 thin films with di(sec-butylamino)silane and ozone. *J. Phys. Chem. C* **2013,** *117*, 19454–19463.
30. Jung, H.; Kim, W.-H.; Oh, I.-K.; Lee, C.-W.; Lansalot-Matras, C.; Lee, S.J.; Myoung, J.-M., Lee, H.-B.-R.; Kim, H. Growth characteristics and electrical properties of SiO_2 thin films prepared using plasma-enhanced atomic layer deposition and chemical vapor deposition with an aminosilane precursor. *J. Mater. Sci.* **2016**, *51*, 5082–5091.
31. Ahn, S.; Kim, Y.; Kang, S.; Im, K.; Lim, H. Low-temperature-atomic-layer-deposition of SiO_2 using various organic precursors. *J. Vac. Sci. Technol. A* **2017**, *35*, 01B131.
32. Choi, Y.-J.; Bae, S.-M.; Kim, J.-H.; Kim, E.-H.; Hwang, H.-S.; Park, J.-W.; Yang, H.; Choi, E.; Hwang, J.-H. Robust SiO_2 gate dielectric thin films prepared through plasma-enhanced atomic layer deposition involving di-sopropylamino silane (DIPAS) and oxygen plasma: Application to amorphous oxide thin film transistors. *Ceram. Int*. **2018**, *44*, 1556–1565.
33. O'Neill, M.L.; Bowen, H.R.; Derecskei-Kovacs, A.; Cuthill, K.S.; Han, B.; Xiao, M. Impact of aminosilane precursor structure on silicon oxides by atomic layer deposition. *Electrochem. Soc. Interface* **2011**, *20*, 33–37.
34. Kim, W.-H.; Oh, I.-K.; Kim, M.-K.; Maeng, W.J.; Lee, C.-W.; Lee, G.; Lansalot-Matras, C.; Noh, W.; Thompson, D.; Chu, D.; Kim, H. Atomic layer deposition of B_2O_3/SiO_2 thin films and their application in an efficient diffusion doping process. *J. Mater. Chem. C* **2014**, *2*, 5805–5811.

35. Ferguson, J.D.; Smith, E.R.; Weimer, A.W.; George, S.M. ALD of SiO_2 at room temperature using TEOS and H_2O with NH_3 as the Catalyst. *J. Electrochem. Soc.* **2004**, *151*, G528–G535.
36. Klaus, J.W.; Sneh, O.; George, S.M. Growth of SiO_2 at room temperature with the use of catalyzed sequential half-reactions. *Science* **1997**, *278*, 1934–1936.