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# Small-Signal Modeling and Analysis for a Wirelessly Distributed and Enabled Battery Energy Storage System of Electric Vehicles

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**Featured Application: The major object of this research is to provide a small-signal modeling method and controller design guidelines in wireless distributed and enabled battery energy storage system (WEDES) battery system for electric vehicles applications.**

**Abstract:** This paper presents small-signal modeling, analysis, and control design for wireless distributed and enabled battery energy storage system (WEDES) for electric vehicles (EVs), which can realize the active state-of-charge (SOC) balancing between each WEDES battery module and maintain operation with a regulated bus voltage. The derived small-signal models of the WEDES system consist of several sub-models, such as the DC-DC boost converter model, wireless power transfer model, and the models of control compensators. The small-signal models are able to provide deep insight analysis of the steady-state and dynamics of the WEDES battery system and provide design guidelines or criteria of the WEDES controller. The derived small-signal models and controller design are evaluated and validated by both MATLAB®/SIMULINK simulation and hardware experimental prototype.

## 1. Introduction

Battery energy storage systems (BESS) have been widely used in various applications, such as electric vehicles (EVs), consumer electronics, medical devices, smart grid, energy backup in data centers, and among others [1–10]. For EV applications, what is referred to be as "range anxiety" is one of the major reasons that prohibit or slows down the adoption of EVs [9–14].

To eliminate range anxiety in and extend the driving range of EVs, different methods have been discussed in the literature [9–17], such as increasing battery pack capacity, utilizing a faster charging method, utilizing a battery pack swapping method, achieving dynamic wireless charging, etc. While these methods can be effective to extend the driving range of EVs, some design challenges or drawbacks cannot be ignored.

When increasing capacity, the weight, size, and cost of the battery pack inevitably increase with the increase in battery capacity [10]. Further, the needed recharge time is also increased. For faster charging, the battery state-of-health (SOH) degrades at a higher rate if faster charging is applied [11,12]. In addition, the fast charger requires a high-power infrastructure that increases the cost of the overall system. For conventional battery swapping, specialized equipment, as well as the experienced personnel, are required to realize battery swapping [13]. For dynamic wireless charging, a large number of transmitter (Tx) coils are required with corresponding power supply units, which increases the infrastructure cost. In addition, this method might not be practical in all locations [14].

Among these methods, the battery swapping concept is a good candidate to reduce recharging time and extend the driving range with low infrastructure cost. To deal with the challenges in the conventional battery swapping concept, a new distributed and enabled battery energy storage (WEDES) system and WEDES controller for EVs are presented in [1], which allows for fast and safe exchange/swapping of smaller and lighter battery modules with wireless power transfer (WPT) technology [18,19].

An illustration of the WEDES system for EVs is shown in Figure 1b, and its example circuit diagram is shown in Figure 1c. Each of the battery modules consists of multiple battery cells, a dedicated electronics circuit, wireless power transmitter coil (Tx coil), wireless communication circuit, and client controller. While the on-board-unit (OBU) consists of a wireless power receiver coil (Rx coil), wireless communication circuit, and host controller. Different from the conventional battery swapping concept where the battery pack as a whole is exchanged at one time, in the WEDES battery system, the conventional single battery pack is divided into multiple small battery modules, which can deliver power through wireless power transfer (WPT) technology to the OBU. The distributed nature of the WEDES system combined with wireless power transfer (no physical connection between battery modules and OBU) makes the battery exchange/swapping easier, safer, and faster.

The distributed WEDES battery system with the WEDES controller addresses state-of-charge (SOC) balancing, bus voltage regulation, and battery module current/voltage regulation at the same time inside the system. Therefore, an SOC balancing control loop, a bus voltage regulation control loop, and a battery module current/voltage control loop are coupled with each other within one battery module as well as between multiple battery modules. These couplings make the analysis and design of the WEDES controller complex and critical. While the initial concept of the distributed WEDES battery system is discussed in [1], the small-signal modeling and controller design analysis are not focused on.

The main contributions of this paper can be summarized as follows:

(1). The overall review of the wireless distributed WEDES system, which allows for fast and safe exchange/swapping of battery modules when utilized in electric vehicles (EVs) applications to deal with the range anxiety issue.
(2). The derivation of small-signal modeling of the WEDES battery system to comprehensively analyze the steady-state stability and dynamic response of the WEDES battery system.
(3). The discussion of the guidelines for the controller design of multiple interacted control loops.
(4). The discussion of the simulation results and hardware experimental results to evaluate and validate the accuracy and effectiveness of the derived small-signal model and designed compensators.

The next Section discusses the detailed small-signal derivation of the WEDES system. Section 3 presents the design of compensators for each control loop. Simulation models and experimental results are presented and discussed in Section 4 to validate the derived small-signal models. Section 5 is the additional comments, and Section 6 concludes the paper.
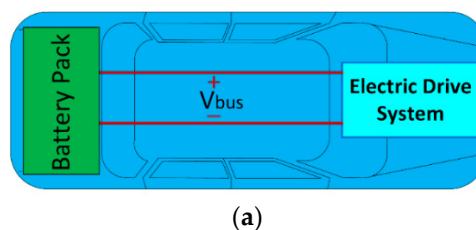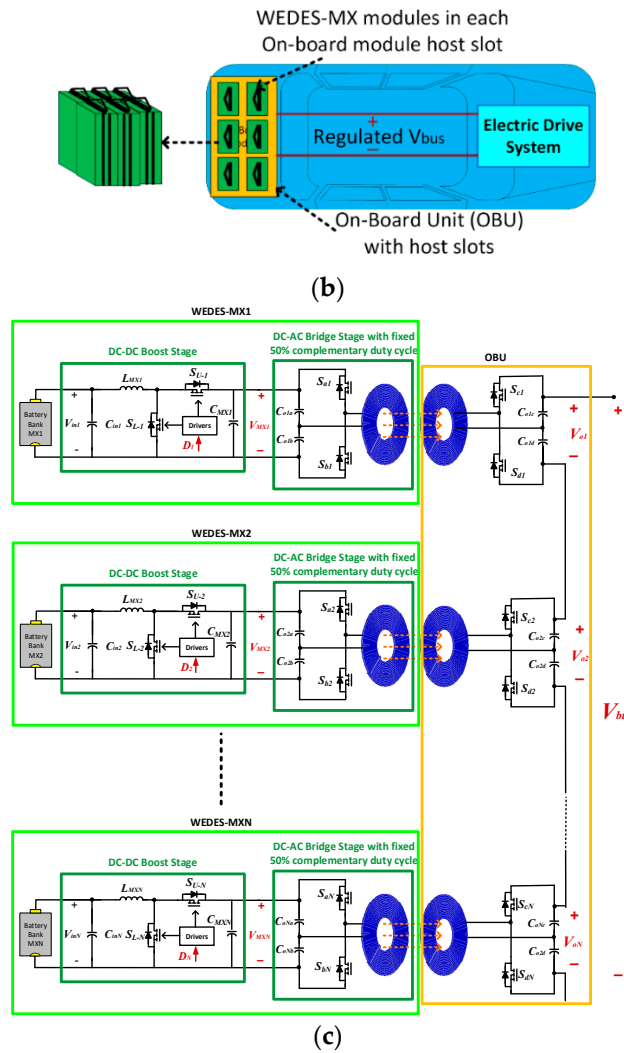


(a)

**Figure 1.** *Cont.*

(**b**)



(**c**)

**Figure 1.** Illustration diagrams of battery system for electric vehicle (EV) application. (**a**) The conventional battery pack and electrics drive system in EVs, (**b**) the wireless distributed and enabled battery energy storage (WEDES) battery system in EVs, and (**c**) example circuit diagram of the WEDES system [1].

## 2. Small-Signal Modeling of the Distributed WEDES System

### 2.1. Overview of the WEDES System and Controller Operation Principle

Figure 1c shows the illustration of an example circuit diagram of the WEDES system, which consists of two major parts: battery modules and on-board-unit (OBU).

Inside each battery module, multiple battery cells are connected in series and/or in parallel to form a battery bank, which can provide voltage/current/power to the rest of the system. The output of the battery bank is then connected to the input of a DC-DC power converter, which is used to achieve bus voltage regulation, battery module current/voltage regulation as well as SOC balancing at the same time as described later in this section. The output of the power converter is connected to an inverter stage for DC-AC power conversion. At the end of the battery module, the AC power from the inverter is applied to the transmitter (Tx) for inductive wireless power transfer (I-WPT) to the OBU.

The OBU mainly consists of receiver coils (Rx) followed by an AC-DC power conversion/rectification stage (rectifier). The outputs of each rectifier ($V_{o1}$ through $V_{oN}$) are connected in series to the bus/output ($V_{bus} = V_{o1} + V_{o2} + \ldots + V_{oN}$).

To realize the functionalities of SOC balancing, bus voltage regulation, and battery module current/voltage regulation, the WEDES controller consists of three different control loops: the SOC balancing control loop (referred to be by the SOC balancing loop), battery module voltage control loop (referred to be by the module voltage loop) and bus voltage control loop (referred to be by the bus voltage loop). Figure 2 shows the diagram of the wirelessly distributed WEDES controller, where $V_{\text{bus\_ref}}$ is the desired value of bus voltage, $V_{\text{MN-total}}$ is an intermediate value for voltage regulation, $C_{\text{\_re\_MX1}}$ though $C_{\text{\_re\_MXN}}$ are the remaining capacities of battery modules for SOC calculation, $SOC_{\text{MX1}}$ though $SOC_{\text{MXN}}$ are the SOC values of battery modules, $\lambda_{\text{DC1}}$ through $\lambda_{\text{DCN}}$ are weighting factors to generate the reference values of $V_{\text{MX1-DC-ref}}$ through $V_{\text{MXN-DC-ref}}$ for each battery module, $\alpha_{\text{MX1}}$ through $\alpha_{\text{MXN}}$ are the SOC multipliers and $\delta_{\text{MX1}}$ through $\delta_{\text{MXN}}$ are enable/disable values.
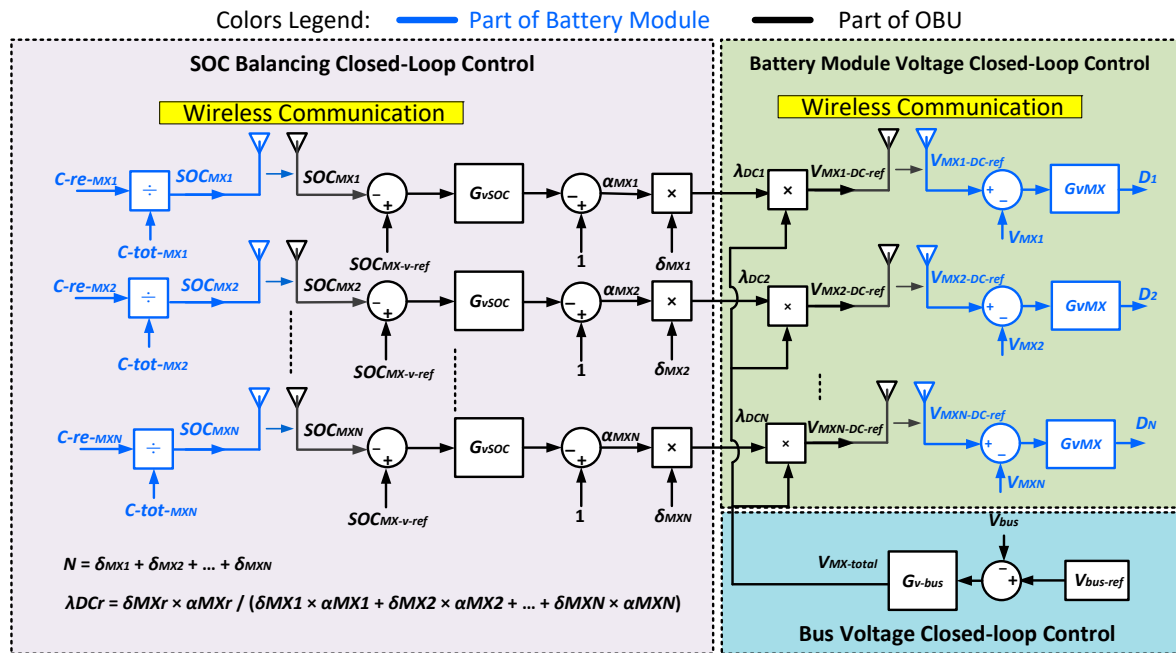


**Figure 2.** Illustration of the WEDES controller presented in [1].

In the WEDES controller, the SOC balancing loop is used to generate multipliers $\alpha_{\text{MX1}}$ through $\alpha_{\text{MXN}}$ to realize SOC balancing between multiple battery modules, as given by Equation (1).

$$\begin{cases} \alpha_{MX1} = (SOC_{MX-ref} - SOC_{MX1}) \times G_{vSOC} + 1 \\ \alpha_{MX2} = (SOC_{MX-ref} - SOC_{MX2}) \times G_{vSOC} + 1 \\ \qquad \dots\dots \\ \alpha_{MXN} = (SOC_{MX-ref} - SOC_{MXN}) \times G_{vSOC} + 1 \end{cases}, \tag{1}$$

where $SOC_{\text{MX-ref}}$ is the average SOC value of all battery modules, as given by Equation (2). When all battery modules are inserted and active, the sum of all $\delta_{\text{MX1}}$ through $\delta_{\text{MXN}}$ equals to $N$ ($\delta_{MX1} + \delta_{MX2} + \dots + \delta_{MXN} = N$).

$$SOC_{MX-ref} = \frac{(\delta_{MX1} \times SOC_{MX1}) + (\delta_{MX2} \times SOC_{MX2}) + \dots + (\delta_{MXN} \times SOC_{MXN})}{\delta_{MX1} + \delta_{MX2} + \dots + \delta_{MXN}}, \tag{2}$$

$$\lambda_{DCr} = \frac{\delta_{MXr} \times \alpha_{MXr}}{(\delta_{MX1} \times \alpha_{MX1}) + (\delta_{MX2} \times \alpha_{MX2}) + \dots + (\delta_{MXN} \times \alpha_{MXN})} \tag{3}$$

If the SOC value of $r$th battery module is larger than others, the corresponding multiplier $\alpha_{\text{MXr}}$ will be set larger, and vice versa. These multipliers $\alpha_{\text{MX1}}$ through $\alpha_{\text{MXN}}$ are then multiplied by

enabled/disable values $\delta_{MX1}$ through $\delta_{MXN}$ to further generate the weighting factors $\lambda_{DC1}$ through $\lambda_{DCN}$, as given by Equation (3). The sum of weighting factors $\lambda_{DC1}$ through $\lambda_{DCN}$ always equals to one. These weighting factors are then used in the battery module voltage loop to regulate the output voltage of the battery modules $V_{MX1}$ through $V_{MXN}$ at the primary side (Tx side), and as a result, achieve bus voltage regulation at the second side (Rx/OBU side).

It should be emphasized that due to the inevitable power loss during wireless power transfer (i.e., transmission efficiency is less than 100%), the bus voltage control loop is important to adaptively adjust $V_{MN\text{-total}}$ value to compensate the conversion ratios and losses of multiple power conversion stages (DC-AC-AC-DC) and realize bus voltage regulation. The relationship between different voltages can be calculated as given by Equation (4).

$$\begin{cases} V_{MX-total} = \left(V_{bus-ref} - V_{bus}\right) \times G_{v-bus} \\ V_{MX-total} = V_{MX1} + V_{MX2} + \ldots + V_{MXN} \\ \quad V_{MXr-DC-ref} = V_{MX-total} \times \lambda_{DCr} \\ \quad V_{bus} = V_{o1} + V_{o2} + \ldots + V_{oN} \end{cases} \tag{4}$$

To summarize, the presented WEDES controller can dynamically control SOC multipliers $\alpha_{MX1}$ through $\alpha_{MXN}$ to adjust the discharging rate for each battery module to achieve SOC balancing, while keeping $\lambda_{DC1} + \lambda_{DC2+} \ldots + \lambda_{DCN} = 1$ such that the bus voltage is always regulated as $V_{bus\text{-ref}}$.

## 2.2. Small-signal Modeling

Based on the block diagram of the WEDES controller shown in Figure 2, the small-signal of the distributed WEDES system with controller is shown in Figure 3. The transfer functions and symbols in Figure 3 are summarized as follows. For simplicity, the *r*th battery module is used for illustration.

$L_{bus}(s)$: Bus voltage control loop gain;

$L_{MXr}(s)$: Battery module voltage control loop gain;

$L_{SOCr}(s)$: SOC balancing control loop gain;

$G_{vdr}(s)$: Duty cycle to DC-DC converter output voltage $V_{MXN}$ transfer function;

$G_{idN}(s)$: Duty cycle to cell current transfer function;

$G_{socir}(s)$: Cell current to cell SOC transfer function;

$G_{iTR}(s)$: Gain of the input current of the half-bridge inverter to the output current of rectifier;

$G_{vTR}(s)$: Gain of the input voltage of the half-bridge inverter to the output voltage of rectifier;

$G_{PWM}$: PWM module gain;

$K_{divr}(s)$: Output voltage sensing gain (including voltage divider gain and ADC conversion gain);

$Delay_{wr}(s)$: Delay of wireless communication;

$Delay_{dr}(s)$: Delay of digital computation;

$ZOH_{vr}(s)$: Zero order hold model of voltage sampling;

$ZOH_{ir}(s)$: Zero order hold model of current sampling;

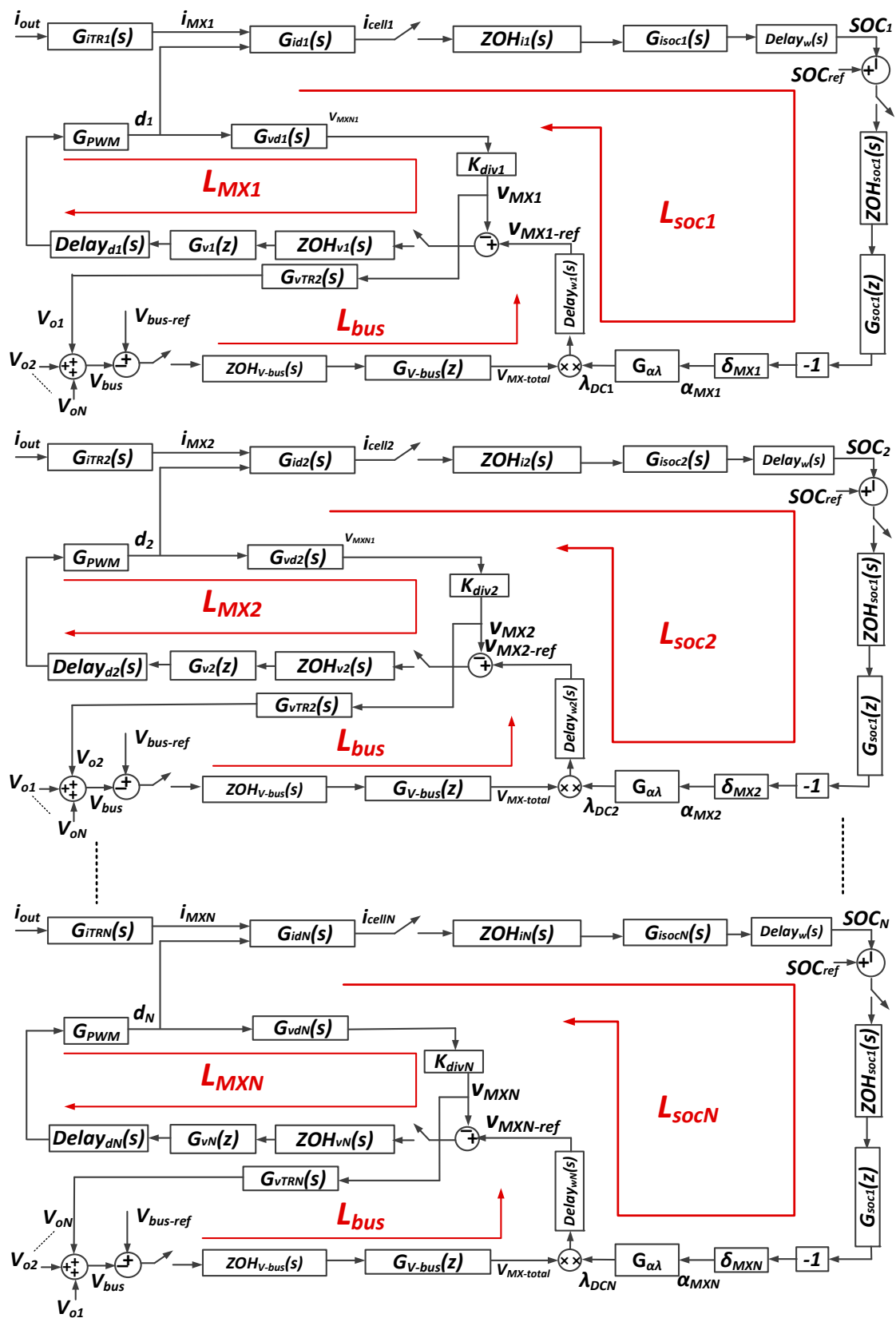$ZOH_{SOCr}(s)$: Zero order hold model of SOC sampling.

**Figure 3.** Small-signal of distributed the WEDES battery system with the WEDES controller.

### 2.3. Derivation of Transfer Functions

Since the design parameters and equilibrium operation point of all WEDES battery modules are the same under steady-state operation (when SOC balancing is achieved), the derivation of transfer functions of all battery modules follows the same procedure. The detailed derivation of $r$th battery module is discussed as follows:

### 2.3.1. Transfer Function of DC-DC Boost Stage

The circuit diagram of the DC-DC boost stage is shown in Figure 4. When the lower side switch $S_{L\text{-}r}$ is on and the upper side switch $S_{U\text{-}r}$ is off, the differential equation of the boost converter can be derived as follows:

$$\begin{cases} L_{MXr}\dfrac{di_{inr}}{dt} = v_{inr} \\ C_{MXr}\dfrac{dv_{MXr}}{dt} = -i_{MXr} \end{cases}, \tag{5}$$

where $i_{inr}$ and $v_{inr}$ are the input current and input voltage, respectively, and $i_{MXr}$ and $v_{MXr}$ are the output current and output voltage of the boost converter, respectively. $L_{MXr}$ is the inductor value, and $C_{MXr}$ is the output capacitor.
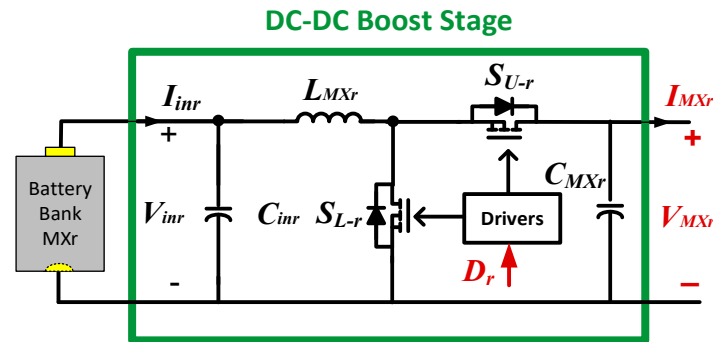


**Figure 4.** Circuit diagram of DC-DC boost stage in the WEDES system.

The state-space form of Equation (5) can be rewritten as Equation (6).

$$K\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = A_1\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + B_1\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}\begin{bmatrix} u_1 \\ u_2 \end{bmatrix}, \tag{6}$$

where the variables are $x_1 = i_{inr}$, $x_2 = v_{MXr}$, $u_1 = v_{inr}$, $u_2 = i_{MXr}$, respectively. $K = \begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}$.

Similarly, when the lower side switch $S_{L\text{-}r}$ is off and the upper side switch $S_{U\text{-}r}$ is on, the differential equation of the boost converter can be derived as follows:

$$\begin{cases} L_{MXr}\dfrac{di_{inr}}{dt} = V_{inr} - V_{MXr} \\ C_{MXr}\dfrac{dV_{MXr}}{dt} = i_{inr} - I_{MXr} \end{cases}. \tag{7}$$

The state-space form of Equation (7) can be rewritten as Equation (8).

$$K\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = A_2\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + B_2\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} 0 & -1 \\ -1 & 0 \end{bmatrix}\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & -1 \end{bmatrix}\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{8}$$

By using the state-space averaging method [20], the average matrix A and B are calculated as given by Equations (9) and (10).

$$A = A_1 D_r + A_2(1 - D_r), \tag{9}$$

$$B = B_1 D_r + B_2(1 - D_r), \tag{10}$$

where $D_r$ is the duty cycle of the boost converter.

The steady-state X is calculated as follows:

$$X = A^{-1}BU = \begin{bmatrix} \frac{I_{MXr}}{1-D_r} & V_{inr} \end{bmatrix}^{-1}. \tag{11}$$

The small-signal equation becomes as given by Equation (12):

$$\hat{X} = A\hat{x} + B\hat{u} + [(A_1 - A_2)X + (B_1 - B_2)U]\hat{d}_r, \tag{12}$$

where $A_1 - A_2 = \begin{bmatrix} 0 & 1 \\ -1 & 0 \end{bmatrix}$, $B_1 - B_2 = 0$, and $\hat{d}_r$ is the small signal variation of duty cycle around its steady state operation point.

Equation (12) can be rewritten as Equation (13):

$$\begin{cases} L_{MXr}\frac{d\hat{i_{inr}}}{dt} = -(1 - D_r)v_{MXr} + \hat{v_{inr}} + \frac{V_{inr}}{1-D_r}\hat{d}_r \\ C_{MXr}\frac{d\hat{V_{MXr}}}{dt} = (1 - D_r)\hat{i_{inr}} - \hat{i_{MXr}} - \frac{I_{MXr}}{1-D_r}\hat{d}_r \end{cases}. \tag{13}$$

To simply the analysis, the AC small-signal variation of $\hat{v_{inN}}$ and $\hat{i_{MXN}}$ is assumed to be 0 (negligible) because the dynamic variation of battery voltage and battery module output current is very slow compared to the dynamic variation of the control signal $\hat{d}_r$ (duty cycle) of the power converter. Therefore, by performing the Laplace transformation, Equation (14) can be derived as:

$$\begin{cases} sL_{MXr}i_{inr}(s) = -(1 - D_r)v_{MXr}(s) + \frac{V_{inr}}{1-D_r}d_r(s) \\ sC_{MXr}v_{MXr}(s) = (1 - D_r)i_{inr}(s) - \frac{I_{MXN}}{1-D_r}d_r(s) \end{cases}. \tag{14}$$

Based on Equation (15), the output voltage to the control signal transfer function of the power converter can be derived as

$$G_{vdr} = \frac{v_{MXr}(s)}{d_r(s)} = \frac{\frac{1}{C_{MXr}}\left(-\frac{I_{MXr}}{1-D_r}s + \frac{V_{inr}}{C_{MXr}}\right)}{s^2 + \frac{(1-D_r)^2}{L_{MXr}C_{MXr}}}. \tag{15}$$

Similarly, the input current to control signal transfer function can be derived as

$$G_{idr} = \frac{i_{inr}(s)}{d_r(s)} = \frac{\frac{1}{L_{MXr}}\left(\frac{I_{MXr}}{C_{MXr}} + \frac{V_{inr}}{1-D_r}s\right)}{s^2 + \frac{(1-D_r)^2}{L_{MXr}C_{MXr}}}. \tag{16}$$

### 2.3.2. Transfer Function of WPT Stage (Half-Bridge Inverter, WPT Coils, and Half-Bridge Rectifier)

Figure 5 shows the circuit diagram of the WPT stage. By writing the Kirchhoff's voltage law (KVL) equations as given by Equation (17), the ratio between the output voltage $V_{Rr}$ and the input voltage $V_{Tr}$ at the resonance frequency can be calculated as given by Equation (18).

$$\begin{bmatrix} j\omega L_{Tr} + \frac{1}{j\omega C_{Tr}} + R_{pTr} & -j\omega M_{TR} \\ -j\omega M_{TR} & j\omega L_{Rr} + \frac{1}{j\omega C_{Rr}} + R_{pTr} + R_{Lr} \end{bmatrix}\begin{bmatrix} I_{Tr} \\ I_{Rr} \end{bmatrix} = \begin{bmatrix} V_{Tr} \\ 0 \end{bmatrix}, \tag{17}$$

$$G_{vTRr}|_{\omega=\omega_o} = \frac{V_{Rr}}{V_{Tr}} = \frac{j\omega M_{TRr}R_{Lr}}{Z_{Tr}Z_{Rr} + (\omega M_{TR})^2} = \frac{j\omega k_{TRr}\sqrt{L_{Tr}L_{Rr}}R_{Lr}}{Z_{Tr}Z_{Rr} + (\omega k_{TRr})^2 L_{Tr}L_{Rr}}, \tag{18}$$

where $Z_{Tr} = j\omega L_{Tr} + \frac{1}{j\omega C_{Tr}} + R_{pTr}$ is the equivalent impedance of Tx side and $Z_{Rr} = j\omega L_{Rr} + \frac{1}{j\omega C_{Rr}} + R_{pTr} + R_{Lr}$ is the equivalent impedance of Tx side. By substituting $s = j\omega$ into Equation (19), the following transfer function can be obtained.

$$G_{vTRr}(s) = \frac{V_{Rr}(s)}{V_{Tr}(s)} = -\frac{sk_{TRr}\sqrt{L_{Tr}L_{Rr}}R_{Lr}}{Z_{Tr}Z_{Rr} + s^2k_{TRr}^2 L_{Tr}L_{Rr}}. \tag{19}$$
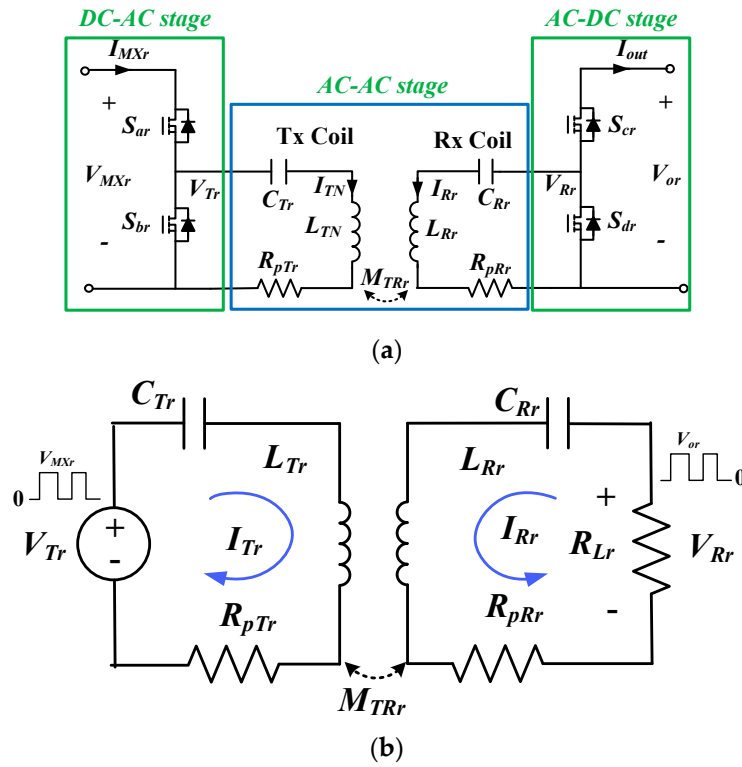


(a)



(b)

**Figure 5.** Circuit diagram of the wireless power transfer (WPT) stage in the WEDES system (**a**) equivalent circuit and (**b**) T-model.

Similarly, the ratio between the Tx current and Rx current can be derived as given by Equation (20).

$$G_{iTRr}(s) = \frac{I_{Rr}(s)}{I_{Tr}(s)} = -\frac{s^2 k_{TRr}C_{Rr}\sqrt{L_{Tr}L_{Rr}}}{s^2 L_{Rr}C_{Rr} + sC_{Rr}(R_{pTr} + R_{Lr}) + 1}. \tag{20}$$

## 3. Compensator Design

### 3.1. Battery Module Voltage Control Loop Compensator Design

The WEDES system design parameters are shown in Table 1. Based on the small-signal model in Figure 3, the uncompensated discrete-time transfer function of the battery module voltage loop for the $r^{\text{th}}$ battery module $G_{\text{bus}r}$ (Z) consists of $G_{\text{PWM}}$, $G_{\text{vd}r}$, $G_{\text{vTR}r}$, $k_{\text{div}r}$, $ZOH_{\text{vr}}$, and digital computation delay $Delay_{\text{dr}}$. $G_{\text{busN}}$ (Z) is calculated as given by Equation (21), and its bode plot is shown as the dashed curve in Figure 6.

$$L_{MXr_{uncomp}}(z) = Z\{G_{PWM}(s){\cdot}G_{vdr}(s){\cdot}G_{vTRr}(s){\cdot}ZOH_{vN}(s){\cdot}Delay_{dN}\} = \frac{-0.0001999z - 0.000272}{z^3 - 1.977z^2 + 0.9789z}, \tag{21}$$

where $ZOH_{vr}(s) = \frac{1-e^{-s \cdot T_s}}{s}$ ; $Delay_{dr}(s) = e^{-sT_{delay}}$ ; $T_{delay}$ is the digital controller computation delay and it is equal to 10 µs in the experimental implementation; $G_{PWM} = 1/1024$ ; $K_{div} = 11$ with 1 kΩ and 10 kΩ resistors as the voltage divider.

**Table 1.** Design parameters of the wireless distributed and enabled battery energy storage (WEDES) system.

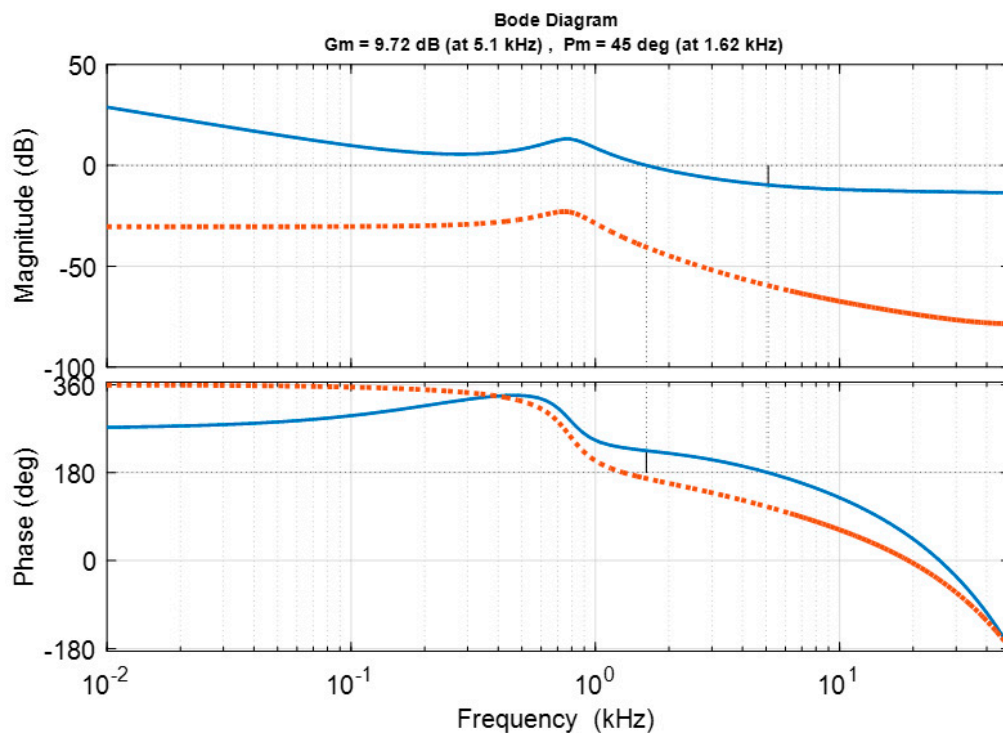| Parameter | Value | Parameter | Value |
|-----------|-------|-----------|-------|
| $V_{MXr}$ | 0–20 V | $L_T$, $L_R$ | 24 µH |
| $V_{bus\text{-}ref}$ | 30 V | $C_T$, $C_R$ | 0.4 µF |
| $I_{out}$ | 2 A | $k_{TR}$ | 0.3 |
| $L_{MXr}$ | 47 µH | $R_{pT}$, $R_{RT}$ @ 50 kHz | 0.1 Ω |
| $C_{MXr}$ | 220 µF | $f_{sw\_bridge}$ | 50 kHz |
| $f_{sw\_converter}$ | 100 kHz | - | - |



**Figure 6.** The bode plot of the uncompensated (red-dashed curve) and compensated (blue-solid curve) battery module voltage control loop gain.

In the battery module voltage compensator design, there is a right-hand-plane-zero (RHPZ), which is located at 4.86 kHz. This RHPZ is introduced due to the existing boost converter. To guarantee the stability of the system, the compensated control bandwidth should be smaller than RHPZ. With a compensator $G_{v\text{-}bus}(z)$ given by (22), the compensated battery module output voltage control loop gain ($G_{MXr\_comp} = G_{MXr\_uncomp}(z) \cdot G_{MXr}(z)$) achieves a control bandwidth of 1.62 kHz and a phase margin of 45°, as shown on the solid curve in Figure 6.

$$G_{MXr}(z) = \frac{950.8z^2 - 1850z + 899.7}{z^2 - z} \tag{22}$$

### 3.2. SOC Balancing Loop Compensator Design

According to the small-signal model shown in Figure 3, the uncompensated SOC loop gain (i.e., with unity SOC loop compensator gain) is given by Equation (23), and its bode plot is represented by the dashed curve in Figure 7.

$$L_{socr-uncomp}(z) = Z\{G_{idN}(s)\cdot ZOH_{icellN}(s)\cdot G_{sociN}(s)\cdot ZOH_{socN}(s)\cdot G_{socN}\cdot(-1)\cdot\delta_{MXN}\cdot G_{\alpha\lambda}\cdot Delay_w\cdot G_{v-bus}\}, \quad (23)$$

where $ZOH_{icellN}(s) = \frac{1-e^{-s\cdot T_s}}{s}$ , $ZOH_{socN}(s) = \frac{1-e^{-s\cdot T_{soc}}}{s}$, $T_{soc}$ is the sampling period for the SOC value in the SOC balancing loop. Since the SOC value of a battery cell varies very slowly compared to the switching period of the power converter, the sampling rate of the SOC balancing loop does not have to be very fast. $T_{soc}$ =1 s is found to be a good trade-off between the hardware resource consumption, system stability and SOC balancing speed.
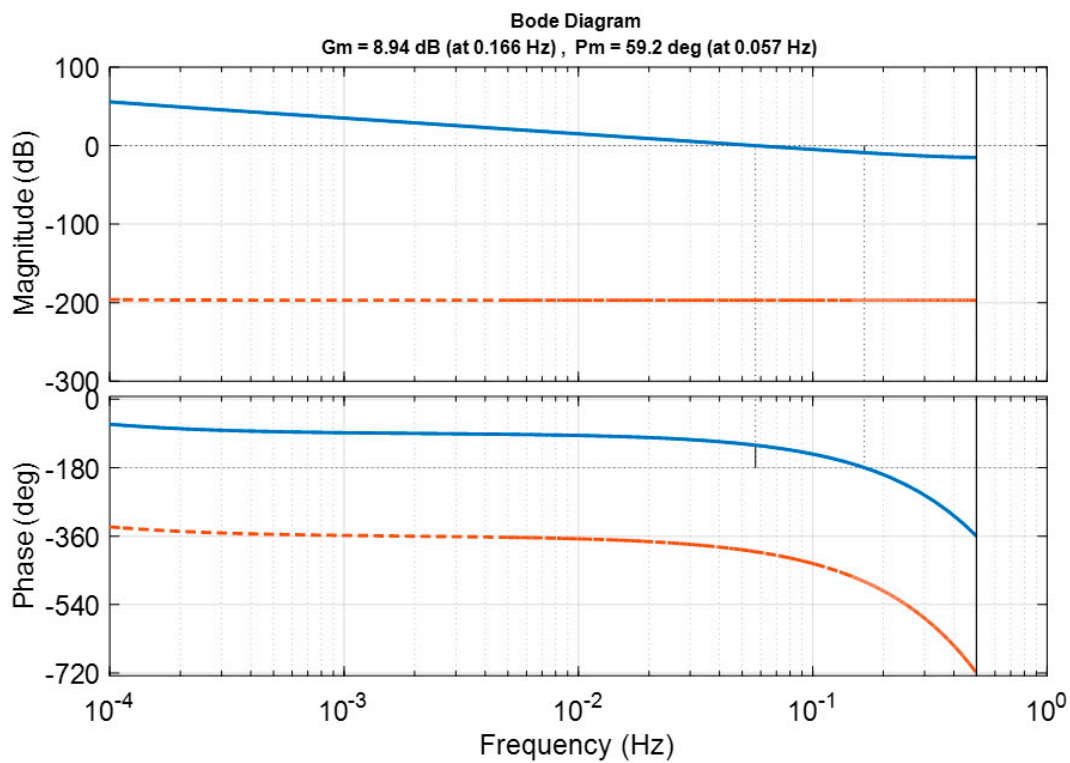


**Figure 7.** The bode plot of uncompensated (red-dashed curve) and compensated (blue-solid curve) SOC balancing control loop.

With a compensator given by Equation (24), the compensated SOC balancing loop gain achieves a control bandwidth of 0.057 Hz and phase margin of 59.2°, as shown on the solid curve in Figure 7. Due to the slow sampling rate of SOC value (1 Hz), it is expected that the control bandwidth of the SOC balancing loop is much lower than that of the voltage control loop.

$$G_{SOCr}(z) = \frac{2.5 \times 10^8}{z - 1} \quad (24)$$

### 3.3. Bus Voltage Control Loop Compensator Design

Based on the small-signal model shown in Figure 3, the uncompensated bus voltage control loop gain (i.e., with gain = 1) is given by Equation (25), and its bode plot is represented by the dashed curve in Figure 8. With a compensator given by Equation (26), the compensated bus voltage loop gain

achieves a control bandwidth of 8.12 kHz and a phase margin of 52.3°, as shown on the solid curve in Figure 8.

$$L_{bus-uncomp}(z) = Z\{ZOH_{v-bus}(s){\cdot}Delay_w\} = \frac{0.2555z - 0.1798}{z^2 - 1.977z + 0.9789}, \quad (25)$$

$$G_{bus}(z) = \frac{1.2z - 1.8}{z - 1}, \quad (26)$$

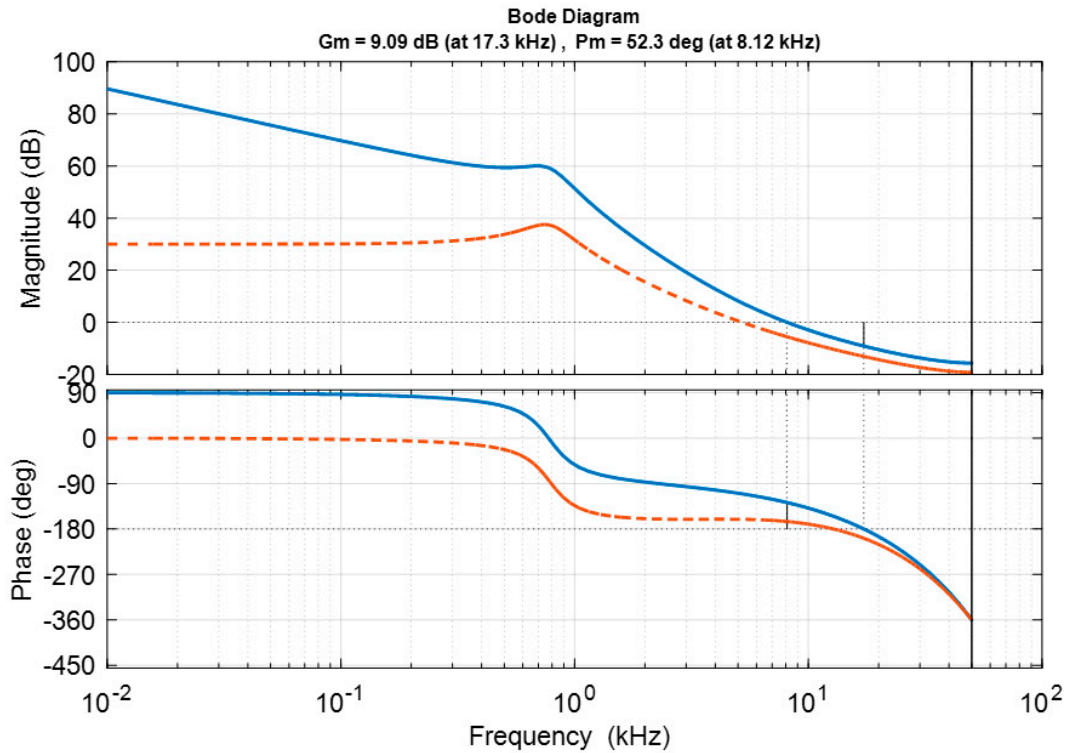where $ZOH_{v-bus}(s) = \frac{1-e^{-s{\cdot}T_s}}{s}$.



**Figure 8.** The bode plot of the uncompensated (red-dashed curve) and compensated (blue-solid curve) bus voltage control loop gain.

## 4. Simulation and Model Experiment Validation

In this section, the small-signal model was evaluated and validated in both simulation and hardware experiments. The simulation model was built in MATLAB®/SIMULINK software (2018a, MatchWorks, Natick, Massachusetts, USA) using the derived transfer functions in Sections 2 and 3. The hardware control compensator was implemented with Texas Instrumental microcontroller TMS320S28335. The design parameters are shown in Table 1. In the hardware experiment, three WEDES battery modules were implemented and utilized.

For the verification of derived small-signal models of the WEDES system, the dynamic response of both simulation and hardware experiments under different operation conditions was compared. If the dynamic performance from simulation results and experimental results are in good agreement, it can be implied that the developed model is valid.

As discussed in previous sections, there are three different control loops (battery module voltage control loop, bus voltage control loop, and SOC balancing control loop) in the WEDES system. During the test for a specific control loop, one of the operation parameters was changed while the rest of the operation parameters were set constant.

### 4.1. Experimental Results for Battery Module Voltage Control Loop

For the test of battery module voltage control loop, the reference output voltage for each battery module was changed suddenly from 10 V ($V_{MX1-DC-ref} = V_{MX2-DC-ref} = V_{MX3-DC-ref} = 10$ V under steady-state operation) to $V_{MX1-DC-ref} = 13$ V, $V_{MX2-DC-ref} = 9$ V and $V_{MX3-DC-ref} = 8$ V. The simulation results and experimental results are shown in Figure 9.
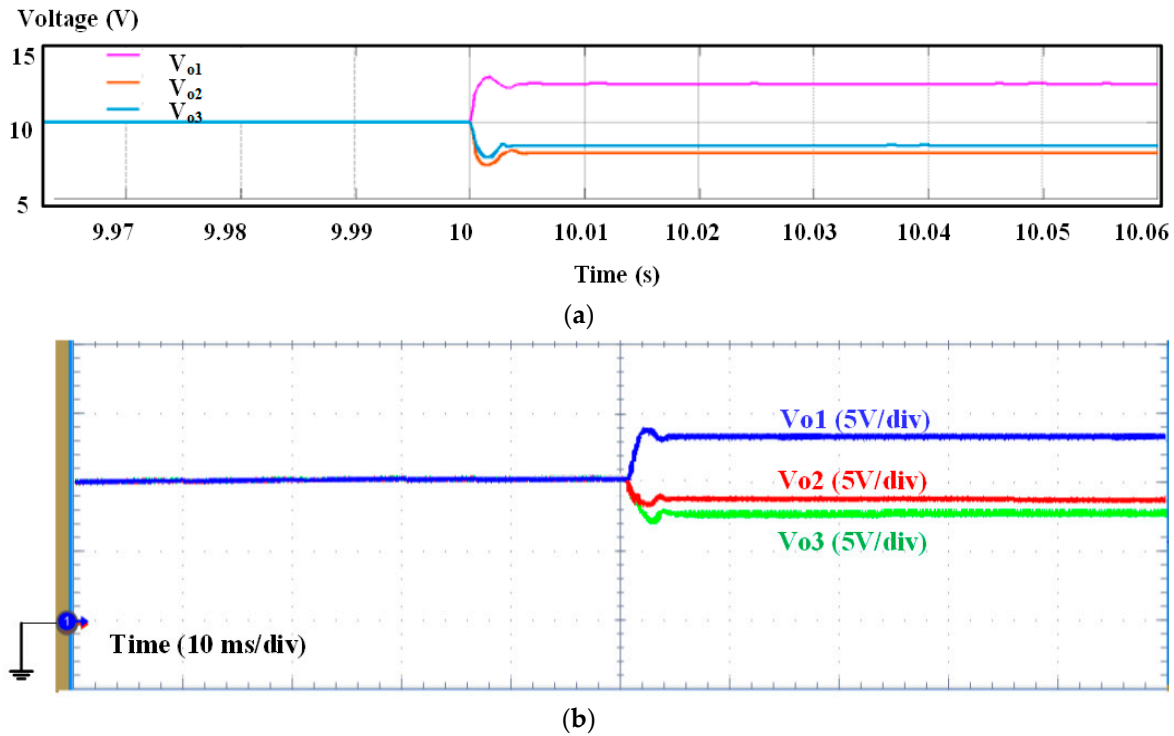


(a)



(b)

**Figure 9.** Waveforms for three battery module output voltage when the reference voltages were changed from $V_{MX1-DC-ref} = V_{MX2-DC-ref} = V_{MX3-DC-ref} = 10$ V to $V_{MX1-DC-ref} = 13$ V, $V_{MX2-DC-ref} = 9$ V and $V_{MX3-DC-ref} = 8$ V, (**a**) simulation results and (**b**) hardware experimental results.

From Figure 9, it can be observed that once the reference voltage values were changed, the output voltage of battery module 1 was controlled to increase while the output voltages of battery modules 2 and 3 were controlled to decrease. In Figure 9, the simulation model results and the hardware experimental results are in good agreement. In other words, the shape, magnitude, and overshoot/undershoot of the waveforms of simulation and hardware experiments match each other, which validates the small-signal model for the battery module voltage loop.

### 4.2. Experimental Results for SOC Balancing Control Loop

For the test of SOC balancing control loop, the SOC value of three battery modules were changed suddenly from $SOC_1 = SOC_2 = SOC_3 = 70\%$ under balanced conditions to $SOC_1 = 75\%$, $SOC_2 = 70\%$, and $SOC_3 = 65\%$. The experimental results are shown in Figure 10.

It can be observed from Figure 10 that once there was a change in SOC values, $V_{o1}$ increased while $V_{o3}$ decreased. This is because the value of $SOC_1$ was larger than the average SOC value of three battery modules (i.e., $(75\% + 70\% + 65\%)/3 = 70\%$), therefore resulted in a larger value of the battery module output voltage $V_{o1}$ for faster discharge. The variation of $V_{o3}$ for battery module 3 followed the same behavior but in the opposite direction. The value of $SOC_2$ was equal to the average SOC value, and therefore, its corresponding battery module output voltage remained constant. Figure 10 also shows that the simulation results and hardware experimental results are in good agreement under the variation of SOC values test condition.
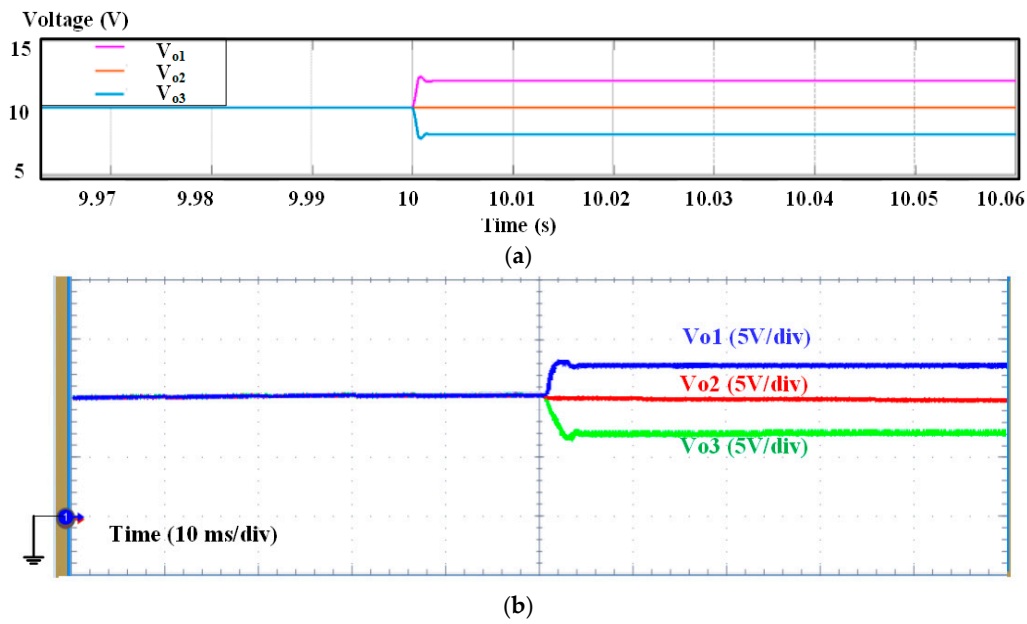
(a)



(b)

**Figure 10.** Waveforms for three battery module output voltage when SOC values of three modules changed from $SOC_1 = SOC_2 = SOC_3 = 70\%$ to $SOC_1 = 75\%$, $SOC_2 = 70\%$, and $SOC_3 = 65\%$, (**a**) simulation results and (**b**) hardware experimental results.

### 4.3. Experimental Results for Bus Voltage Control Loop

The last test was implemented for the bus voltage control loop. In this test, the bus voltage reference value was changed suddenly from 30 V to 37.5 V, as shown in Figure 11. It can be observed from Figure 11 that as the bus voltage reference value increased, the battery module voltage values changed from 10 V to 12.5 V correspondingly, which yielded a total bus voltage equal to its new reference value. The waveforms shown in Figure 11 demonstrate the consistency between simulation results and hardware experimental results.
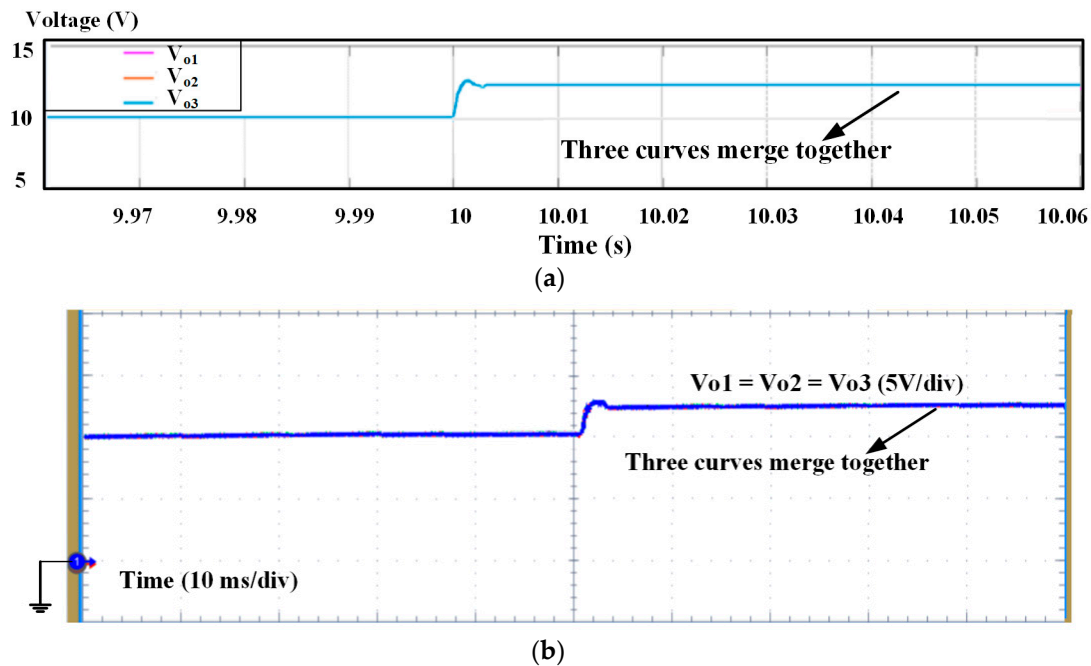


(a)



(b)

**Figure 11.** Waveforms for three battery module output voltage when bus reference voltage changes from $V_{bus-ref} = 30$ V to $V_{bus-ref} = 37.5$ V, (**a**) simulation results and (**b**) hardware experimental results.

## 5. Additional Comment

It should be noted that the presented WEDES system in this paper is different from a traditional Inductor-Capacitor (LC) compensation wireless power transfer (WPT) system or a traditional battery energy storage system (BESS). Instead, it is a combination of both systems. Table 2 shows a comparison between the presented WEDES system in this paper, conventional WPT system [18,21,22], and conventional BESS system [23–25]. It is shown that the presented WEDES system combines the advantages of both the conventional WPT system and BESS system, and can achieve bus voltage regulation and SOC balancing, and allow for fast and safe exchange/swapping of smaller and lighter battery modules with WPT technology.

**Table 2.** Comparison summary between the WEDES system, conventional Inductor-Capacitor (LC) compensation wireless power transfer (WPT) system, and conventional battery energy storage system (BESS).

| Parameter | WEDES System in this Paper | Conventional LC Compensation WPT System [18,21,22] | Conventional BESS System [23–25] |
|---|---|---|---|
| Typical Components/Devices | Battery cells, power converter, inverter, WPT coils, and rectifier | Battery cells, inverter, WPT coils, and rectifier | Battery cells and power converter/inverter |
| System Complexity | Medium | Medium | Low |
| Able to Realize SOC Balancing | Yes | No | Yes |
| Able to Realize Voltage Regulation | Yes | Yes | Yes |
| Typical Battery Operation | Discharging | Charging | Discharging |
| Able to Transfer Power Wirelessly | Yes | Yes | No |
| Able to Insert/Remove Battery Module during Normal Operation | Yes | No | No |
| Efficiency | High (>85%) | High (>90% at short distance) | Highest (>95%) |

## 6. Conclusions

In this paper, the small-signal modeling of a distributed WEDES battery system was derived to analyze the steady-state stability and dynamic response of the entire system, as well as provide guidelines for the controller design of multiple interacted control loops. Based on the small-signal models and associated transfer functions, all three control loops, including battery module output voltage control loop, SOC balancing control loop, and bus voltage control loop with compensators, were evaluated and validated by both simulations and a 3-module WEDES battery system. It was shown that the experimental results from simulation and hardware prototype were in good agreement, which validates the accuracy and effectiveness of the derived small-signal model and designed compensators.

**Conflicts of Interest:** The author declares no conflict of interest.

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