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A Manufacturing Method for High-Reliability Multilayer Flexible Electronics by Electrohydrodynamic Printing

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Abstract: To meet the demand for higher performance and wearability, integrated circuits are developing towards having multilayered structures and greater flexibility. However, traditional circuit fabrication methods using etching and lamination processes are not compatible with flexible substrates. As a non-contact printing method in additive manufacturing, electrohydrodynamic printing possesses advantages such as environmental friendliness, sub-micron manufacturing, and the capability for flexible substrates. However, the interconnection and insulation of different conductive layers become significant challenges. This study took composite silver ink as a conductive material to fabricate a circuit via electrohydrodynamic printing, applied polyimide spraying to achieve interlayer insulation, and drilled micro through-holes to achieve interlayer interconnection. A 200 × 200 mm^2 ten-layer flexible circuit was thus prepared. Furthermore, we combined a finite element simulation with reliability experiments, and the prepared ten-layer circuit was found to have excellent bending resistance and thermal cycling stability. This study provides a new method for the manufacturing of low-cost, large-sized, multilayer flexible circuits, which can improve circuit performance and boost the development of printed electronics.

Keywords: multilayer circuit; additive manufacturing; printing electronics; reliability

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1. Introduction

With the end of Moore's Law, integrated circuits have shifted from blindly pursuing an increase in integration to enhancing intelligence [1]. Intelligent electronics, including smart wearable devices, energy storage devices, sensors, and smart fabrics, are typically adhered to structures or biological surfaces to obtain more accurate sensing signals and enhanced wear comfort, which demands greater flexibility from these circuits [2–4]. Additionally, the superb conformal ability of flexible circuits allows them to adhere to the curved surfaces of three-dimensional objects without being limited by installation space. For example, conformal circuits can be applied to radar antennas on aircraft surfaces, structural health monitoring sensors, etc., significantly reducing equipment weight and enhancing aerodynamic performance [5–8]. However, traditional silicon-based circuit manufacturing methods, which utilize photolithography, etching, and other processes, are unsuitable for fabrication flexible substrates such as polyethylene terephthalate (PET) and polydimethylsiloxane (PDMS). Screen-printing technology is able to manufacture large-area conductive patterns on flexible substrates and is compatible with high-viscosity pastes, achieving superior conductivity. However, screen printing can only achieve a pattern resolution of at least a few hundred micrometers, thereby posing challenges for the fabrication of high-precision flexible circuits [9,10].

The advantages of inkjet printing as an additive manufacturing method are its high precision and environmental friendliness, and it is suitable for various substrates such as metals and flexible polymers [11–13]. Among the many inkjet printing methods, electrohydrodynamic (EHD) printing is compatible with various types of nanomaterials, and possesses the ability to prepare flexible electronics with an ultra-fine accuracy below 5 μm [14,15]. The principle of EHD printing is to apply a voltage between the nozzle and substrate, and the ink forms a Taylor cone under the action of the electric field that comes into contact with the substrate. At this time, the pathway conducts, the Taylor cone disappears, and then the circuit disconnects to generate a new Taylor cone [16]. During this cycle, the ink accumulates on the substrate with an ultra-fine resolution, and combined with a precision displacement platform, micro-scale patterns can be printed. Some researchers have prepared flexible heaters, supercapacitors, strain sensors, and other devices through EHD printing [14,17]. However, these circuits are almost all single-layer structures, which lead to larger volumes and weights compared to multilayer circuits with the same performance [18]. Multilayer circuits undoubtedly have more complex preparation processes; researchers use laser etching or photolithography to prepare flexible multilayer circuits, but these methods have high costs [19–21]. Therefore, it is necessary to develop a new multilayer circuit manufacturing method to achieve interlayer insulation and interconnection between multilayer circuits.

Bending stress is the most common working load in flexible electronics, which can lead to the cracking, delamination, and degradation of functional materials. Therefore, bending cycle tests are the most important indicator for evaluating the reliability of flexible electronics [22,23]. Especially for large multilayer circuits, their higher thickness leads to higher tensile/compressive stress at regions far from the neutral surface during bending, thereby increasing the risk of failure [24]. For circuits prepared via inkjet printing, it is difficult to ensure sufficient adhesion between the conductive layer and the insulation layer, and delamination may occur during the bending cycle process, which poses challenges to the selection of conductive ink and insulation layer materials. Given this research background, this study adopts a new flexible circuit fabrication method based on EHD printing, aiming to prepare large-area flexible multilayer electronics with excellent bending reliability. In order to make multilayer circuits more compatible with a wider range of usage scenarios, thermal cycling reliability is also considered.

2. Materials and Methods

2.1. Laboratory Experiment

The multilayer circuit manufacturing method developed in this study is shown in Figure 1. Firstly, the conductive path was printed onto a PET substrate via EHD, as shown in Figure 1a. The ink used for printing was WIK-36A high-conductivity composite silver ink from LOCTITE (Brussels, Belgium). Interlayer insulation was achieved by spraying insulated ink, as shown in Figure 1b. The insulated ink was obtained by mixing 5 mL of 20% polyimide (PI) solution with 15 mL of dimethylacetamide (DMAC) solution and stirring at 500 rpm for 0.5 h. The distance between the spray pen and the substrate was 20 mm, the spraying pressure was 0.1 MPa, and the time was 10 s per layer. After spraying the insulation layer, the PET substrate was transferred to a hot plate and dried at 80 °C for 5 min. Then, the initial operation was repeated for the next layer of conductive path printing. The method of interconnection between layers is shown in Figure 1c. We used a micro drilling bit to drill through-holes in the interconnection area and injected high-viscosity conductive paste into them. We designed ten-layer circuit patterns as shown in Figure 1d to verify the conductivity between each layer. Unconnected patterns were printed on the bottom layer, as shown in Figure S1 of the Supplementary Materials. We printed the square areas to serve as pads to drill through-holes for interlayer interconnection, and the circular areas served as pins to test connection status. By designing different conductive layer patterns, as shown in Figure S2, specific pins were connected, such as pin 1 and pin 2. When testing the resistance between different pins, the unconnected pins should be open circuit, while

the connected pins are conductive. Therefore, whether effective interlayer interconnection has been achieved can be determined by the open circuit or conductivity between the pins.

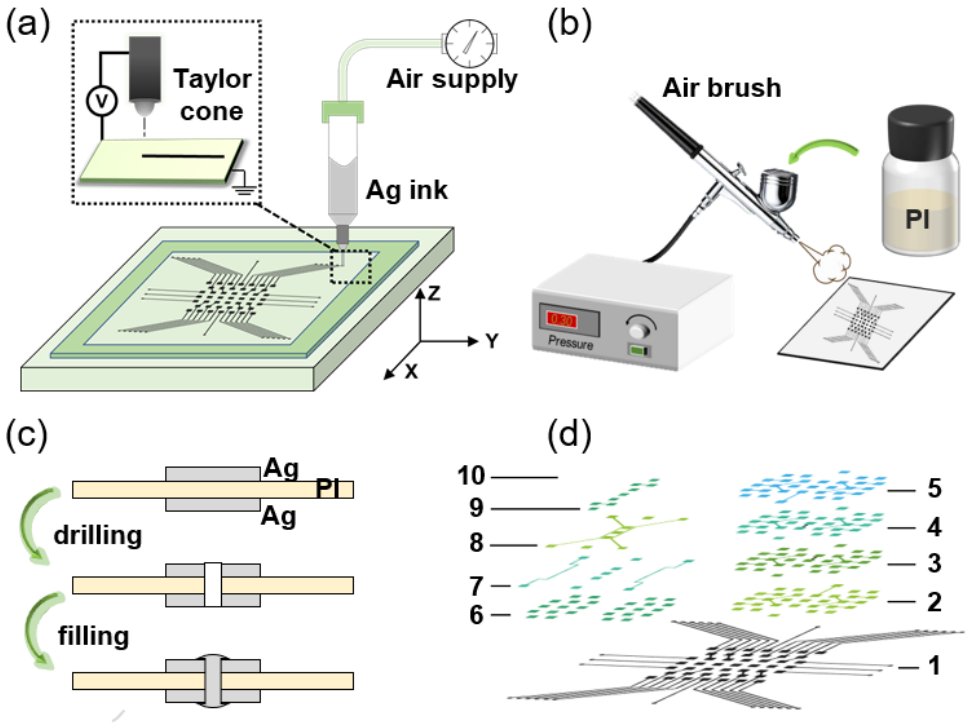

Figure 1. Schematic manufacturing process of multilayer flexible circuits: (**a**) electrohydrodynamic printing; (**b**) insulation; (**c**) interconnection; (**d**) conductive patterns of the 10-layer circuit.

In order to explore the process window of EHD printing, we conducted experiments at different printing speeds, nozzle heights, and nozzle diameters to determine the influence of various process parameters on printing quality. During the experiment, the electric field strength remained at 1.2×10^7 V/m. Furthermore, we investigated the sintering mechanism of conductive ink through post-treatment with heat.

We conducted bend cycling tests by using a self-developed testing platform with a bending angle of 120° and one bending cycle for 5 s. The thermal cycling test was conducted using a thermal cycling test chamber for a total of 1000 cycles. The thermal cycling profile was in accordance with the requirements of JESD22-A104: the temperature ranged from −55 °C to 85 °C, one cycle was held for 3000 s, with a rising time and falling time of 900 s and a cycle of 600 s at a consistent temperature. Five samples were prepared under each condition to exclude randomness. We measured the resistance between pin 1 and pin 2 (Figure S1) to evaluate the reliability of the multilayer circuit, because this conductive path was most affected by bending stress and passed through the most through-holes. Resistance and resistivity measurements were taken using four MCP-t370 probes by Mitsubishi Chemical (Tokyo, Japan). The microstructure and cross-section morphology of the multilayer flexible circuits were investigated using a scanning electron microscope (SEM, TESCAN CLARA, Brno, Czech), and the elemental composition was identified via energy dispersive spectrometry (EDS, TESCAN CLARA).

2.2. Numerical Simulation

In order to investigate the stress–strain distribution of multilayer circuits with different loads under thermal cycling and bend cycling, we conducted corresponding finite element analysis (FEA) simulation using ANSYS APDL (version 18.0). Several assumptions were made to ensure the accuracy and feasibility of the numerical simulation, as listed below:

- All materials were uniform and dense;
- All interconnecting interfaces were tightly combined;
- Thickness was constant in the same layer;
- Changes in a material's thermodynamic parameters with temperature were considered in the thermal cycling simulation.

The numerical simulation process is shown in Figure 2. The FEA model was established by APDL commands as shown in Figure 2a. Thermodynamic simulation used thermal element SOLID70 and structural element SOLID185. Tetrahedral elements were used for meshing, and the elements around the conductive parts were refined to improve the simulation accuracy, as shown in Figure 2b. The insulation layer between the conductive layers is very thin (within 2 μm), so we omitted the insulation layer between the conductive layers in the FEA modeling and used conductive blocks instead. The cross-section schematic diagram of the FEA model is shown in Figure S3. In the FEA of the bend cycling test, the displacement constraint was applied on either side of the plane, resulting in a bending angle of 120°. In the FEA of the thermal cycling test, simulation was conducted with the bending stress in order to fit the usage scenarios of conformal electronics. The thermal profile was consistent with the experiments, as shown in Figure 2c.

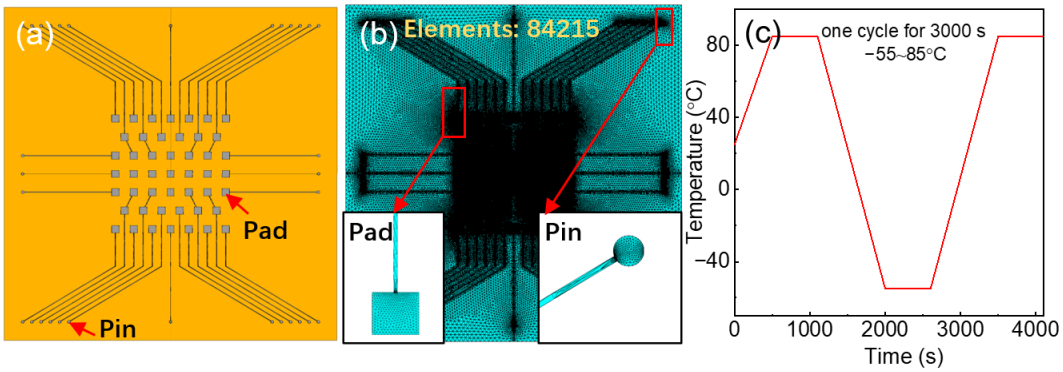

Figure 2. Pretreatment of finite element simulation: (**a**) FEA model; (**b**) mesh generation; (**c**) thermal cycling load files.

3. Results and Discussion

In high-precision printing, the line width is an important indicator for evaluating the printing effect. The width of the conductive path is also an important design parameter, as uncontrollable line widths would lead to short circuits between pins. Unlike traditional lithography processes, printing electronics cannot obtain specific line widths through masks, and the line widths acquired through printing have a strong process correlation. Therefore, it is necessary to clarify the rule of variation in line width through various process parameters to obtain conductive patterns with specific line widths. The influence of the printing speed, working height, and nozzle diameter of EHD printing on the line width is shown in Figure 3. As the printing speed increases, the line width gradually decreases, and the rate of change of the line width gradually decreases before stabilizing. The printing speed does not affect the diameter of the Taylor cone jet, but it does determine the amount of ink deposited per unit of time. A lower speed leads to greater ink deposition, and the wetting and spreading of the ink on the substrate increase the line width, as shown in Figure 3a. As the working height increases, the line width steadily increases due to the diffusion of the Taylor cone jet in the air, as shown in Figure 3b. When the working height approaches zero using high-speed printing, the line width becomes close to the diameter of the Taylor cone jet. The diameter of the nozzle directly determines the diameter of the Taylor cone jet. As the nozzle size increases, the line width steadily increases, as shown in Figure 3c. When the nozzle diameter is too large, it cannot produce a stable Taylor cone jet. Moreover, excessive printing speeds and working heights lead to discontinuous printing lines, resulting in large edge roughness of the printed lines. The diameter of the drill bit

used for drilling in this study is 150 μm. The drill bit damages the conductive path when the line width is too small. We purposefully selected a parameter combination based on the designed line width of 200 μm, so we used a 300 μm nozzle, a working height of 100 μm, and a printing speed of 0.5 m/s in the subsequent multilayer circuit preparation process; using these parameters, we were able to reliably obtain a 200 μm line path, as shown in Figure S4 of the Supplementary Materials. The deposition rate of the ink is also a key parameter, and we calculated the ink deposition rate of 1.2 mL/h.

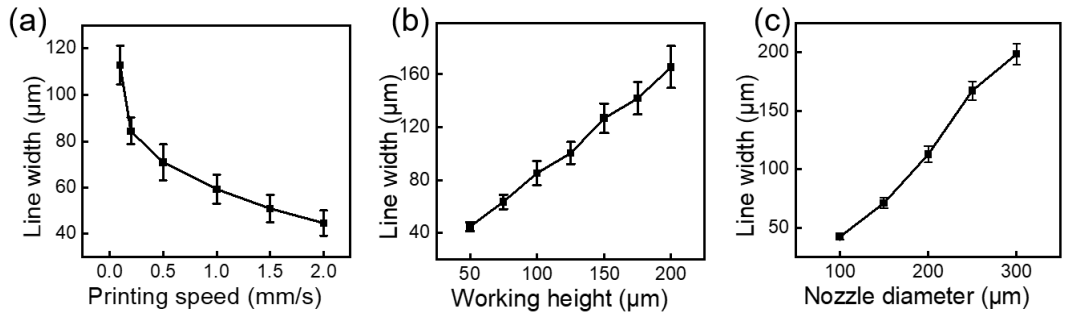

Figure 3. Printed line width under the influence of (**a**) printing speed, (**b**) working height, and (**c**) nozzle diameter.

Generally, metal nanoinks require post-treatment above 150 °C to exhibit good conductivity. However, the glass transition temperature of PET substrates is approximately 110 °C, so post-treatment needs to be carried out below 110 °C. In addition, we need to determine the conductivity mechanism, which is necessary to explain the increase in resistance during the bending cycles. The morphologies of the printed conductive path after 60 min of sintering at different temperatures are shown in Figure 4a–d; combined with the electrical resistivity results of Figure 4e, it can be seen that after post-treatment at temperatures below 150 °C, there was no significant change in the microstructure of the silver path, and micrometer sized silver nanoflakes were uniformly mixed as shown in Figure 4a–c. After sintering at 100 °C for 1 h, the resistance of the conductive circuit showed a significant decrease compared to the one without post-treatment, with a resistivity of 14.3 μΩ·cm. When the post-treatment temperature was raised to 150 °C, the resistance did not decrease further, indicating that the decrease in resistance caused the volatilization of organic solvents, which led to a decrease in the contact resistance between nanoflakes. However, at this time, these sliver nanoflakes were not sintered. When the temperature was raised to 300 °C, the resistance significantly decreased and quickly stabilized. The nanoflakes were sintered together due to the atomic diffusion at such a high temperature, which further reduced the resistivity, as shown in Figure 4d. In summary, sufficient conductivity could already be obtained at 100 °C via organic volatilization and the overlap between silver flakes, so we put the printed ten-layer circuit in a constant temperature box at 100 °C for 1 h.

Based on the process above, the ten-layer flexible circuits were prepared as shown in Figure 5. After testing the conductivity between different pins, effective interconnection was achieved between each layer. The unconnected pins were non-conductive, which proved that there was no short circuiting. The purpose of using a flexible substrate is to attach the circuit to a three-dimensional surface, so we attached the ten-layer circuits onto a wing-shaped resin substrate, as shown in Figure 5b,c. The resin block was fabricated using photocurable 3D printing, and the minimum curvature radius of the curved substrate was 20 mm. The flexible multilayered circuit showed an excellent conformal ability and tightly adhered to the curved substrate without delamination, proving that the multilayered circuit can adapt to complex curved surfaces.

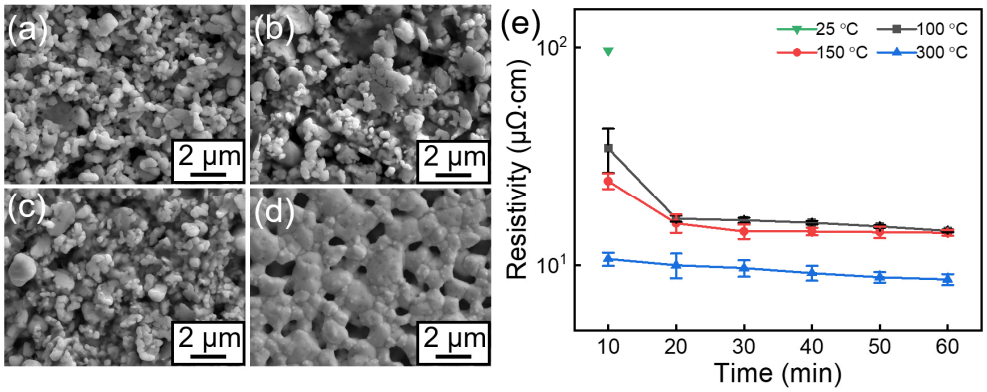

Figure 4. SEM images of the printed conductive path after 60 min sintering with the temperature of (**a**) 25 °C, (**b**) 100 °C, (**c**) 150 °C, and (**d**) 300 °C. (**e**) Variation curve of the electrical resistivity of conductive lines over time at different temperatures.

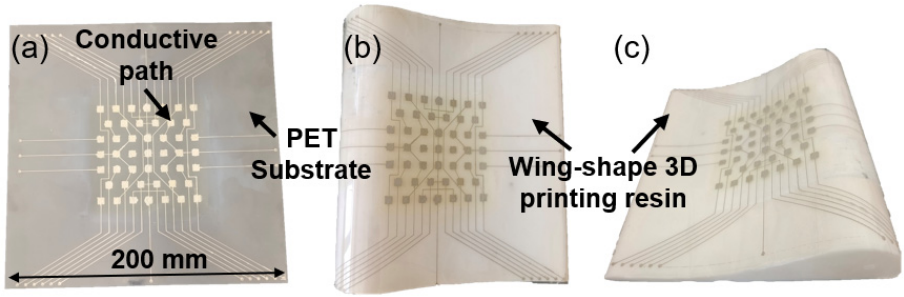

Figure 5. Optical images of (**a**) 10-layer flexible circuit and (**b**,**c**) conformal circuit.

Bending stress is the most common load on flexible circuits. To improve the bending reliability of the multilayered circuits, we established different conductive layer thicknesses in different areas in order to improve it. The part above the neutral plane bears the tensile stress during the bending process, while the part below the neutral plane bears the compressive stress. As mentioned in Figure 4, the good conductivity at a post-processing temperature of 100 °C is due to the overlap between the nanoflakes rather than a result of sintering. Compression stress will compress the nanoflakes to enhance conductivity. Therefore, the conductive layer can be printed thinner in the areas with higher compression stress. Conversely, tensile stress will loosen the nanoflakes, and an excessively thin conductive layer may result in an open circuit. Therefore, we made the conductive layer thicker in areas with higher tensile stress. We achieved a thicker conductive layer by increasing the number of prints, as shown in Figure 6a–c. We repeated printing twice for the area of the 10-layer circuit under compressive stress and obtained an average thickness of 5.6 μm. For the area under tensile stress, we repeated printing five times and obtained an average thickness of 26.5 μm, as shown in Figure 6d. A cross-section SEM image of a conductive through-hole is shown in Figure 6e. It can be seen that the conductive through-hole connected different conductive layers together. The interface between the conductive and insulating layers was tightly bonded without any delamination phenomenon, as shown in Figure 6f. EDS surface scanning was performed on the ten-layer circuit's cross-section, and the results are shown in Figure 6g–i. The main component of the conductive layer was Ag, and O and C elements were concentrated in the polyimide insulating layer, which separates the different conductive layers well and avoids the formation of short circuits. In addition, it can be found that there was no Ag in the insulating layer, but there was a low concentration of C and O elements in the conductive layer, which is due to the fact that we used a post-processing temperature of 100 °C and the organic compounds in the ink did not evaporate completely.

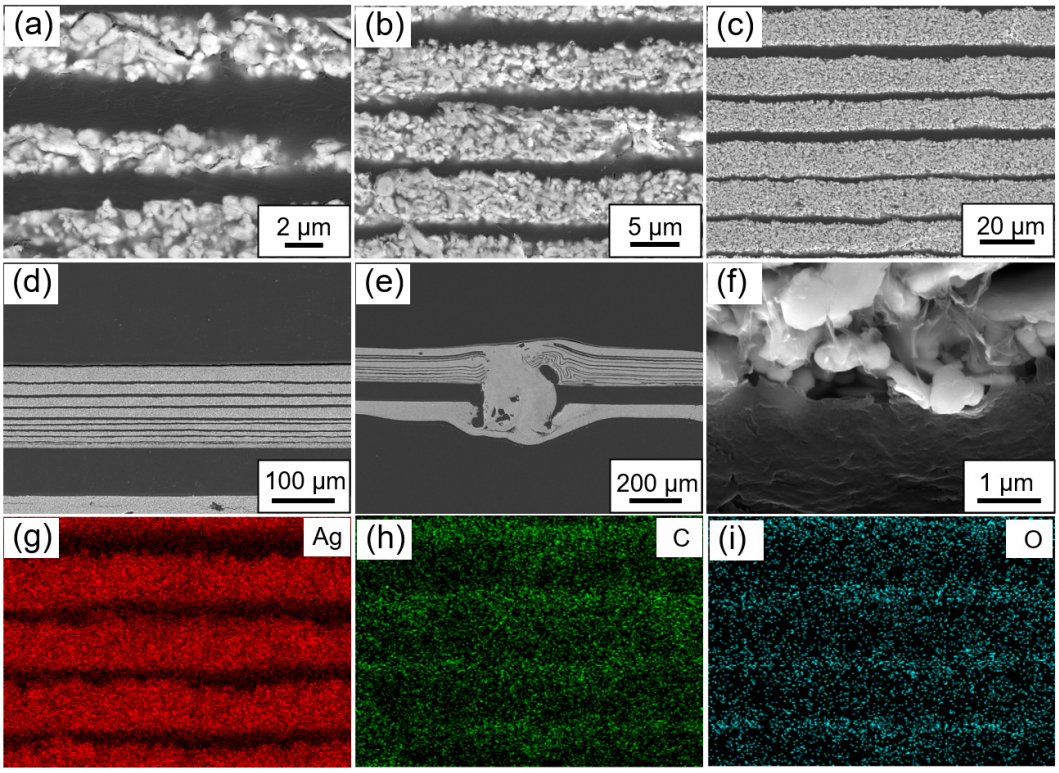

Figure 6. Cross-section SEM images of the different conductive layers thicknesses obtained via repeated printing (**a**) once, (**b**) twice, and (**c**) five times. Cross-section SEM images of (**d**) 10-layer flexible circuit, (**e**) conductive through-hole, and (**f**) interface between the conductive and insulating layers. EDS results of the 10-layer flexible circuit cross-section (**g**–**i**).

The curved substrates result in the flexible circuit undergoing bending stress for a long time. In order to verify the reliability of the flexible multilayer circuit under cyclic bending with a large curvature radius, a combination of simulations and experiments was carried out to explore the reliability and failure mechanism of the multilayer circuits. The displacement distribution and stress distribution are shown in Figure 7a,b, indicating that stress is concentrated in a small range of the bending center, only 0.55 MPa, due to the very small modulus of PET. A bend cycling test was conducted on flexible circuits to monitor the changes in resistance during the bending process, as shown in Figure 7c. The resistance exhibited periodic changes with increasing amplitude over the bending cycle. After 500 cycles, the resistance change rate was 7.9%, and after 8000 cycles, the resistance was approximately three times the initial resistance, demonstrating excellent bending reliability. Results of the microscopic morphology analysis of the circuit after 8000 bending cycles are shown in Figure 8. It can be seen that the microstructure on the surface of the circuit did not show obvious changes, but fine cracks appeared on the surface with a width of 1 μm. During the cyclic bending process, the maximum crack width was observed when the bending angle reached its maximum value and led to the maximum resistance. As the bending angle decreases, the nanoflakes around the cracks overlapped with each other, reducing the resistance and exhibiting periodic changes. Additionally, we found that, after the bend cycling experiment, the resistance of the circuit continued to slowly decrease. After 8000 bending cycles, the resistance was 2.6 times the initial resistance. However, the resistance decreased to 1.7 times the initial resistance after 10 h. This may be due to the effect of gravity, which makes the loose nanoflakes overlap in a tighter configuration.

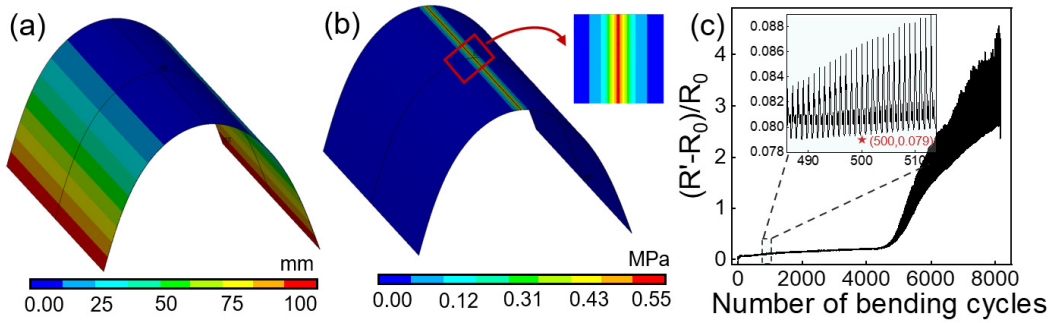

Figure 7. Bending reliability of the 10-layer flexible circuit: (**a**) displacement distribution obtained via FEA simulation; (**b**) von Mises stress distribution via FEA simulation; (**c**) resistance change rate during bending cycle test.

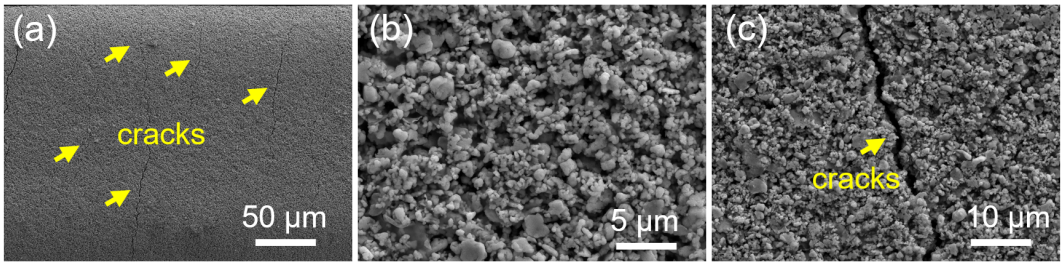

Figure 8. SEM morphology of the conductive pattern after 8000 bending cycles: (**a**) total area; (**b**) enlargement of the normal area; (**c**) enlargement of the crack area.

In order to make the multilayer circuit more compatible with a wider range of usage scenarios, the temperature cycling test environment was taken from −25 °C to 85 °C, and corresponding thermal cycling simulation was carried out. Conformal electronics experience both bending stress and thermal stress. Therefore, thermal–mechanical coupling simulations were carried out with bending prestress, and we applied the stress distribution obtained from bending simulation as a load, which can be used to explore the thermal cycling reliability of multilayer circuits under bending conditions. The temperature distribution at the moment of maximum temperature gradient during the heating process is shown in Figure 9a. The temperature distribution of the entire multilayer circuit was consistent, with a maximum temperature difference of only 0.13 °C. This is because the thickness of the multilayer circuit was only 0.2 mm, and the temperature quickly reached uniformity in a hot convection environment. The maximum stress during the thermal cycling process occurs at extremely low temperatures because the difference in the thermal expansion coefficient of the material is the greatest. Thermal stress is generated by mismatches in temperature, and the maximum stress point occurs at the junction of the silver line at the bending center and the PET, which was 6.8 MPa. It can be seen that the thermal stress generated by this multilayered circuit under thermal cycling load is extremely small. Due to the long testing time and the large amount of data required to detect changes in circuit resistance, multiple samples were tested simultaneously, and the initial resistance was measured as R_0. Samples were measure under 100, 200, 500, 800, and 1000 temperature cycles for resistance measurement, and the measured value was denoted as R'. The resistance change during thermal cycling is shown in Figure 9c. After 200 cycles, the resistance dropped to 95% of the initial resistance and remained unchanged. The initial slight decrease in resistance was because of the annealing effect in the high-temperature region, which further densified the conductive path. The experimental results were consistent with the simulation results, and the minimal thermal stress caused by thermal cycling did not cause a decrease in performance. Moreover, the resistance remained stable after 1000 thermal cycles.

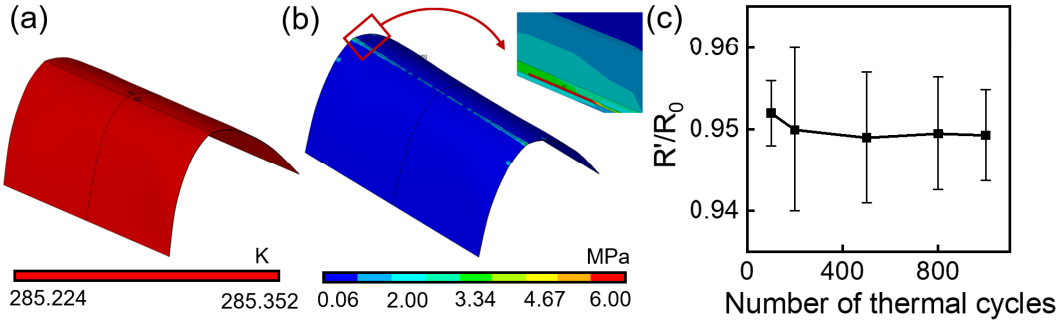

Figure 9. Thermal cycling reliability of the 10-layer flexible circuit. (**a**) Temperature distribution by FEA simulation. (**b**) Von Mises stress distribution by FEA simulation. (**c**) Resistance change rate during thermal cycling test.

4. Conclusions

This work proposed a large-area, low-cost, and highly reliable method for preparing multilayer flexible circuits. The advanced method of electrohydrodynamic printing was used to fabricate the conductive path, and the mechanisms by which various parameters influenced printing quality were explored in detail. Interlayer insulation was achieved by spraying PI layers and interconnection was achieved by micro vias. The resistivity of the silver conductive path after post-processing at 100 °C was only 14.3 μΩ·cm. The ten-layer flexible circuit has excellent bend cycling reliability and thermal cycling reliability. The failure mechanism under two cyclic loads was elucidated through a combination of numerical simulation and reliability testing. After 8000 bending cycles, the circuit resistance still met the high conductivity requirement, while the resistance only decreased by 5% after 1000 thermal cycles. The method proposed in this study has broad potential applications in the field of flexible devices, helping to accelerate the development of wearable electronics and conformal electronics.

Supplementary Materials: The following supporting information can be downloaded at: https://www.mdpi.com/article/10.3390/coatings14050625/s1.

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