

Article

A Parameter Optimization Design Method for Single-Phase Dual Active Bridge AC-DC Converter

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Abstract: The single-stage dual active bridge (DAB) AC-DC converter has the advantages of high power density, low cost, and simple control; it has a broad potential for application in the field of onboard chargers (OBC). However, the lack of fast and accurate quantitative parameter optimization design methods in single-stage DAB AC-DC converters limits the overall efficiency of the converter. Based on the above problem, in order to improve the overall operating efficiency of the converter by optimizing the parameter transformer ratio and power inductance, this paper proposes a parameter design method considering a multi-timescale strategy by combining the steady-state analysis model of the converter in the line cycle and switching cycle and step-by-step reducing its design space through the constraints on the parameters. The first step is to obtain a safe design space for the parameters under the converter's transmitted power and current stress constraints. The second step obtains the optimization design space of the parameters under the optimization of conduction loss and switching loss of the converter. Finally, the optimal parameters are determined by the loss analysis model. The proposed parameter optimization method entirely takes into account the steady-state characteristics of the DAB AC-DC converter during the line cycle, and the step-by-step constraints greatly accelerate the parameter design process. In addition, the proposed parameter optimization design method applies to all types of single-stage DAB AC-DC converters, which can be well applied to engineering practice.

Keywords: single-stage DAB AC-DC converter; parameter optimization design; multi-timescale analysis; safe design space; optimized design space



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1. Introduction

Single-stage dual active bridge (DAB) AC-DC converters have more potential in terms of efficiency, reliability, and power density due to the single-stage power conversion, which eliminates the use of large-capacity electrolytic capacitors on the DC bus [1–5]; instead, they have a promising future in the fields of on-board chargers, energy storage systems, and DC power distribution systems [6]. Numerous single-stage DAB AC-DC converter topologies have been proposed in existing research, and in particular, a totem pole-type DAB AC-DC converter is introduced in ref. [7], which employs a totem pole bridgeless rectifier structure on the AC side and multiplexes the high-frequency bridge arms in the rectifier with the primary-side bridge arms of the DAB converter. This further reduces switches and converter losses, giving it an advantage over single-stage DAB AC-DC converter topologies.

Due to the single-stage power conversion of the single-stage DAB AC-DC converter, the input voltage to the converter is a rectified sine wave, resulting in the converter usually operating over an extensive voltage gain range. Therefore, the research on single-stage DAB AC-DC converters mainly focuses on optimizing the modulation strategy to improve the converter's efficiency over an ultra-wide voltage gain range [8–10]. However, from the steady-state analysis model of the DAB converter, it can be seen that the steady-state performance of the converter is also affected by its circuit parameters. Therefore, it isn't easy to fully improve the converter's performance only through optimizing the modulation

strategy. Based on this, to realize the synchronous optimization by combining hardware and software to improve the overall efficiency of the converter further, this paper proposes a parameter optimization design method for the single-stage DAB AC-DC converter.

The parameter design method of the DAB converter has been studied in related literature. In ref. [11], the voltage gain of the converter with the highest operating efficiency is obtained by solving the problem under single phase-shift modulation by considering the actual operating condition of the DAB converter and the modulation strategy. Then the optimal design of the transformer ratio is obtained. However, this method only optimizes the transformer ratio without considering the optimal design of the power inductor. In ref. [12], the optimal parameters are obtained by iterative numerical computation based on the loss model, and the optimal design method can get the exact solution. However, due to the complexity of the loss model, the calculation time of the algorithm is long, and the optimization effect depends on the accuracy of the loss model, so it isn't easy to apply in engineering. In ref. [13], the discrete design strategy is used to optimize the parameters, but the method assumes that the transformer ratio is 1, so it does not have the generality. In ref. [14], a numerical method is used to obtain the optimal parameters by minimizing the inductor RMS current under the TPS modulation scheme. However, this method consumes a lot of time through numerical search. In ref. [15], an accurate frequency domain steady-state model of the DAB converter is developed, based on which the loss model of the converter is derived, and then the total loss is optimized by particle swarm optimization algorithm to obtain the optimal parameters.

The proposed parametric design methods mentioned above are based on the DAB DC-DC converter. Therefore, only the waveforms of a single switching cycle for a specific operating condition are considered in the design. For the DAB AC-DC converter, the operating waveforms of each switching cycle in the line cycle are inconsistent due to the frequency variations of the input voltage and the transferred power, and the operating waveforms of a single switching cycle cannot reflect the steady-state operation of the converter. More importantly, the above differences lead to a highly complex loss model for the DAB AC-DC converter, and it is difficult to establish the loss analysis model of the converter under a single switching cycle like the DAB DC-DC converter.

Therefore, compared with the existing design methods, this paper explores the parameter design method of the DAB AC-DC converter, concerning its multi-timescale steady-state operating characteristics for the first time. The proposed parameter design method combines the operating waveforms of the converter in the line cycle and switching cycle and seeks the optimization of transformer ratio and power inductance within the design space of the determined parameters to further improve the overall operating efficiency of the single-stage DAB AC-DC converter.

The rest of the paper is organized as follows. Section 2 presents the analysis of the multi-timescale steady state of the DAB AC-DC converter and the idea of a step-by-step design approach. A safe design space for the parameters is established from the constraints of output power and inductor current stresses in Section 3. In Section 4, an optimized design space for the parameters is established by exploring the effect of the parameters on the conduction loss and switching loss of the converter. In Section 5, the optimal parameter combinations are determined based on the converter loss analysis model. In Section 6, the scheme's effectiveness is verified by an experimental prototype. Finally, conclusions are drawn in Section 7.

2. Parameter Optimization Design Framework for DAB AC-DC Converter

2.1. Multi-Timescale Steady-State Analysis of the DAB AC-DC Converter

The topology of the totem pole type DAB AC-DC converter is shown in Figure 1. It consists of a totem pole bridgeless rectifier and a DAB DC-DC converter with a small HF filter capacitor C_c in the middle. Using the extended phase-shift (EPS) optimized modulation scheme proposed in ref. [16], the converter can be operated with guaranteed

open-loop PFC and minimum circulating currents over the entire operating range, which ensures the performance of the converter at the control level for the same set of parameters.

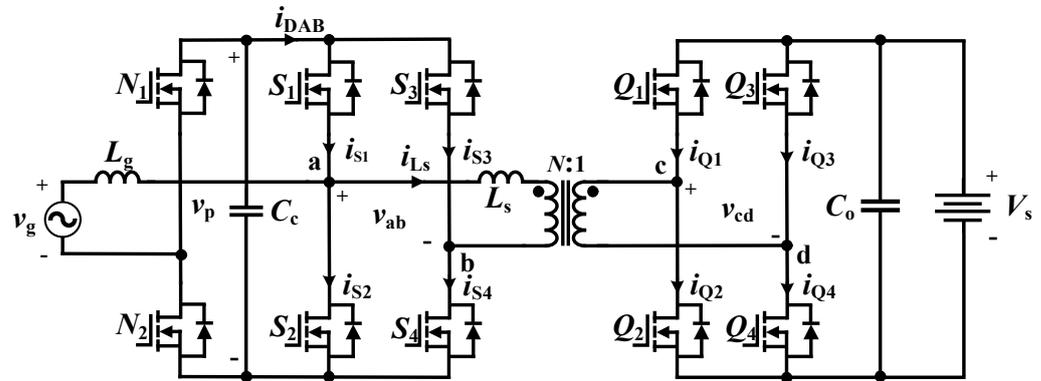


Figure 1. Totem pole DAB AC-DC converter topology.

The specifications of the converter designed in this paper are shown in Table 1; the RMS AC input voltage of the converter is 110 V, the output voltage $V_s = 360\sim 400$ V, the switching frequency $f_s = 100$ kHz, and the rated output power $P_N = 800$ W. The MOSFET is chosen to be Rohm’s SCT3060AL, which has a drain-source voltage of 650 V and a drain current of 39 A, and it can satisfy the requirements of the converter’s steady-state operation.

Table 1. DAB AC-DC converter design indicators.

Parameter	Value	Parameter	Value
Input Voltage v_g	110 Wrms	Output voltage V_s	360~400 V
Line frequency f_g	50 Hz	Switching frequency f_s	100 kHz
Rated power P_N	800 W	MOSFET	SCT3060AL

The expression for the inductor current in each switching cycle can be obtained from the time-domain steady-state analytical model of the DAB AC-DC converter under EPS modulation. However, the steady-state characteristics of the line cycle of the DAB AC-DC converter result in different steady-state waveforms of the converter in each switching cycle. Therefore, in analyzing the characteristic quantities such as the peak inductor current during the steady-state operation of the DAB AC-DC converter, the inductor current waveform can’t be considered only during a single switching cycle. The steady-state waveforms of the converter during line cycle T_g and switching cycle T_s under EPS modulation are shown in Figure 2. The inductor-current waveform of the m th switching cycle of the DAB converter is determined by the input voltage $V_p(m)$ and the transmitted power $p(m)$ at the moment, where $p(m)$ is:

$$p(m) = v_g(m)i_g(m) = V_p(m)i_{DAB}(m) \tag{1}$$

where v_g and i_g are the AC input voltage and current, and i_{DAB} is the average input current of the DAB converter. Since both $V_p(m)$ and $p(m)$ magnitudes vary with $T_g/2$, the peak inductor current, RMS value, and ZVS range for steady-state operation of the converter are analyzed over half a line cycle.

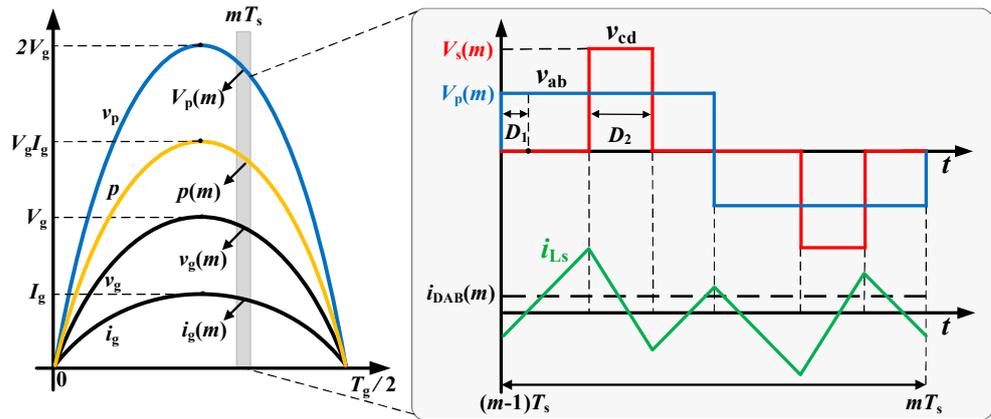


Figure 2. Steady-state waveforms of the converter under EPS at T_g and T_s .

In ref. [16], the expression for the peak-to-peak inductor current I_{pp} of the DAB converter under EPS modulation is:

$$I_{pp} = \frac{v_p(2D_1 - D_2) + NV_s D_2}{L_s f_s} \tag{2}$$

From Equation (2), the peak-to-peak inductor current I_{pp} for each switching cycle of the converter at operating condition ($V_s = 400$ V, $P = 800$ W) in $T_g/2$ with parameter $N = 1$ and $L_s = 50$ μ H can be calculated, as shown in Figure 3a. Similarly, the inductor current RMS I_{L_RMS} in each switching cycle can be obtained, as shown in Figure 3b.

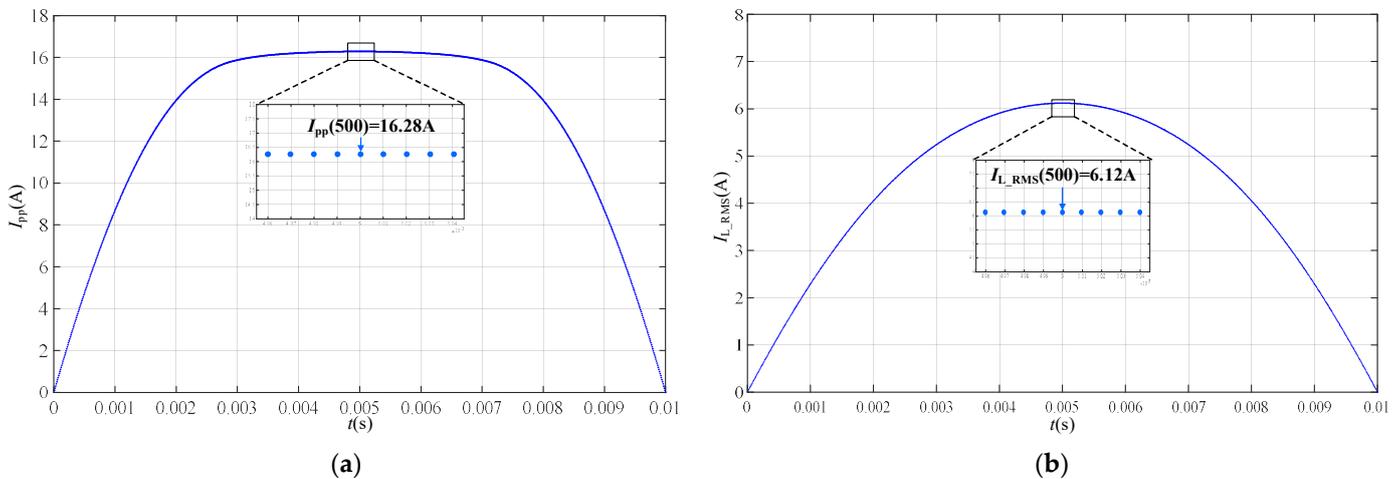


Figure 3. Steady-state waveforms of switching cycle in $T_g/2$ under the condition (400 V, 800 W): (a) the peak-to-peak inductor current I_{pp} ; (b) the inductor current RMS I_{L_RMS} .

From Figure 3, it can be seen that, for the single-stage DAB AC-DC converter, the I_{pp} and the I_{L_RMS} are varied by switching cycle. Under the operating condition (400 V, 800 W), the maximum peak inductor current occurs at the 500th switching cycle ($t = 0.005$ s), when $I_{pp}(500) = 16.28$ A and the $I_{L_RMS}(500) = 6.12$ A. Therefore, it cannot calculate the conduction loss of the converter for a specific operating condition based on the I_{L_RMS} for a single switching cycle.

The ZVS range of the DAB AC-DC converter switch is analyzed below. For the DAB AC-DC converter, it is necessary to analyze at least $(0.5T_g)/T_s = 1000$ switching cycles by considering that the input voltage and the transmitted power vary periodically within $T_g/2$, which results in different ZVS realizations of the converter at each switching cycle.

This complicates the determination of the range of ZVS realization during the steady-state operation of the DAB AC-DC converter.

The turn-on current of each switching tube in a totem pole DAB AC-DC converter with EPS modulation is calculated as follows:

$$\begin{cases} i_{S1} = i_{Ls}(t_0) - i_{Lg}(t_0) \\ i_{S2} = i_{Lg}(t_3) - i_{Ls}(t_3) \\ i_{S3} = -i_{Ls}(t_3) \\ i_{S4} = i_{Ls}(t_0) \end{cases} \quad \begin{cases} i_{Q1} = -Ni_{Ls}(t_1) \\ i_{Q2} = Ni_{Ls}(t_4) \\ i_{Q3} = Ni_{Ls}(t_2) \\ i_{Q4} = -Ni_{Ls}(t_5) \end{cases} \quad (3)$$

From the above equation, i_{S1} and i_{S2} depends on the current of inductor L_g and inductor L_s . And the current of inductor L_g is:

$$\begin{cases} i_{Lg}(t_0) = i_g + \frac{v_g}{4L_g f_s} \\ i_{Lg}(t_3) = i_g - \frac{v_g}{4L_g f_s} \end{cases} \quad (4)$$

And in the positive half-line cycle: $i_g > 0$; in the negative half-line cycle: $i_g < 0$, so the ZVS realizations of switch tubes S_1 and S_2 isn't identical.

Due to the symmetry of the inductor currents in the switching cycles under EPS modulation, the ZVS realizations of switch S_3 and S_4 , Q_1 and Q_2 , and Q_3 , and Q_4 are the same, so only the ZVS cases of switch S_1 , S_2 , S_4 , Q_2 , and Q_4 need to be analyzed. In this section, the turn-on moment current values of each switch of the converter at operating conditions (400 V,800 W) are solved for the parameters $N = 1$ and $L_s = 50 \mu\text{H}$, as shown in Figure 4.

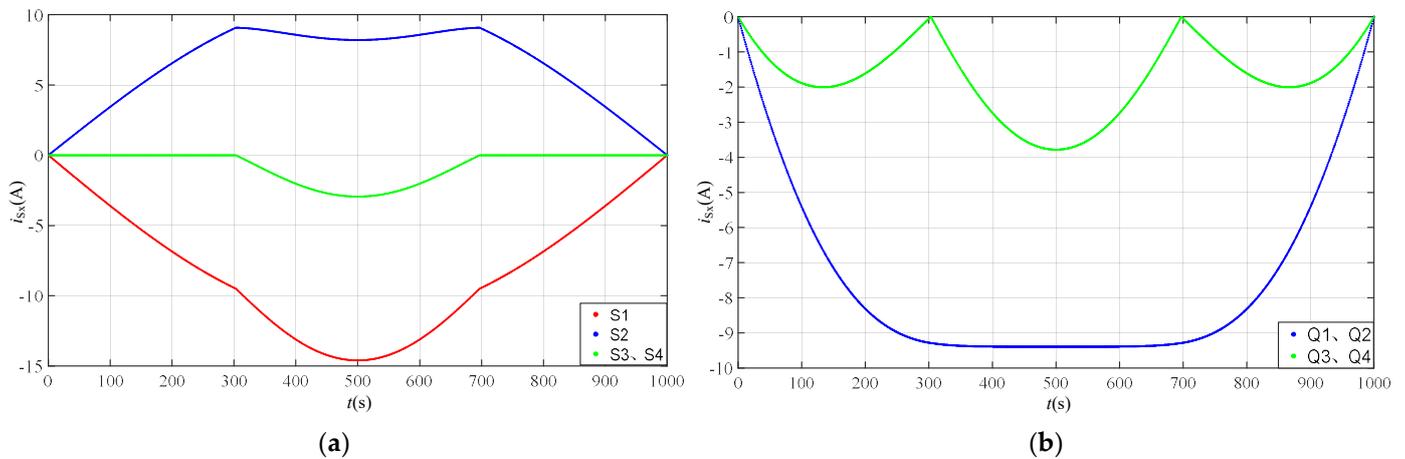


Figure 4. Current of each switching under the condition (400 V, 800 W) when $N = 1$, $L_s = 50 \mu\text{H}$: (a) Primary Switch $S_1 \sim S_4$; (b) Secondary Switch $Q_1 \sim Q_4$.

To simplify the ZVS analysis of the converter, it is considered that ZVS can be realized when the current of the switch at the turn-on moment is less than zero. As shown in Figure 4, the current at the opening moment of the switch S_1 and S_2 mainly depends on the AC current i_g , so in the positive half-line cycle: S_1 can realize ZVS and S_2 hard-switching, and in the negative half-line cycle: S_2 can realize ZVS and S_1 hard-switching. The secondary switch $Q_1 \sim Q_4$ can realize ZVS in the entire power region; the primary switch S_3 and S_4 can realize ZVS only in the high power region.

From the above analysis, the inductor current peak-to-peak I_{pp} , I_{RMS} , and ZVS ranges of the converter are obtained in the line cycle. This is essential for the subsequent determination of the parameter design space of the converter and the calculation of the converter losses.

2.2. Parameter Optimization Design Framework

When the control method of the converter is determined, the next step is to design the hardware parameters of a converter. For the parameter design of the DAB AC-DC converter, there are the following steps: (1) Determine the specifications of the converter according to the application scenario; (2) Establish the switching cycle steady-state analysis model of the DAB converter; (3) Calculate the steady-state eigenvalue of the converter under the determined modulation scheme; (4) Design and optimize the parameters of the circuit under the solved steady-state eigenvalue; (5) Test the prototype of the converter.

For the DAB converter, the parameters to be designed are the transformer ratio N and the power inductance L_s . In practical operating conditions, the following constraints are essential to protect the safety and high efficiency of the converter: (1) the constraint of the transmission power: the parameters of the circuit enable the converter to reach the maximum transmission power requirement; (2) the constraint of the current stress: the main circuit parameters obtained by designing the current peak in the full-load condition should be less than the maximum value that the power device can withstand. The design area that satisfies the above two conditions is the safe design space. In addition, we consider that the parameter design results affect the inductor current RMS and ZVS range of the converter, which correspond to the conduction loss and switching loss of the converter, respectively, and thus affect the converter's efficiency. Therefore, this paper explores the distribution of the RMS and ZVS ranges of the converter with different parameters N and L_s to narrow down the optimal parameter design region further, referred to as the optimal design space of the parameters.

In the following, each section is described in detail.

3. Safe Design Space for Parameters

3.1. Transmission Power Constraints

Ensuring that the parameters can guarantee the transferred power and voltage gain requirements of the converter is the first step in the parameter design. It allows a preliminary determination of the design region of the parameters to decrease the design space of parameters. From Table 1, the rated power of the converter is $P_N = 800$ W. And the maximum transmission power of the converter under EPS modulation is:

$$P_M = \frac{V_p N V_s}{8 f_s L_s} \quad (5)$$

Considering the 1/4 power margin for the converter design, it is required that the maximum transferred power of the converter is at least 5/4 of the rated power. Since the maximum value of the instantaneous transferred power of the AC-DC converter is twice the steady-state transferred power, the P_M should be not less than 5/2 of the rated power:

$$P_M = \frac{V_p N V_{s_min}}{8 f_s L_s} \geq \frac{5}{2} P_N \quad (6)$$

Substituting the prototype parameters into Equation (4), the constraints satisfied between N and L_s can be calculated with:

$$N \geq \frac{40 f_s L_s P_N}{2 V_p V_{s_min}} = \frac{40 \cdot 100000 \cdot 800}{2 \cdot 311 \cdot 360} \cdot 10^{-6} = \frac{1}{70} L_s \quad (7)$$

According to the constraint of the transferred power, the relationship between the transformer ratio N and the power inductance L_s can be derived. Next, the range of transformer ratio N is solved. For a DAB converter, it is illustrated in ref. [17] that the closer the voltage gain M tends to 1, the smaller the return power and loop current and the higher the power transfer efficiency, where the voltage gain $M = N V_s / V_p$. But for a single-stage DAB AC-DC converter, due to the input voltage V_p , the voltage gain M varies during the

line cycle and tends to infinity at the zero-crossing point of V_p . Therefore, it can only be constrained to the minimum value of voltage gain M_{\min} , and the range of M_{\min} is:

$$M_{\min} \in \left(\frac{NV_{s-\min}}{V_p}, \frac{NV_{s-\max}}{V_p} \right) = \left(\frac{360N}{311}, \frac{400N}{311} \right) \quad (8)$$

To ensure that the voltage gain M under EPS modulation is always greater than 1, it is necessary to ensure that $M_{\min} \geq 1$ and then get the lower limit of the transformer ratio N . Considering that a larger transformer ratio N will lead to a significant increase in the secondary current, it is set that $N < 3$. The range of the transformer ratio N is:

$$\frac{311}{360} \leq N \leq 3 \quad (9)$$

Therefore, the range of the transformer ratio N and power inductance L_s is constrained by Equations (5) and (7), and the range that satisfies the conditions can be obtained as shown in Figure 5. The yellow area in the figure is the effective range of the parameters N and L_s under the transmission power constraints, and within this range, the selected parameters are able to satisfy the requirements of the transmission power.

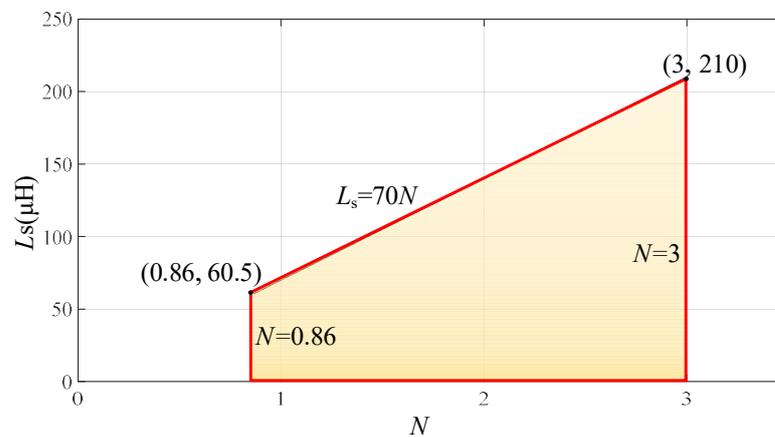


Figure 5. Range of values of N and L_s under transmission power constraint.

3.2. Current Stress Constraints

After determining the parameter range of the circuit under the transmission power constraint, the parameter design space under the current stress constraint needs to be considered. The current stress constraint ensures that the maximum current of the inductor is less than the maximum current that the switch can withstand. As shown in Figure 3a, the peak value of inductor current I_{pp} under specific operating conditions varies by switching cycle. Considering the two times margin of peak inductor current under EPS modulation, it is necessary to ensure that the maximum I_{pp} during the line cycle cannot exceed the current stress constraint.

Within the transmission power constraints shown in Figure 5, a set of randomly selected parameters $N = 1.5$ and $L_s = 40 \mu\text{H}$. The maximum inductor current peak-to-peak I_{pp} variation with the output power P versus the output voltage V_s can be obtained, as shown in Figure 6. The drain current of the selected switch SCT3060AL is 39 A. The I_{pp} allowed to flow in the whole power range of the switch on the secondary side is $39/1.5 = 26$ A when $N = 1.5$. Therefore, when I_{pp} exceeds 26 A, i.e., the red region, it can be considered that the current stress constraint is not satisfied under these parameters.

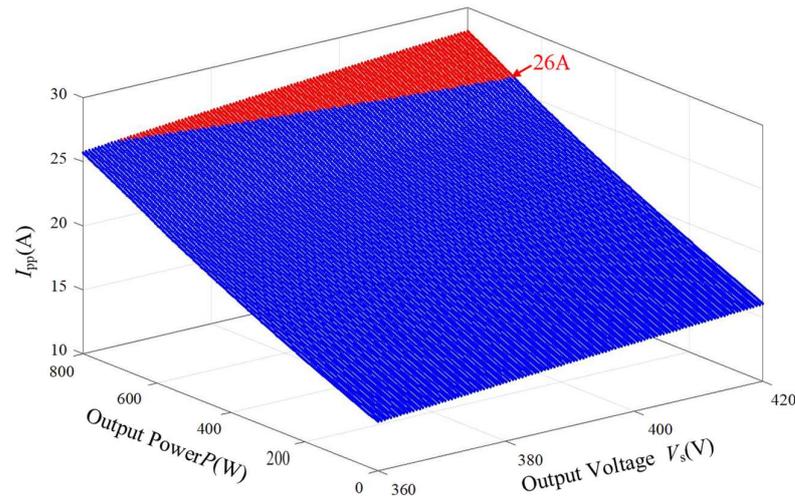
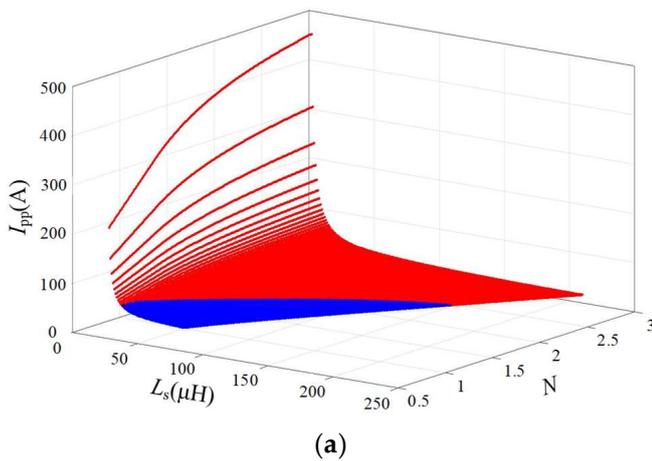


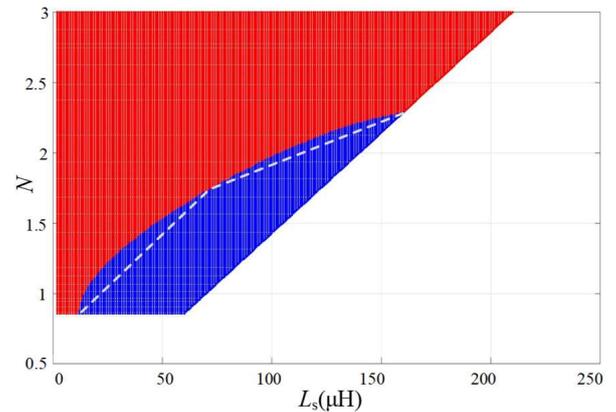
Figure 6. I_{pp} at full load range when $N = 1.5$, $L_s = 40 \mu\text{H}$.

To find a safe design space to satisfy the current stress, the value of I_{pp} is calculated for all possible combinations of N and L_s under the operating condition ($V_{smax} = 400 \text{ V}$, $P_{max} = 800 \text{ W}$) within the region under the transmission power constraint shown in Figure 5. It can be seen in Figure 7 that under the operating condition (400 V, 800 W), according to the parameter design space in Figure 5, there still exists a region where the maximum I_{pp} value is larger than the current stress that the MOSFET SCT3060AL can withstand; that is the red part in Figure 7a. The blue part shown in Figure 7b is the region where the parameters N and L_s under the current stress constraints are satisfied, and the red and blue boundary lines are fitted segmentally to form the new constraints between the parameters as:

$$\begin{cases} L_s \geq 68N - 47 \\ L_s \geq 160N - 206 \end{cases} \quad (10)$$



(a)



(b)

Figure 7. I_{pp} distribution for all combinations of N and L_s at conditions (400 V, 800 W): (a) I_{pp} distribution for all N and L_s ; (b) The region of parameters N and L_s satisfy the constraint.

Ultimately, a safe design space for the parameters N and L_s is obtained by constraining the transmitted power and current stress, which is the blue area in Figure 8. Although the safe design space of the parameters narrows down the value region of the parameters N and L_s , the specific values of N and L_s still cannot be obtained. Therefore, the following consideration is to explore the influence of parameters N and L_s on the converter’s efficiency from the perspective of the converter’s performance to narrow the design region of the parameters further.

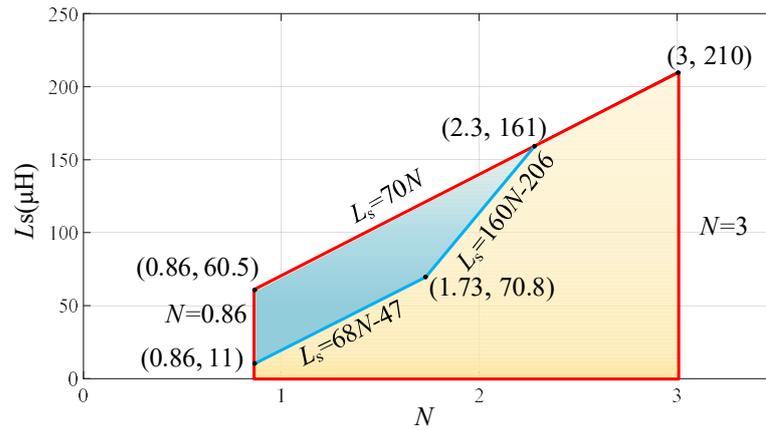


Figure 8. Safe design space for parameters N and L_s .

4. Optimization Design Space for Parameters

To ensure that the parameters selected in the safe design space perform well in terms of converter efficiency, this subsection mainly explores the influence of parameters N and L_s on converter loss. The parameters N and L_s affects the waveform of inductor current i_{L_s} , which changes the RMS value of inductor current and the current value of each switching moment. These will affect the conduction loss and ZVS range of the converter, respectively. Therefore, the optimized design space of parameters N and L_s is explored below from the optimization perspective of conduction loss and switching loss.

4.1. Parameter Optimization Design Based on Conduction Loss

As shown in Figure 3b, the inductor current RMS I_{L_RMS} of the converter varies switching cycle by switching cycle within $T_g/2$, so comparing the magnitude of conduction loss with different parameters by the I_{L_RMS} is impossible. In this section, the energy consumed by the converter on the switch conduction resistance R_{ds_on} in $T_g/2$ is calculated from the definition of conduction loss. Since both the primary and secondary sides of the converter conduct two switch at the same time, the energy consumed on the primary and secondary switch conduction resistors in $T_g/2$, E_{on_pri} , E_{on_sec} , is:

$$\begin{cases} E_{on_pri} = P_{on_pri} \cdot (T_g/2) = \sum_{m=1}^{1000} (I_{L_RMS}^2(m) \cdot 2R_{ds_on} \cdot T_s) \\ E_{on_sec} = P_{on_sec} \cdot (T_g/2) = \sum_{m=1}^{1000} (N^2 I_{L_RMS}^2(m) \cdot 2R_{ds_on} \cdot T_s) \end{cases} \quad (11)$$

Thus, the total loss $P_{on} = P_{on_pri} + P_{on_sec}$ is calculated by the following equation:

$$P_{on} = I_{L_RMS}^2 \cdot 4R_{ds_on} = \sum_{m=1}^{1000} (I_{L_RMS}^2(m) \cdot 2R_{ds_on} + N^2 I_{L_RMS}^2(m) \cdot 2R_{ds_on}) / 1000 \quad (12)$$

From the above equation, the current rms value I_{RMS} under the conduction loss equivalent of the converter can be defined, and the relationship between I_{RMS} and the rms value of the inductor current I_{L_RMS} for each switching cycle is:

$$I_{RMS} = \sqrt{\frac{1 + N^2}{2}} \sqrt{\left(\sum_{m=1}^{1000} I_{L_RMS}^2(m)\right) / 1000} \quad (13)$$

From Equation (11), when the transformer ratio $N = 1$, the square of the I_{RMS} is equal to the average of the sum of the squares of the I_{L_RMS} for 1000 switching cycles. The I_{RMS} can intuitively reflect the magnitude of the converter conduction loss; therefore, in this section, the I_{RMS} is solved for different combinations of parameters N and L_s under the operating condition (400 V, 800 W) to explore the effect of parameters on the magnitude of the conduction loss.

In Figure 9a, the curve of I_{RMS} with L_s is obtained when the transformer ratio $N = 1.5$. It can be seen from the figure that at the same transformer ratio N , the I_{RMS} decreases with the increase of inductance L_s . Then, the curve of I_{RMS} with L_s was obtained for transformer ratios $N = 0.9, 1.2, 1.5, 1.8,$ and 2.1 , respectively. As shown in Figure 9b, the I_{RMS} increases with the increase of transformer ratio N at the same L_s . Therefore, within the safe design space of parameters N and L_s , the smaller the transformer ratio N and the larger the inductance L_s , the smaller the I_{RMS} of the converter and the lower the corresponding conduction loss. The influence of parameters N and L_s on the switching loss of the converter is discussed below.

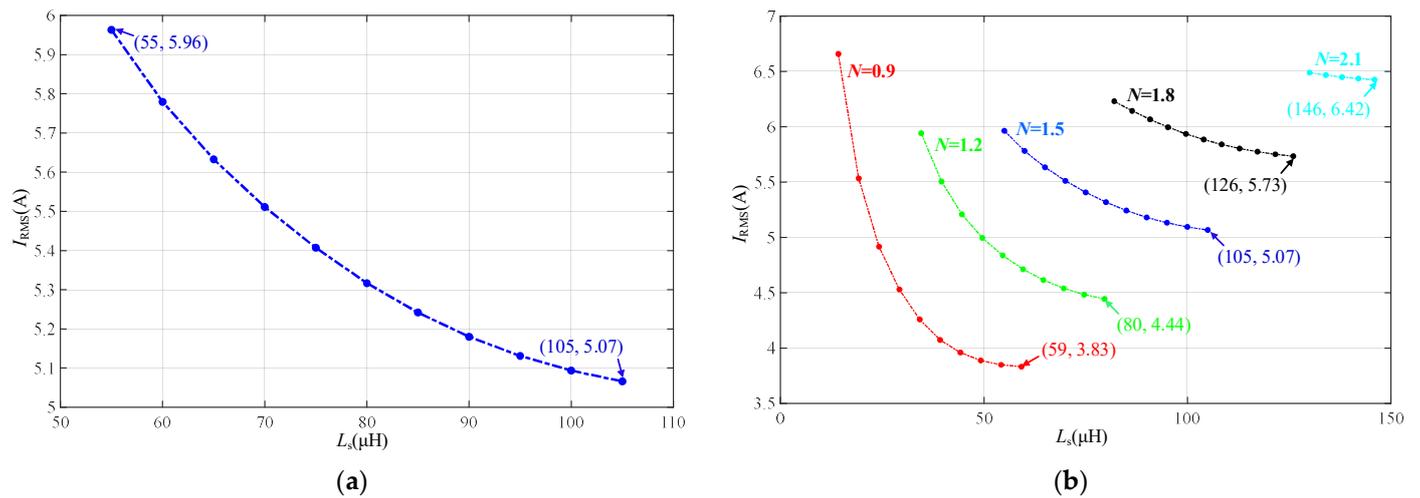


Figure 9. Variation of I_{RMS} with different combinations of parameters N and L_s under the condition (400 V, 800 W): (a) I_{RMS} - L_s curve at $N = 1.5$; (b) I_{RMS} - L_s curve at different N .

4.2. Parameter Optimization Design Based on Switching Loss

The optimization of the converter switching losses is mainly achieved by expanding the soft-switching range of the switch. For the MOSFET SCT3060AL, since its turn-on loss is much more significant than the turn-off loss, this section mainly analyzes the influence of the parameters on the zero-voltage turn-on (ZVS) range of the converter switch.

From the ZVS analysis results of the converter under EPS modulation in Figure 4, to quantitatively compare the ZVS realizations of the converter under different combinations of parameters N and L_s , it is necessary to count the ZVS realizations of the eight switch in the converter under a specific operating condition within $T_g/2$, totally 8000 switching cycles. To simplify the ZVS analysis of the converter, the curve of the number of hard-switching of the converter as a function of L_s is obtained for the operating condition (400 V, 800 W) with $N = 1.5$, Figure 10a. Similarly, curves for the number of hard-switching of the converter concerning the Inductance L_s are obtained for transformer ratios $N = 0.9, 1.2, 1.5, 1.8,$ and 2.1 , Figure 10b.

As shown in Figure 10, the number of hard-switching switch decreases with the increase of inductance L_s at the same N . The number of hard-switch of the converter decreases as the transformer ratio N increases. Based on the above analysis, it can be seen that the change in transformer ratio N has an opposite effect on the conduction loss and switching loss of the converter. In contrast, the change in inductance L_s has the same effect on the converter's conduction loss and switching loss. Considering that the I_{RMS} is large for $N > 1.8$, the design interval for transformer ratio $N > 1.8$ is excluded. Based on this, the optimized design space for the parameters is obtained, Figure 11.

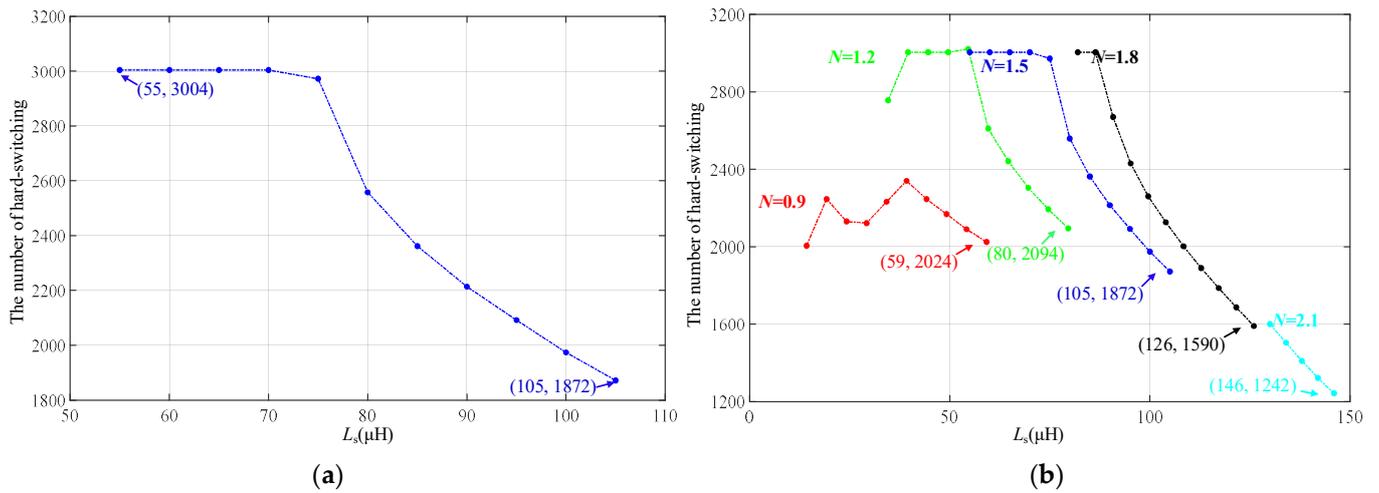


Figure 10. ZVS realizations with different parameters N and L_s under the condition (400 V, 800 W): (a) The number of hard-switching under $T_g/2$ at $N = 1.5$; (b) The number of hard-switching under $T_g/2$ at different N .

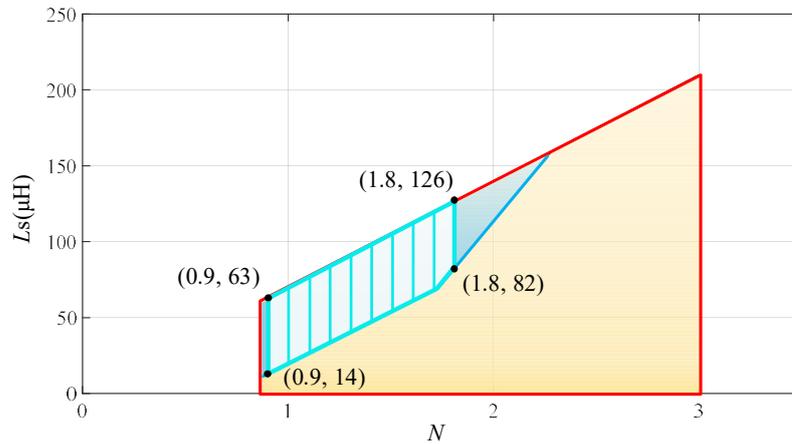


Figure 11. Optimization design space for parameters N and L_s .

In the optimization design space of parameters, the I_{RMS} and ZVS ranges are comprehensively compared under different combinations of parameters N and L_s . The discrete statistics of I_{RMS} and ZVS ranges corresponding to the parameters under the optimized design space are performed. As shown in Figure 12, where the transformer ratio N is set to a step of 0.1 and the power inductance L_s is set to a step of 5 μH , and the distributions of the I_{RMS} and the number of hard-switching under the different combinations of the parameters are obtained.

As shown in Figure 12: (1) under the same transformer ratio N , the I_{RMS} and the number of hard-switching switch both decrease with the increase of inductance L_s , so for the same transformer ratio N , the value of the optimized design parameter for L_s is always the maximum value in the design space; (2) when the transformer ratio $N = 0.9$ and $L_s = 63 \mu\text{H}$, its conduction loss is minimum but the switching loss is significant; (3) when the transformer ratio $N = 1.8$ and $L_s = 126 \mu\text{H}$, its switching loss is minimum but the conduction loss is largest. To determine the optimal parameters, the conduction loss and switching loss ratios under different parameters are quantitatively evaluated. In the following, the losses of the converter under three parameter combinations (0.9,63), (1.5,105) and (1.8,126) are quantitatively analyzed by using the converter loss analysis model.

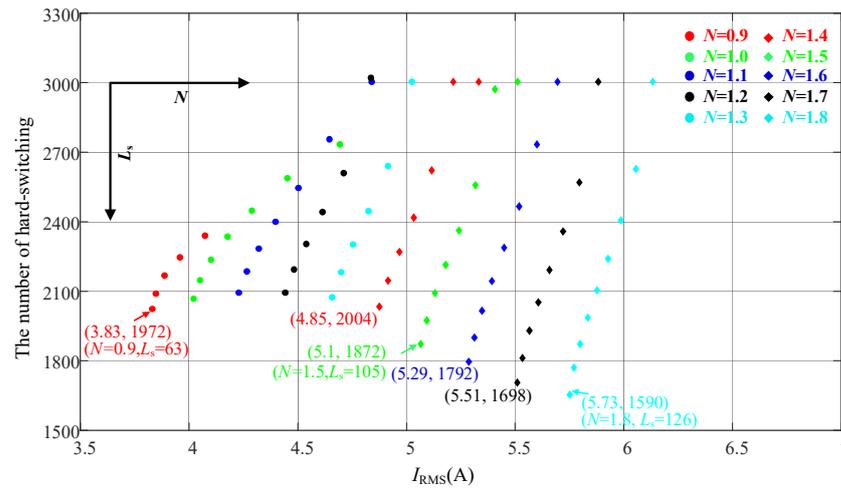


Figure 12. Discrete Statistics of I_{RMS} and ZVS for different parameters N and L_s .

5. Loss Analysis to Determine Parameter Optimization Results

The losses in a DAB AC-DC converter mainly include the conduction loss P_{con_sw} and switching loss P_{sw} of the power switches, copper loss P_{cu} and core loss P_{core} of the magnetic elements [18,19]. Precisely, the total conduction loss P_{con} is calculated as the sum of the switch conduction loss and the magnetic element copper loss, which is proportional to the square of the I_{RMS} . For the switching loss, a simple and effective switching loss model is used in ref. [20] to predict the switching loss of the switch under different operating conditions. Both turn-on and turn-off losses are included in the calculation. The key to the core loss calculation is to find the operating magnetic density, which is usually related to the cross-sectional area of the magnetic device, and then combine it with the core loss density in the material datasheet to calculate the core loss [21]. In this paper, according to the AP method, the core size of the transformer is PQ5050, the core size of the inductor is PQ3535, and the winding wire type is 0.1×200 winding. The specific loss analysis process is shown in Appendix A.

Using the loss analysis model of each part of the converter, the loss of the converter under each optimized parameter combination can be analyzed, and then its theoretical efficiency can be obtained. First, the parameter combination under $N = 0.9, L_s = 63 \mu\text{H}$ is numbered as “1”; $N = 1.5, L_s = 105 \mu\text{H}$ is numbered as “2”; $N = 1.8, L_s = 126 \mu\text{H}$ is numbered as “3”. Then the theoretical losses and efficiencies of the converter at output voltage $V_s = 360 \text{ V}$ and 400 V and transmitted power from 200 W to 800 W were calculated and the results are shown in Figure 13.

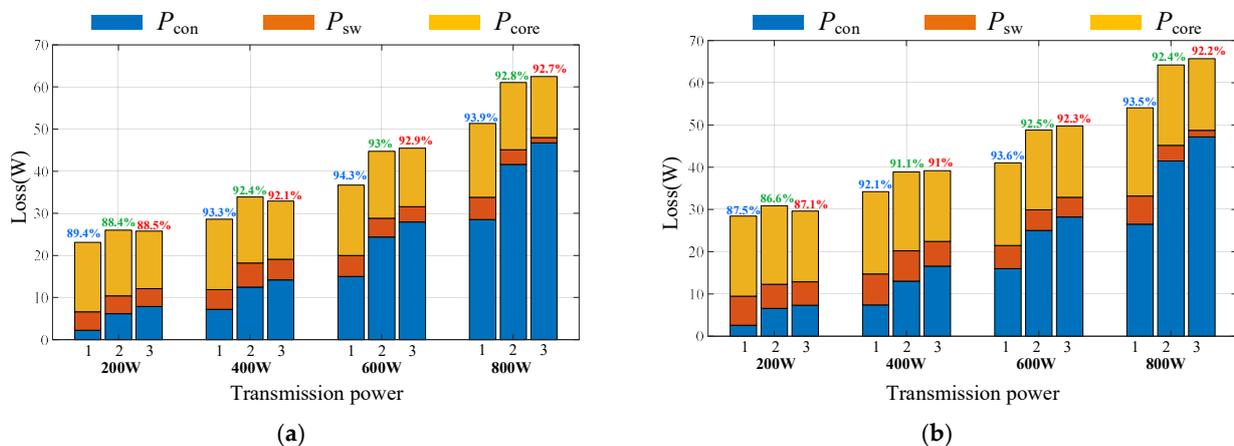


Figure 13. Power losses at different working conditions for different parameters: (a) output voltage $V_s = 360 \text{ V}$; (b) output voltage $V_s = 400 \text{ V}$.

As shown in Figure 13, the core loss generally does not change much with power, so the core loss accounts for the main part in the low-power condition. With the increase of power, the proportion of conduction loss in the system increases significantly, at which point the proportion of core loss gradually decreases. From the switching loss in the full-power section in Figure 13, it can be seen that the switching loss accounts for a relatively small proportion of the overall loss of the converter because most of the switch of the converter under the EPS can realize the ZVS, and the switching loss of the MOSFET SCT3060AL is relatively tiny.

By comparing the efficiencies of different parameters under the same operating condition, it can be seen that, although parameters “2” and “3” have smaller switching loss compared with parameter “1”, due to the small proportion of switching loss in the total loss, the conduction loss of parameter “1” is much smaller than that of the other two parameters. Therefore, the overall efficiency of the converter with parameter combination “1”, with transformer ratio $N = 0.9$ and $L_s = 63 \mu\text{H}$, is higher than that of other parameter combinations.

6. Experimental Verification

In the above work, the step-by-step constraints on the transformer ratios N and L_s are applied to gradually narrow their design ranges with the design requirements of the converter’s parameters, and the parameter optimization results of the transformer ratio $N = 0.9$ and $L_s = 63 \mu\text{H}$ are finally determined by loss analysis. Therefore, in this section, a single-stage totem pole DAB AC-DC converter experimental prototype is built, as shown in Figure 14. Customized with three different groups of parameters of N and L_s , the experimental results under different parameter groups are compared to prove the effectiveness of the parameter optimization design method.

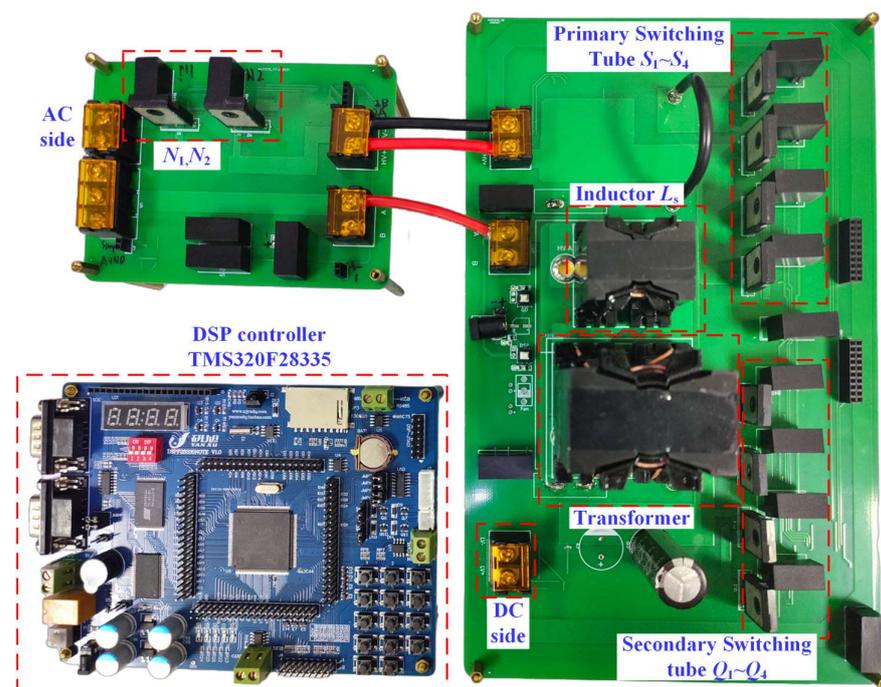


Figure 14. Single-stage totem pole DAB AC-DC experimental prototype.

The transformer and power inductance for three groups of parameters are shown in Table 2. The first group of parameters is the optimized design result: $N = 0.9$, $L_s = 65 \mu\text{H}$; the second group of parameters is: $N = 1$, $L_s = 55 \mu\text{H}$, and the third group of parameters is: $N = 1.5$, $L_s = 107 \mu\text{H}$.

Table 2. The transformers and inductor with different parameters.

Group I	Group II	Group III
$N = 0.9:1$ $L_s = 65 \mu\text{H}$	$N = 1:1$ $L_s = 55 \mu\text{H}$	$N = 1.5:1$ $L_s = 107 \mu\text{H}$
		

Figure 15 shows the experimental waveforms of the converter at operating condition (360 V, 800 W) with three groups of parameters. Among them, Figure 15a shows the experimental waveforms under the parameter combination of “ $N = 0.9, L_s = 65 \mu\text{H}$ ” where the AC current amplitude $I_g = 11.05 \text{ A}$; Figure 15b shows the experimental waveforms under the parameter combination of “ $N = 1, L_s = 55 \mu\text{H}$ ”, where the AC current amplitude $I_g = 11.14 \text{ A}$; Figure 15c shows the experimental waveform with parameter combination of “ $N = 1.5, L_s = 107 \mu\text{H}$ ”, and the AC current amplitude $I_g = 11.32 \text{ A}$. Through the test, the efficiencies of the converter in the three groups of parameters are 93.5%, 93.2%, and 91.2%, respectively.

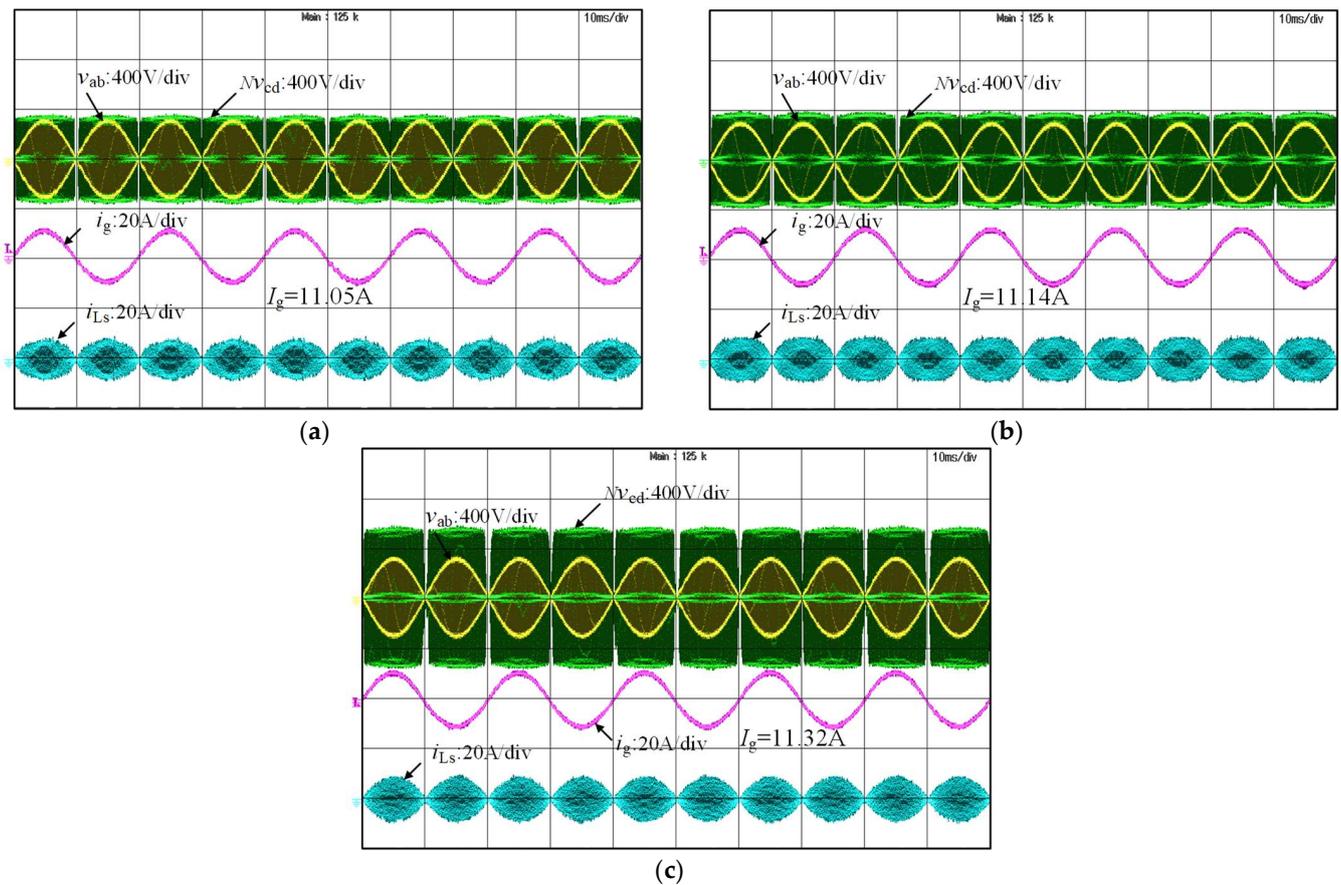


Figure 15. Waveforms of each group of parameters under condition (360 V, 800 W): (a) $N = 0.9, L_s = 65 \mu\text{H}$; (b) $N = 1, L_s = 55 \mu\text{H}$; (c) $N = 1.5, L_s = 107 \mu\text{H}$.

Figure 16 shows the experimental waveforms of the converter at operating condition (400 V, 800 W) with three groups of parameters. Among them, Figure 16a shows the experimental waveforms under the parameter combination of “ $N = 0.9, L_s = 65 \mu\text{H}$ ” where the AC current amplitude $I_g = 11.15 \text{ A}$; Figure 16b shows the experimental waveforms under the parameter combination of “ $N = 1, L_s = 55 \mu\text{H}$ ”, where the AC current amplitude $I_g = 11.21 \text{ A}$; Figure 16c shows the experimental waveform with parameter combination of “ $N = 1.5, L_s = 107 \mu\text{H}$ ”, and the AC current amplitude $I_g = 11.4 \text{ A}$. Through the test, the efficiencies of the converter in the three groups of parameters are 92.5%, 92.1%, and 90.5%, respectively.

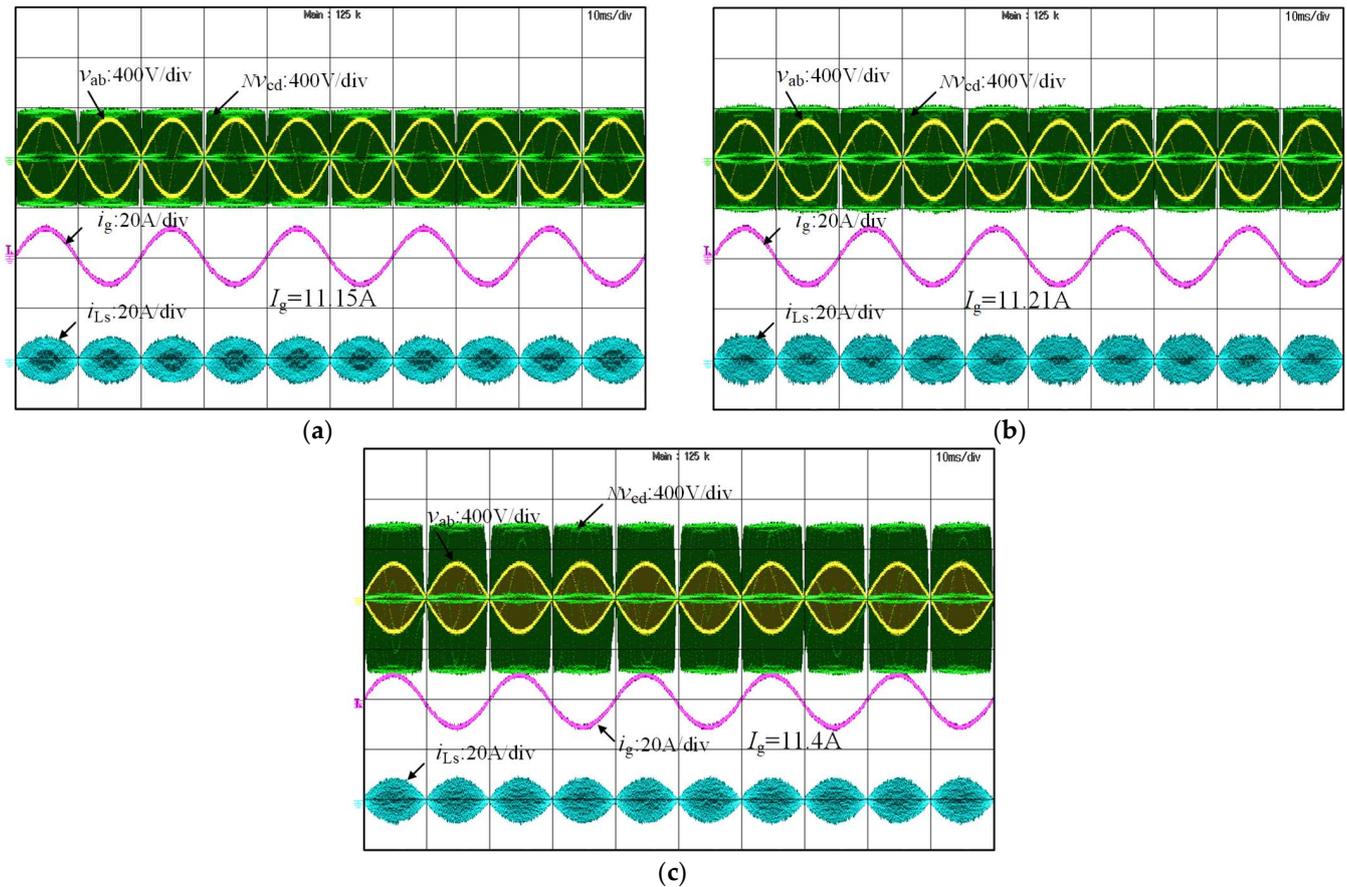


Figure 16. Waveforms of each group of parameters under condition (400 V, 800 W): (a) $N = 0.9, L_s = 65 \mu\text{H}$; (b) $N = 1, L_s = 55 \mu\text{H}$; (c) $N = 1.5, L_s = 107 \mu\text{H}$.

The efficiencies of each power under the three groups of parameters were tested separately, and the results are shown in Figure 17. When the output voltage $V_s = 360 \text{ V}$, the overall efficiency of the converter under the first group of parameters is the highest and the peak efficiency reaches 93.7%. When the output voltage $V_s = 400 \text{ V}$, the overall efficiency of the converter under the first group of parameters is the highest and the peak efficiency reaches 92.8%. According to the comparison of the experimental results in Figure 17a,b, the overall efficiency of the converter at the output voltage $V_s = 360 \text{ V}$ is higher than that at $V_s = 400 \text{ V}$, which is consistent with the loss analysis results.

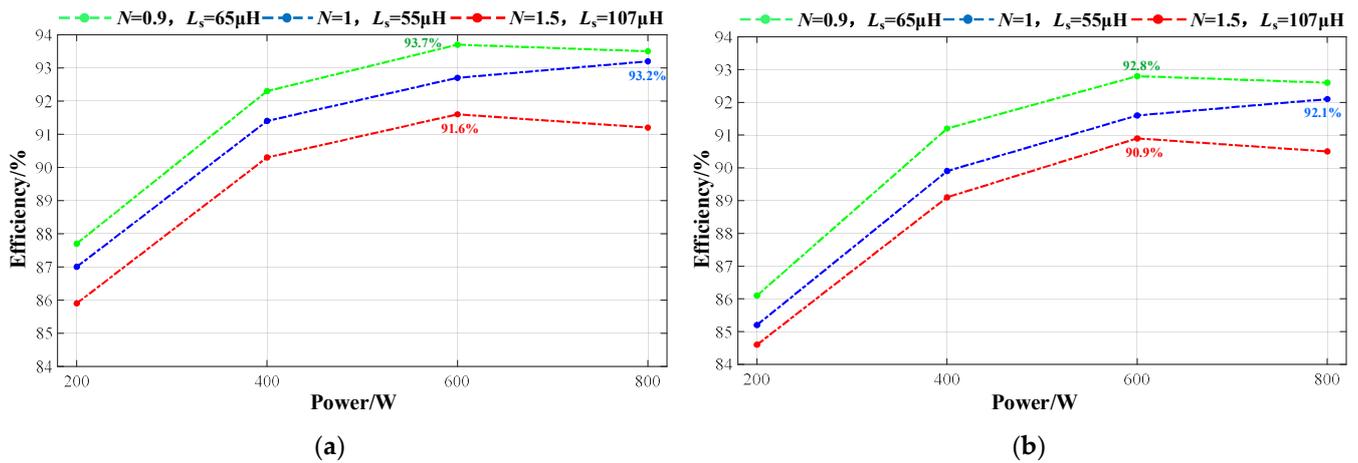


Figure 17. Efficiency curves of three groups of parameters under different operating conditions: (a) $V_s = 360\text{ V}$; (b) $V_s = 400\text{ V}$.

The above experimental results demonstrate the improvement of the converter’s overall efficiency under the parameters $N = 0.9$ and $L_s = 65\ \mu\text{H}$. Compared with the efficiency of the converter under the remaining two groups of parameters, the overall efficiency of the parameter-optimized converter is improved by 0.7% and 1.9% at the output voltage $V_s = 360\text{ V}$ and by 1% and 2.1% at $V_s = 400\text{ V}$, respectively.

However, as shown in Figure 18, there is an error between the computational and experimental efficiency of the designed parameters.

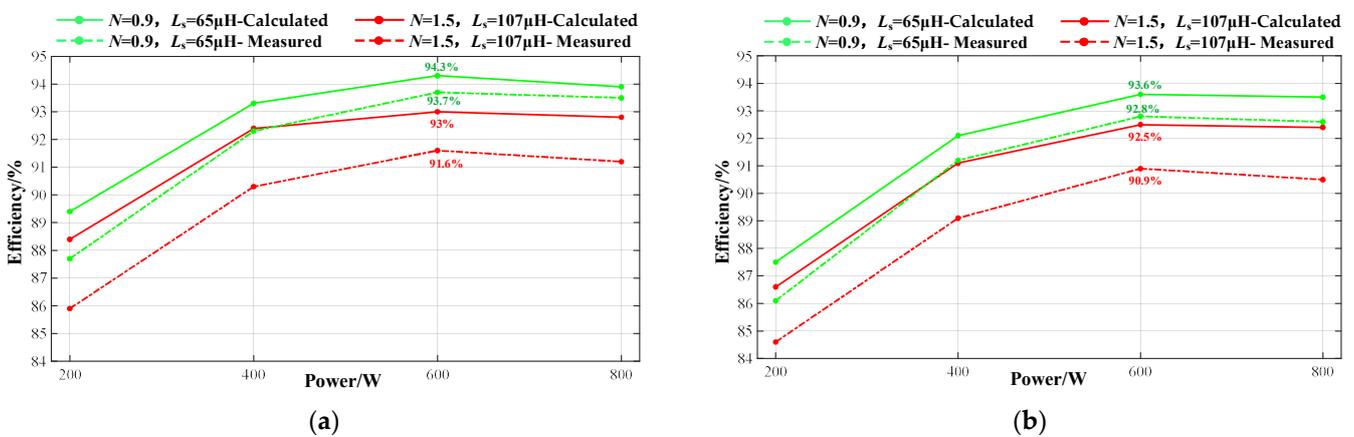


Figure 18. Comparison of the calculated efficiency with the measured efficiency: (a) $V_s = 360\text{ V}$; (b) $V_s = 400\text{ V}$.

After comparison, it can be found that there are some deviations between the calculated and measured values of efficiency, with the largest deviation occurring at $V_s = 360\text{ V}$, $P = 400\text{ W}$, and at the parameters $N = 1.5, L_s = 105\ \mu\text{H}$, the calculated value is 92.4% while the measured value is 90.5%, a difference of 1.9%.

This is mainly due to the following reasons: (1) the effect of temperature on resistance is not taken into account in the calculation of conduction loss; (2) the simplified model for calculating switching loss makes the switching loss inaccurate; (3) the Steinmetz equation taken in the calculation of core loss is not accurate enough for non-sinusoidal signal; (4) other converter losses besides the above mentioned losses are not taken into account. However, in general, the calculated and measured efficiency trends for the parameters are consistent.

7. Conclusions

To improve the overall efficiency of the single-stage DAB AC-DC converter, this paper proposes a parameter design method that considers multi-timescale analysis by combining the steady-state model in line cycle and switching cycle. Using the idea of step-by-step constraints establishes the safe design space and optimization design space of parameters. The design space of the parameters is reduced step by step, which reduces the computational amount of the loss analysis model. Compared with the traditional method based on the parameter design of the DAB DC-DC converter, the proposed optimization design method fully considers the steady-state characteristics of the line cycle of the DAB AC-DC converter, and the step-by-step constraint greatly accelerates the parameter design process. The final experimental results verify the effectiveness of the proposed parameter optimization design method.

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Appendix A

The loss analysis of the DAB AC-DC converter is mainly composed of the following three parts: conduction losses, switching losses and core losses, which are derived as follows.

(1) Conduction losses

The conduction loss P_{con} of the converter mainly consists of the conduction loss of the switch $P_{\text{con_sw}}$ and the copper loss of the magnetic element P_{cu} .

The conduction loss of the switch $P_{\text{con_sw}}$ is:

$$P_{\text{con_sw}} = 2R_{\text{ds_on}}I_{\text{g_RMS}}^2 + (2R_{\text{ds_on}} + 2N^2R_{\text{ds_on}})I_{\text{RMS}}^2 \quad (\text{A1})$$

The copper loss of the magnetic element P_{cu} is:

$$P_{\text{cu}} = R_{\text{Lg}}I_{\text{g_RMS}}^2 + (R_{\text{Ls}} + R_{\text{Tp}} + N^2R_{\text{Ts}})I_{\text{RMS}}^2 \quad (\text{A2})$$

where $R_{\text{ds_on}}$ is the on-resistance of the switch, R_{Lg} is the winding resistance of the AC side inductor L_{g} , R_{Ls} is the winding resistance of the power inductor L_{s} , R_{Tp} , and R_{Ts} are the winding resistances of the primary and secondary sides of the high-frequency transformer, respectively.

(2) Switching losses

The turn-on loss and turn-off loss of the converter are calculated as follows:

$$\begin{cases} P_{\text{on}} = \frac{1}{2}V_{\text{ds}}I_{\text{ds-RMS}}t_{\text{tr-on}}f_{\text{s}} + \frac{1}{2}C_{\text{oss}}V_{\text{ds}}^2f_{\text{s}} \\ P_{\text{off}} = \frac{1}{2}V_{\text{ds}}I_{\text{ds-RMS}}t_{\text{tr-off}}f_{\text{s}} - \frac{1}{2}C_{\text{oss}}V_{\text{ds}}^2f_{\text{s}} \end{cases} \quad (\text{A3})$$

where f_{s} denotes the switching frequency, t_{tr} represents the turn-on and turn-off durations of the switch. And the energy stored in the switch's capacitance C_{oss} can be obtained by fitting the $C_{\text{oss}}-V_{\text{ds}}$ curve from the datasheet of SCT3060AL.

(3) Core losses

The magnitude of core loss is mainly related to the flux density B_m , magnetization frequency f_s , material coefficients α and β , and core volume V_{core} . The core loss is generally calculated using the Steinmetz equation (SE):

$$P_{\text{core}} = V_{\text{core}} f_s^\alpha B_m^\beta \quad (\text{A4})$$

Specific design of transformers and inductors as follows:

For a high-frequency transformer with core model PQ5050, the AP calculation equation is:

$$AP = A_e A_w = \frac{P_T}{2f_s B_m J K_0} \quad (\text{A5})$$

where A_e is the core effective cross-sectional area and A_w is the core window area. P_T is the transformer power, which is the sum of the transformer primary and secondary power. k_0 is the core window utilization taken, J is the current density, B_m is the maximum flux density.

For the power inductor L_s with core model PQ3535, the AP calculation equation is:

$$AP = A_e A_w = \left(\frac{L_s I_{\text{peak}}^2}{B_m J K_0} \right)^{1.14} \quad (\text{A6})$$

where L_s is the inductance value and I_{peak} is the peak inductance current.

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