Special Issue

Negative Capacitance Field-Effect Transistors

Message from the Guest Editor

High-performance logic transistors require a large on-state current in order to guarantee fast operation, and, simultaneously, a suppressed off-state current in order to reduce the stand-by power consumption. Unfortunately, the subthreshold swing—the efficiency of a transistor switching between on and off states—is limited to 60 mV/dec by the so-called Boltzmann tyranny. One possible solution to circumvent this fundamental physics limit, as proposed by S. Salahuddin and S. Datta in 2008, is to build negative capacitance field-effect transistors (NC-FET) by introducing a ferroelectric dielectric material into the gate stack. This Special Issue calls for research papers, communications, and review articles that focus on the following: (1) experimental progress in NC-FET with innovative materials, device structures, and fabrication processes; (2) exploration of novel functionality using NC-FET and ferroelectricity in general; and (3) critical examination of the microscopic mechanisms of ferroelectric switching and the impact on FET operations.

Guest Editor

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Deadline for manuscript submissions

closed (31 August 2021)

Micromachines

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