Special Issue

Network-on-Chip and Application

Message from the Guest Editors

Advancement in computing system architectures, coupled with the Moore's Law and Dennard scaling, has enabled system-on-a-chip (SoC) architects to accommodate hundreds of processing, memory, and other cores on a single chip. The network-on-a-chip (NoC) paradigm is based on packet-switched routing mechanism. It can address most of the on-chip communication problems, including performance limitations of long interconnects and the integration of many heterogeneous cores on a chip. However, NoC performance, hardware cost, and power consumption depend on its various parameters, such as topology, the number and depth of virtual channels, routing, and flow control mechanisms. The goal of this Special Issue is to assemble and put forward innovative ideas and solutions related to NoC architecture, design, implementation, and applications. Moreover, the NoCs for FPGAs, multi/many-core SoCs, and heterogeneous systems will also be explored. Researchers and developers are invited to submit their unpublished network-on-a-chip-related work. The extended versions of published papers in conferences, symposiums or workshops are also welcomed.

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