Special Issue

CMOS Low Power Design Vol. 2

Message from the Guest Editors

Edge-AI hardware encompasses several aspects of low-power circuit design which exploit novel devices, circuits, and system architectures to realize high energy-efficiency. Event-driven asynchronous circuits enable low power consumption, while emerging post-CMOS nonvolatile memory devices promise very high-density in-memory computing with reduction in energy per synaptic operation. At the same time, digital architectures and field-programmable gate arrays (FPGAs) leverage approximate computing algorithms and partial reconfiguration to trade off energy efficiency with precision. Novel sensor interfaces and security of such devices will be essential for widespread deployment of Edge-AI. Authors are invited to submit regular papers following the *JLPEA* submission guidelines within the remit of the second volume of the Special Issue call. Topics include but are not limited to:

- Ultra-low power
- Edge-AI
- Neuromorphic computing
- IoTs
- Mixed-signal
- Emerging devices
- In-memory computing
- Hardware security

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Deadline for manuscript submissions

closed (30 September 2020)

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About the Journal

Message from the Editor-in-Chief

Journal of Low Power Electronics and Applications (ISSN 2079-9268) is an open access journal which provides an advanced forum for the studies of electronics for low power applications. A special emphasize is made on ultralow power bio-medical applications. It publishes reviews, regular research papers and short communications.

Our aim is to encourage scientists to publish their experimental and theoretical results in as much detail as possible. There is no restriction on the length of the papers. Full experimental and/or methodical details must be provided.

Editor-in-Chief

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Journal Rank:

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