Special Issue

Selected Papers from IEEE S3S Conference 2017

Message from the Guest Editors

For more than two decades, low-power consumption has been paramount for integrated circuits (ICs) and systems-on-a-chip (SoCs). In modern sub-100 nm technologies, low-power design flows have matured with techniques, such as clock/power gating, multi-Vt/Vdd assignment, and dynamic frequency/voltage scaling, being considered as mainstream. However, further power savings are still needed for extremely power-constrained applications, such as green computing, mobile wireless communications, IoT sensor nodes, and biomedical devices. Feasible ways of achieving further power savings include, for example, sub-threshold and ultra-low-voltage operation, SOI technology and circuits, and 3-D and heterogeneous integration. The 2017 IEEE Unified S3S (SOI-3D-SubVt) Conference event gathered researchers studying the aforementioned three topics to share their views and advances regarding lower-power and more efficient ICs and SoCs. This Special Issue is the seventh Special Issue dedicated to extended versions of papers from the IEEE S3S Conference 2017 based on their low-power content and their scientific/technical excellence.

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Message from the Editor-in-Chief

Journal of Low Power Electronics and Applications is an open access journal which provides an advanced forum for rapid dissemination of innovative research and important results in all aspects of low power electronics and design.
It publishes reviews, regular research papers and short communications. Our aim is to encourage scientists to publish their experimental and theoretical results in as much detail as possible. The full experimental details must be provided so that the results can be reproduced.

Editor-in-Chief

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