Special Issue

CMOS Power Amplifier Design and Applications

Message from the Guest Editors

The design of CMOS power amplifiers continues to pose challenges in the design of wireless transceivers because of the low breakdown voltage in CMOS devices, the no-substrate via-hole in the CMOS process, and the low quality of the passive components. In particular, a highly linear power amplifier is required because of the high peak-to-average power ration and the wide bandwidth signal for 5G and next generation WLAN systems. Also, recent wireless communication standards require power amplifiers supporting dual or multi-bands. On the other hand, it is important to develop a tunable power amplifier that can minimize the efficiency degradation under impedance mismatch conditions. Topics in this Special Issue include (but are not limited to):

- CMOS power amplifiers for 5G systems, LTE, WLAN, etc.
- CMOS power amplifiers with high power, high efficiency and/or high linearity
- Dual-band or multi-band CMOS power amplifiers
- Tunable CMOS power amplifiers
- Envelope tracking power amplifiers
- Doherty power amplifiers
- Outphasing power amplifiers
- Digital power amplifiers
- Transmitters with CMOS power amplifiers

Guest Editors

Prof. Dr. Ilku Nam

Integrated Circuits & Systems Lab., Dept. of Electrical Engineering, Pusan National University, 2 Busandaehak-ro, Geumjeong-gu, Busan 46241, Republic of Korea

Prof. Dr. Ockgoo Lee

Wave Integrated Circuits and Systems Lab., Dept. of Electrical Engineering, Pusan National University, Busan 46241, Republic of Korea

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Electronics
Editorial Office
MDPI, Grosspeteranlage 5
4052 Basel, Switzerland
Tel: +41 61 683 77 34
electronics@mdpi.com

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Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guest-edited by leading experts in selected topics of interest.

Editor-in-Chief

Prof. Dr. Flavio Canavero
Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Torino, Italy

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