Special Issue

Hardware Design Systems at Chip and Board Level

Message from the Guest Editor

We invite contributions for a SI on hardware design methodologies, specification languages, and standards for on-chip and inter-chip interconnect. Designers are increasingly looking for turn-key tool flows when assembling components at the ASIC, MCM, PCB or rack level. Automated flows validate functional requirements, estimate metrics for performance, area and energy, and generate documentation and software stubs for hardware/software co-design and hierarchical modular assembly. High-performance serial interconnect is increasingly used at the physical layer with channel bonding, channel sharing, and protocol adaption implemented in hardware at the end points. Automatic deployment of such channels is especially important for portable hardware accelerators that must be projected onto different numbers of FPGAs on various blades. Equally, memory bank aggregation and sharing must also be managed with something akin to link editing required to allocate address maps in both DRAM and register spaces. Again, inter-vendor tool flows should preferably manage the nuts-and-bolts of debug access and facilitate multi-chip composition.

Guest Editor

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Deadline for manuscript submissions

closed (31 October 2021)

Electronics

an Open Access Journal by MDPI

Impact Factor 2.6
CiteScore 6.1

mdpi.com/si/53205

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Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guest-edited by leading experts in selected topics of interest.

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