Special Issue

Research on Key Technologies for Hardware Acceleration

Message from the Guest Editor

To meet the requirements of modern intelligent systems, customized hardware accelerators are emerging for different tasks by integrating cross-level optimizations and innovations of algorithm, compilation, architecture, and circuit designs. The aim of this Special Issue is to focus on the key technologies including reconfigurable FPGAs, 2.5D/3D chiplets, and in-/near-memory computing for hardware acceleration. Submissions for this Special Issue on “Research on Key Technologies for Hardware Acceleration” are welcome on any scope related, but not limited, to the following areas:

- Co-optimization of hardware-friendly emerging AI algorithms, including pruning, quantization, etc.
- Reconfigurable hardware accelerators on FPGA for intelligent vision tasks.
- The ultra-low power ASIC accelerator for voice applications.
- The methodologies of compilation and mapping to AI hardware accelerators.
- The hardware accelerators based on in-/near-memory computing architecture.
- The interconnection and parallel structure of 2.5D chiplets or 3D stacked chips.

Guest Editor

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Message from the Editor-in-Chief

Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guest-edited by leading experts in selected topics of interest.

Editor-in-Chief

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manuscripts are peer-reviewed and a first decision is provided to authors approximately 16.8 days after submission; acceptance to publication is undertaken in 2.4 days (median values for papers published in this journal in the first half of 2025).

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