Special Issue

Recent Advances in High-Speed Electronics

Message from the Guest Editor

This Special Issue addresses advances in high-speed electronics aimed at resolving potential technical issues in high-speed systems. As the data rate increases, data transmission experiences numerous changes, including parasitic effects in high-speed interconnects. Nodes in schematics are theoretically ideal, which has no effect on the electrical performance in circuit theory. The nodes are expressed as a combination of parasitic resistance (R), inductance (L), and capacitance (C). Thus, nodes must be investigated for accurate analysis of data transmission. Another change concerns the buffer or complementary metal oxide semiconductor (CMOS) in high-speed systems. The buffer was previously assumed to be an ideal driver; however, it is no longer considered to be a simple driver due to its electrical performance. To handle this issue, the input/output buffer information specification (IBIS) was introduced. The change that must be highlighted is equalization to compensate for electrical loss during high-speed data transmission. The above changes are critical in high-speed system design. Thus, they are the focus of this Special Issue regarding high-speed systems.

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Message from the Editor-in-Chief

Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guest-edited by leading experts in selected topics of interest.

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