Special Issue

Advanced Electronic Packaging Technology

Message from the Guest Editor

As Moore's Law is reaching its limitation, the development of advanced packaging is moving towards advanced system integration in order to achieve more function, lower cost and smaller form factor. Advanced packaging brings the heterogeneous integration of various front-end technology nodes and higher levels of customization down both the scaling and functional roadmap. Recently, new technologies, such as TSV (Though Silicon Via), Wafer-level Fan-out (WL-FO) and 3D IC stacking, are fast growing and play important roles in the applications of advanced system integration. In this Special Issue, the recent progress on advanced packaging technologies will be presented including WLP, 3D IC, 2.5D Interposer, TSV, TGV, Fan-Out, Flip-Chip, 3D WLCSP, Hybrid bonding, Panel-level packaging, etc.

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Message from the Editor-in-Chief

Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guest-edited by leading experts in selected topics of interest.

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