

Special Issue

Next-Generation Accelerator Architectures for AI and Deep Learning

Message from the Guest Editor

The exponential growth of AI and DL applications has driven the demand for specialized hardware that can deliver exceptional performance, efficiency, and scalability. Traditional general-purpose processors are no longer sufficient to meet the computational and energy requirements of modern AI and DL workloads. As such, this Special Issue focuses on exploring the design, development, and deployment of next-generation accelerator architectures tailored for AI and DL. Topics covered include innovative hardware designs, such as Tensor Processing Units, Graphics Processing Units, and custom accelerators like Application-Specific Integrated Circuits and Field-Programmable Gate Arrays. This Issue also addresses architectural trends like heterogeneous computing, memory hierarchy optimizations, and emerging paradigms such as in-memory and neuromorphic computing. Contributions to this Issue emphasize both theoretical advancements and practical implementations, highlighting novel techniques to enhance throughput, reduce latency, and optimize energy efficiency. The Issue also explores software–hardware co-design, benchmarking frameworks, and real-world applications.

Guest Editor

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Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guestedited by leading experts in selected topics of interest.

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