Special Issue

Design of Hardware Accelerators for Deep Learning and Privacy-Preserving Machine Learning

Message from the Guest Editors

Deep Learning (DL) models are becoming increasingly complex and computationally demanding, straining traditional hardware. Simultaneously, the rise of privacy regulations and sensitive applications (e.g., healthcare, finance) necessitates robust Privacy-Preserving Machine Learning (PPML) techniques, which themselves impose significant computational overhead. Efficient specialized hardware accelerators are thus crucial to enable the practical deployment of powerful, privacy-conscious AI, especially in resource-constrained edge devices or large-scale cloud servers. This Special Issue thus aims to showcase cutting-edge research on novel hardware architectures and co-design methodologies that enable high-performance, energy-efficient execution of advanced DL models while integrating robust PPML techniques like Homomorphic Encryption (HE), Secure Multi-Party Computation (SMPC), and Trusted Execution Environments (TEEs).
Topics of interests include but not limited to the following:

- DL Hardware Accelerators
- Privacy-Preserving ML (PPML) Hardware
- Co-Design and Frameworks
- Emerging Technologies
- Efficiency and Security

Guest Editors

Dr. Rui Wang

Faculty of Electrical Engineering, Mathematics and Computer Science, Delft University of Technology, Van Mourik Broekmanweg 6, 2628 XE Delft, The Netherlands

Dr. Javad Dogani

IMDEA Networks Institute, Avenida del Mar Mediterráneo 22, 28918 Leganés, Spain

Deadline for manuscript submissions

15 February 2026

Electronics

an Open Access Journal by MDPI

Impact Factor 2.6
CiteScore 6.1

mdpi.com/si/246846

Electronics
Editorial Office
MDPI, Grosspeteranlage 5
4052 Basel, Switzerland
Tel: +41 61 683 77 34
electronics@mdpi.com

mdpi.com/journal/electronics

Electronics

an Open Access Journal by MDPI

Impact Factor 2.6
CiteScore 6.1

mdpi.com/journal/electronics

About the Journal

Message from the Editor-in-Chief

Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guest-edited by leading experts in selected topics of interest.

Editor-in-Chief

Prof. Dr. Flavio Canavero
Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Torino, Italy

Author Benefits

High Visibility:

indexed within Scopus, SCIE (Web of Science), CAPlus / SciFinder, Inspec, Ei Compendex and other databases.

Journal Rank:

JCR - Q2 (Engineering, Electrical and Electronic) / CiteScore - Q1 (Electrical and Electronic Engineering)

Rapid Publication:

manuscripts are peer-reviewed and a first decision is provided to authors approximately 16.8 days after submission; acceptance to publication is undertaken in 2.4 days (median values for papers published in this journal in the first half of 2025).