Special Issue

Secure Hardware Architecture and Attack Resilience

Message from the Guest Editors

The rapid advancement of digital systems and the increasing reliance on embedded devices in critical applications—such as IoT, autonomous vehicles, and industrial automation—have made hardware security a cornerstone of system integrity, confidentiality, and resilience. This Special Issue seeks high-quality research contributions that advance secure hardware architectures and attack-resilient designs, bridging theoretical security principles with practical, real-world implementations. We invite original research articles on topics including (but not limited to) the following:

- Hardware root of trust (PUF, TRNG, secure boot, measured boot, etc.);
- Cryptographic accelerators (ASIC/FPGA/GPU-based designs and implementations);
- Post-quantum cryptographic hardware;
- Fault injection (FI) and side-channel attack (SCA) and mitigation;
- Advances in micro-architecture attack and defense;
- RISC-V security;
- Trusted execution environments (TEEs) and confidential computing

We welcome submissions that address both theoretical and applied aspects of hardware security, with a focus on real-world applicability and robustness.

Guest Editors

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Deadline for manuscript submissions

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About the Journal

Message from the Editor-in-Chief

Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guestedited by leading experts in selected topics of interest.

Editor-in-Chief

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manuscripts are peer-reviewed and a first decision is provided to authors approximately 16.8 days after submission; acceptance to publication is undertaken in 2.4 days (median values for papers published in this journal in the first half of 2025).

