Special Issue

Challenges and Future Trends of In-Memory Computing in Micro-Chips

Message from the Guest Editors

The explosive growth of AI, edge computing and dataintensive applications has intensified the demand for high-performance, energy-efficient computing hardware. Conventional von Neumann architectures suffer from the memory wall, where frequent data transfer between memory and processing units dominates latency and power consumption. In-memory computing (IMC) offers a promising solution by performing computation within memory arrays, reducing data movement and enabling massive parallelism. This Special Issue focuses on the critical challenges that must be addressed for IMC to transition from laboratory prototypes to mainstream micro-chip deployments. Key issues include device variability, limited precision, endurance and retention constraints, peripheral circuit overhead, interface compatibility, programmability and the lack of standardized benchmarking. The scope spans device, circuit, architecture and system integration levels, covering both analog and digital IMC approaches across emerging memory technologies such as RRAM-, PCM-, FeFET- and SRAM-based CIM.

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