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# **Software Verification and Validation for Embedded Systems**

Guest Editor:

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Deadline for manuscript submissions:

closed (10 January 2021)

### **Message from the Guest Editor**

Dear Colleagues,

Verification evaluates intermediary products, such as requirement specification, architectural design, models, or software code, thus ensuring that they comply with previously established requirements for correctness, completeness, and consistency.

Embedded systems are electronically controlled devices where software and hardware are tightly coupled. Embedded systems often have unique characteristics that should be reflected in the verification and validation (V&V) plan. In this Special Issue, we are particularly interested in V&V at the software level for embedded systems.

- Methodologies for verification and validation of embedded software
- Techniques for testing of embedded software
- Tools and environment for automated and semiautomated embedded software testing
- Model-based testing
- Software test requirements and architecture
- Static vs. dynamic testing
- Performance, robustness, usability and security testing
- Software fault injection
- Embedded real time software testing and runtime error handling
- Fault localization and debugging
- Empirical studies and experience reports









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### **Editor-in-Chief**

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## **Message from the Editor-in-Chief**

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