



Deep Learning-Based Routing for Network-on-a-Chip (NoC): Opportunities, Challenges, and Solutions

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closed (30 September 2021)

Message from the Guest Editors

System-on-a-chip (SoC) technology incorporates all the required electronic circuits of numerous computer components onto a single integrated chip. This Special Issue aims to bring together leading as well as academic and industrial researchers to explore the opportunities of DL for routing in NoC and to focus its impact on the solutions of the aforementioned challenges and propose feasible solutions. We encourage papers covering various topics of interest that include but are not limited to the following list:

- DL-based architectures/frameworks for NoC systems;
- DL-based technologies (routers/PEs) for routing protocols in NoC systems;
- DL-based routing services for specific applications of NoC systems (Multicast, unicast, etc.);
- DL-based network topology design for NoC architectures;
- DL-based routing protocols for NoC systems;
- DL-based energy efficient routing protocols for NoC systems;
- DL-based mapping algorithms for NoC systems;
- DL-based network floorplanning algorithms for NoC systems;
- DL-based wireless NoC (WNoC) architectures/frameworks (partially/fully wireless network);





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Message from the Editor-in-Chief

Electronics is a multidisciplinary journal designed to appeal to a diverse audience of research scientists, practitioners, and developers in academia and industry. The journal is devoted to fast publication of latest technological breakthroughs, cutting-edge developments, and timely reviews of current and emerging technologies related to the broad field of electronics. Experimental and theoretical results are published as regular peer-reviewed articles or as articles within Special Issues guest-edited by leading experts in selected topics of interest.

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