

Special Issue

Design and Implementation of Reconfigurable Optoelectronic Integrated Chips

Message from the Guest Editor

Reconfigurable optoelectronic integrated chips (ROEICs) have been the subject of much interest in recent years due to their potential applications in artificial intelligence (AI) and optical communication systems. This Special Issue is chiefly concerned with the following aspects of ROEICs: 3D ROEICs, silicon photonics, co-packaged optics (CPO), reconfigurations in optical neural networks (ONNs), sensing, integrated storage and computing chips, the reconfigurability of nonlinear activation functions, and other related topics. The details of each topic will be briefly introduced in the following paragraphs. This Special Issue aims to highlight advances in the development, modeling, simulation, and implementation of ROEICs, from the component device level to that of complete systems.

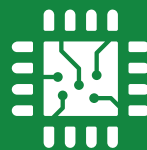
Guest Editor

Dr. Jiyuan Zheng

Beijing National Research Center for Information Science and Technology, Tsinghua University, Beijing 100084, China

Deadline for manuscript submissions

31 December 2025



Chips

an Open Access Journal
by MDPI



mdpi.com/si/239725

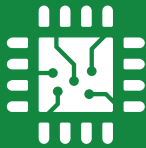
Chips

Editorial Office
MDPI, Grosspeteranlage 5
4052 Basel, Switzerland
Tel: +41 61 683 77 34
chips@mdpi.com

mdpi.com/journal/

[chips](https://mdpi.com/journal/chips)





Chips

an Open Access Journal
by MDPI



[mdpi.com/journal/
chips](https://mdpi.com/journal/chips)



About the Journal

Message from the Editor-in-Chief

Chips is a new journal with the aim to become a leading reference on all aspects of the IC domain. The journal is devoted to publishing rigorously peer-reviewed articles (such as original research, reviews, and communications) with the specific target to disseminate novelties in terms of research and knowledge as well as the most advanced state of the art on IC technologies, design, testing, and production. The journal offers the opportunity to actively spread new concepts and advancements in the IC domain and its increasing interrelated and multidisciplinary areas in a timely manner. More specifically, the journal will cover chip design, including CAD tools, chip production, and their wide spectrum of applications.

Editor-in-Chief

Prof. Dr. Gaetano Palumbo
Dipartimento di Ingegneria Elettrica Elettronica e Informatica,
Università di Catania, I-95125 Catania, Italy

Author Benefits

Open Access:

free for readers, with article processing charges (APC) paid by authors or their institutions.

Rapid Publication:

manuscripts are peer-reviewed and a first decision is provided to authors approximately 23.3 days after submission; acceptance to publication is undertaken in 4.2 days (median values for papers published in this journal in the first half of 2025).

Recognition of Reviewers:

APC discount vouchers, optional signed peer review and reviewer names are published annually in the journal.