

Special Issue

Low-Power IC Design for Efficient AI

Message from the Guest Editors

This Special Issue seeks to highlight cutting-edge research and practical innovations in low-power integrated circuit design specifically tailored for AI applications.

- Circuit-Level Innovations

- Ultra-low-voltage logic and memory architecture.
- Dynamic voltage and frequency scaling (DVFS) for AI accelerators.
- Novel transistor technologies and device-level optimizations.

- Architecture and System Design

- Specialized hardware for neural networks (TPUs, NPUs, neuromorphic chips).
- Power-aware datapath design for machine learning inference.
- Memory hierarchies optimized for AI workloads.

- Design Methodologies

- Low-power design techniques for deep learning accelerators.
- Trade-offs between accuracy, latency, and energy consumption.
- Quantization and sparsity exploitation at the silicon level.

- Application-Specific Solutions

- Edge AI processors for IoT and wearables.
- Energy-efficient training circuits.
- Multi-modal AI SoCs with heterogeneous computer cores.

- Measurement, Characterization, and Analysis

Guest Editors

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Message from the Editor-in-Chief

As the world of science becomes ever more specialized, researchers may lose themselves in the deep forest of the ever increasing number of subfields being created. This open access journal *Applied Sciences* has been started to link these subfields, so researchers can cut through the forest and see the surrounding, or quite distant fields and subfields to help develop his/her own research even further with the aid of this multi-dimensional network.

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