Special Issue

Recent Advances in Microelectronics Fabrication and Packaging

Message from the Guest Editors

New innovations are needed both in the electronic transistor space and in advanced packaging. Non-silicon materials, such as III-V, 2D materials, etc., are also to be explored for next-generation transistors. These new transistors require vastly different microelectronic processing steps of lithography, etching, and deposition, which remain to be developed. In the advanced packaging space, newer packaging technologies such as Fan-Out Wafer-Level Packaging (FOWLP) and Wafer-scale die-let assembly though TCB/Hybrid bonding are currently being explored and commercialized. The combination of novel transistor manufacturing with advanced packaging will enable continued Moore's law scaling of computational performance for future applications. This Special Issue aims to focus on recent advances in both microelectronic fabrication for next-generation transistors and their interconnects as well as advanced packaging.

Guest Editors

Dr. Goutham Ezhilarasu
CHIPS, University of California, Los Angeles, CA, USA

Prof. Dr. Subramanian S. Iyer
CHIPS, University of California, Los Angeles, CA, USA

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Editorial Office
MDPI, Grosspeteranlage 5
4052 Basel, Switzerland
Tel: +41 61 683 77 34
applsci@mdpi.com

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As the world of science becomes ever more specialized, researchers may lose themselves in the deep forest of the ever increasing number of subfields being created. This open access journal Applied Sciences has been started to link these subfields, so researchers can cut through the forest and see the surrounding, or quite distant fields and subfields to help develop his/her own research even further with the aid of this multi-dimensional network.

Editor-in-Chief

Prof. Dr. Giulio Nicola Cerullo
Dipartimento di Fisica, Politecnico di Milano, Piazza L. da Vinci 32,
20133 Milano, Italy

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