Supporting Information

Design and construction of a new plasma applicator for the improved disinfection and activation of large surfaces

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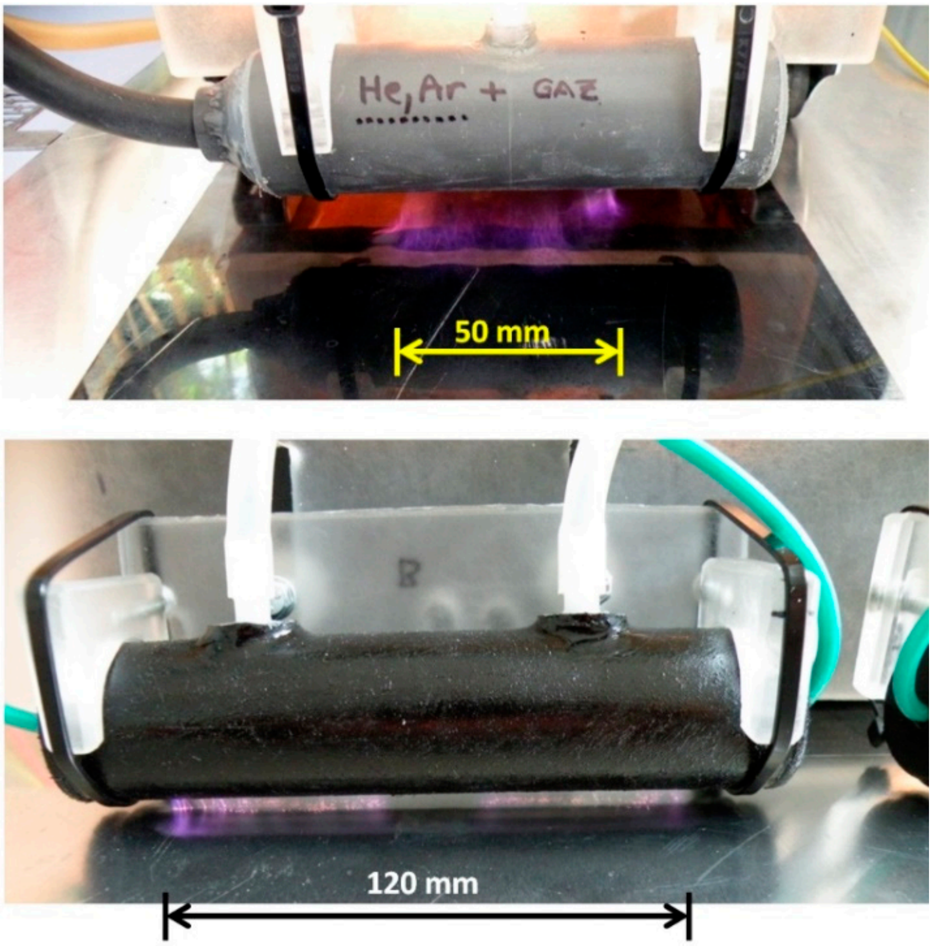

Figure S1. Laboratory made plasma applicators (50 mm and 120 mm versions)

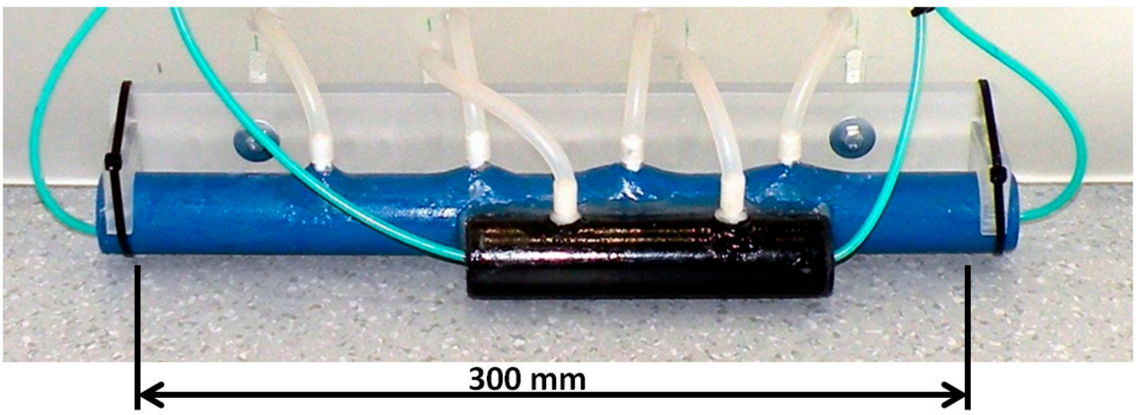

Figure S2. Laboratory made plasma applicator, 300 mm width version

Plasma operational stability diagram drawing algorithm:

The information required for drawing the stability diagram is collected from visual observations made on the physical aspect/appearance of the plasma discharge. We write down, and we take pictures of the visual characteristics of the discharge as a function of the input voltage/power and feed gas flow rates. When plasma discharge is first initiated, we quickly set the necessary conditions (gas flow & input voltage) to form a stable discharge. At this time, for a given fixed value of the power supply voltage, we change the feed gas flow rate (increase or decrease) and we note down the observations regarding the appearance of the plasma discharge (its shape, size, tendency, color, etc.). Then we select a new voltage value and the gas flow rates are again varied as mentioned above. In a similar manner, we keep a constant value of the feed gas flow rate and we modify the supply voltage, again writing down the plasma discharge physical parameters.

The obtained values which correspond to similar plasma evolution stages will define basically the same given region on the stability diagram. We name this region after the main parameter of the plasma discharge which is similar for the two cases (i.e. color, shape, breakdown voltage, etc.).

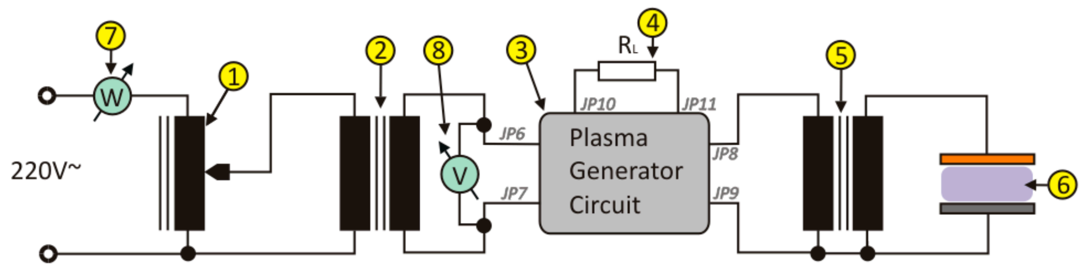

Figure S3.The connection setup of our entire plasma generation system we used in this article

The notations on Figure S3 refer to the following components:
(1) - variable autotransformer (variac) , (2) – mains isolation transformer, (3) – plasma generation circuit from Figure 4, (4) – power limiting resistor , (5) – high voltage output transformer,
(6) – plasma applicator, (7) – wattmeter, (8) – voltmeter.

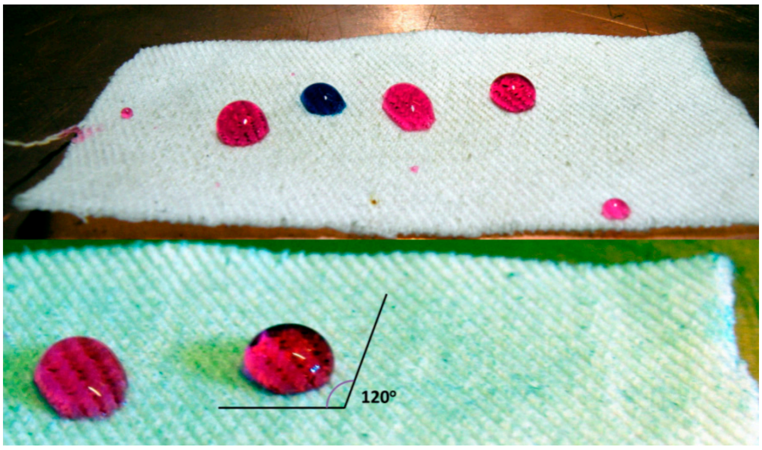

Figure S4. Hydrophobic cotton fabric after plasma treatment, 50W @ 5l/min, He:O_2 mixture (70:30), 30 seconds treatment time

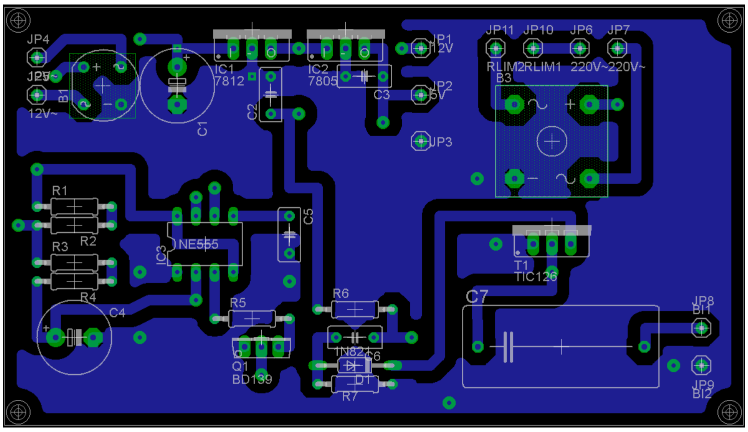

Figure S5. The bottom layer of the PCB of the plasma generator circuit (1:1 scale)

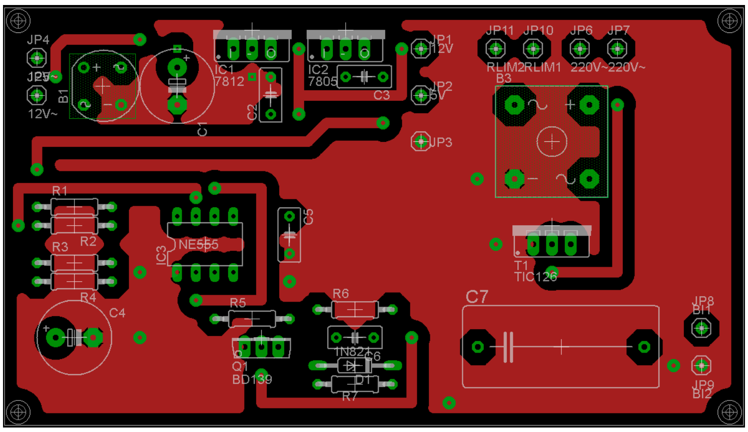

Figure S6. The top layer of the PCB of the plasma generator circuit (1:1 scale)

Description of the plasma generating circuit from Figure 2:

As you can see on Figure 2, the entire circuit is almost self-explanatory: the low voltage power supply part contains just a rectifier bridge (*B1*) and two linear regulator circuits (*IC1* and *IC2*) which provide two output voltage levels +5V and +12V which feed the drive signal generating module. This module is based on the trusted and well known 555 timer I.C (*IC3*) configured in the astable oscillator mode with the frequency being set by the values of the components: *R1*, *R2*, *R3*, *R4* and *C4*, according to the equation:

$$f = \frac{1.44}{[(R1+R2)+2(R3+R4)]\cdot C} \text{ [Hz]} \qquad \text{(SI\_1)}$$

The output square wave signal from *IC3* is fed to the base of the transistor *Q1* which has the job to form the drive impulse signal which commands the thyristor *T1* from the high voltage generating module. This circuit works in the following way: an AC voltage (0...240V~) is fed to the connectors JP6 and JP7 from an auxiliary variac transformer, and gets rectified to pulse DC by the diode bridge *B3*. This DC voltage then charges the capacitor *C7*. When the output square wave signal on the pin 3 of *IC3* is in high state, the transistor *Q1* is in conduction mode and thus the voltage value on its collector terminal is very low (< 0.3V), so in this situation we have no drive impulse on the gate terminal of the thyristor *T1*. When the signal on the base of *Q1* becomes 0 logic, the transistor *Q1* is blocked, which means that the voltage at the connection point of *R6* and *C6* becomes high (12V). In this moment the capacitor *C6* is rapidly charged through *R6* and this rapid variation of its voltage generates a firing impulse which drives the gate terminal of the thyristor *T1* through the diode *D1*. In this moment the thyristor *T1* discharges the high voltage stored in the capacitor *C7* on the primary winding of the high voltage transformer connected to the pins *JP8* and *JP9*. This is the way the high voltage impulses are generated with this circuit.

Now if we think about plasma generation, the circuit described above is very advantageous from many points of view, but mainly because the capacitive discharge mode gives us a great control of the absorbed power in the plasma discharge, by simply controlling the input voltage at the connectors *JP6* and *JP7*, the discharged energy to the plasma being given by the equation:

$$E_p = \frac{U^2 C}{2} \text{ [J]} \qquad \text{(SI\_2)}$$

where *U* is the peak voltage on the charged capacitor *C* (*C7*).

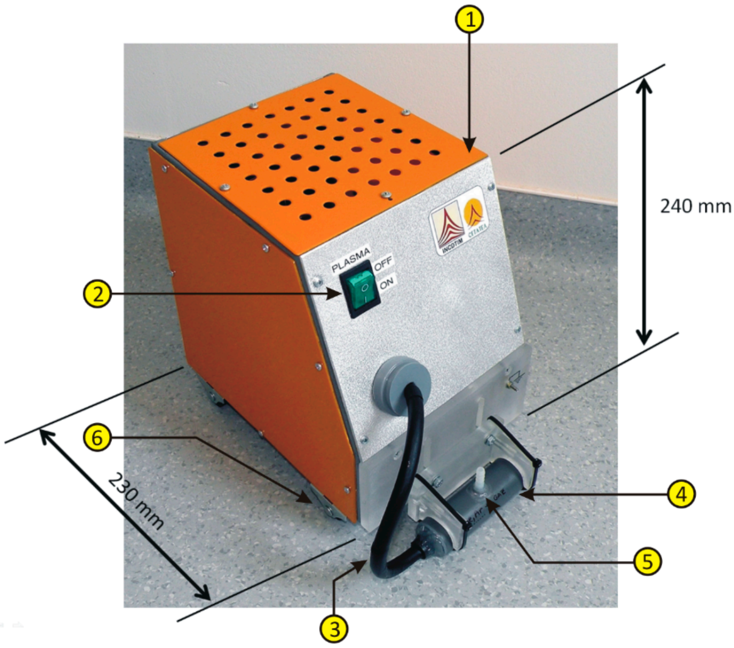

Figure S7. Our portable/demonstration unit with a single plasma applicator, (50 mm treatment width)

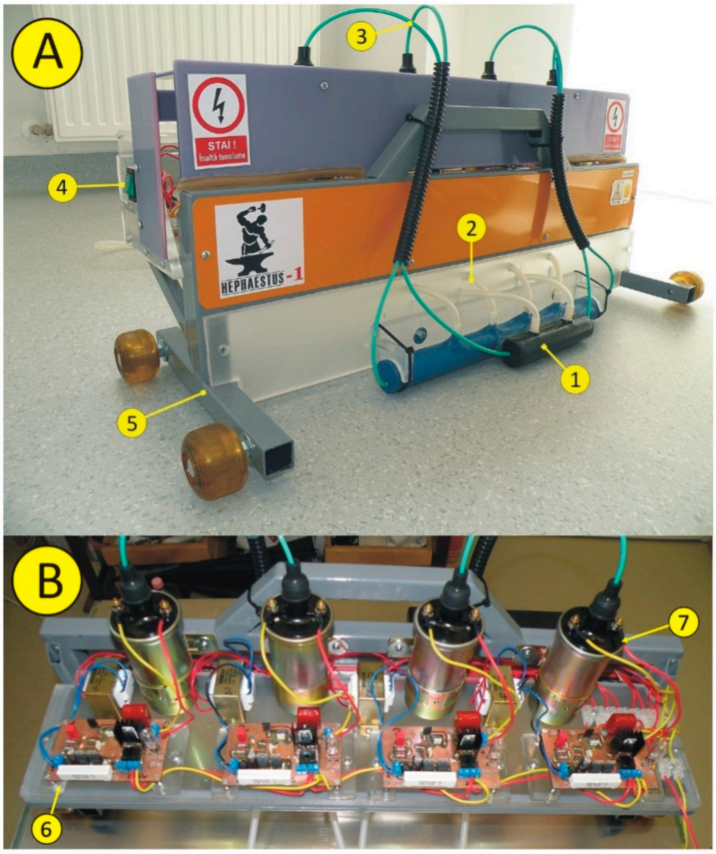

Figure S8. Our larger, laboratory level plasma generator with a treatment width of 300 mm

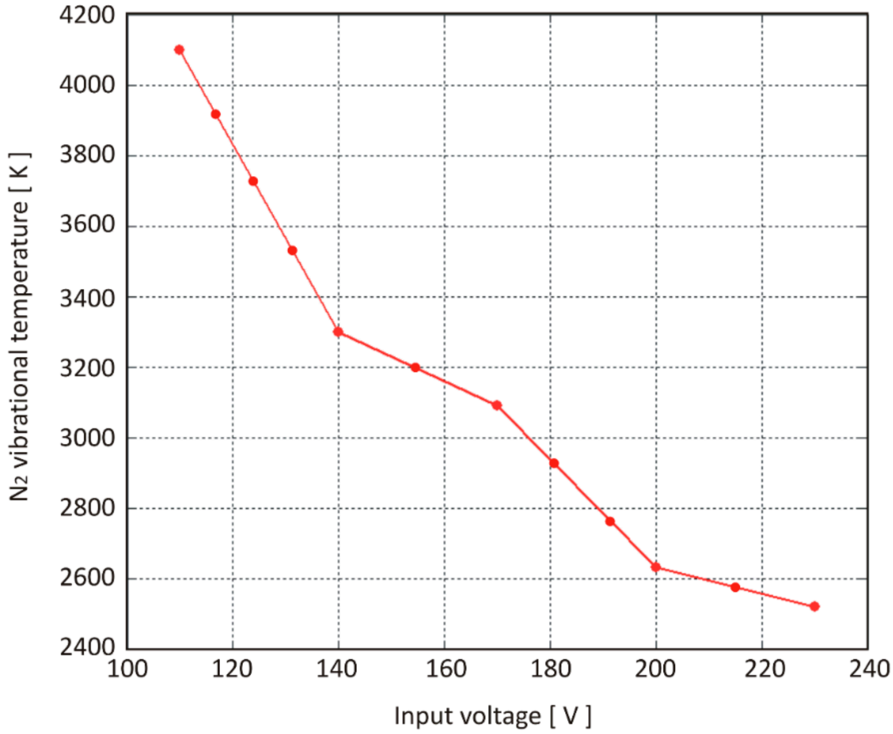

Figure S9. The variation of the N_2 ionic vibrational temperature as a function of the input voltage (for our 50 mm wide cold plasma applicator)

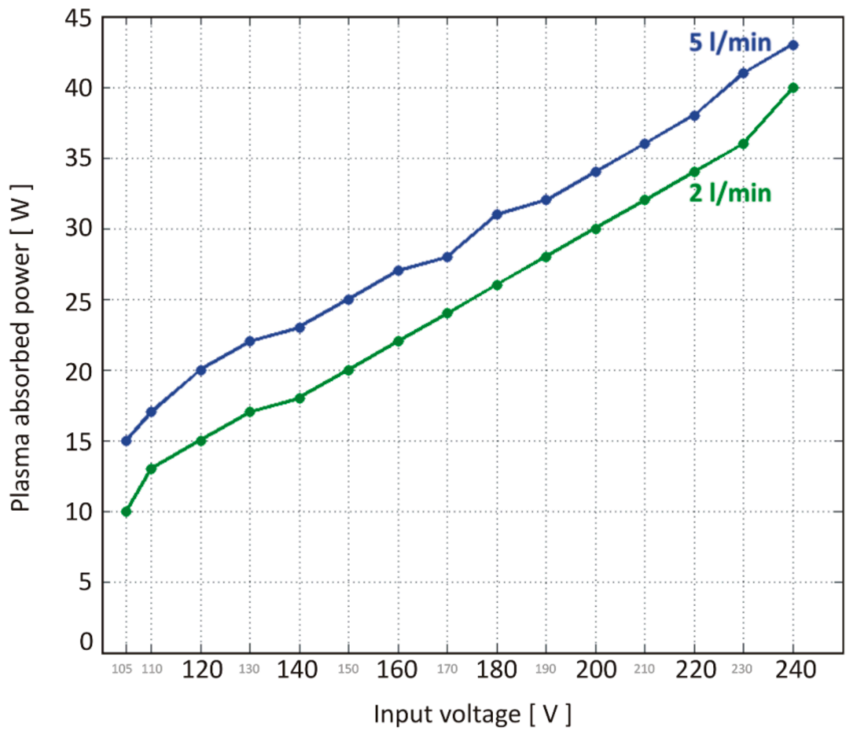

Figure S10. The variation of the plasma absorbed power as a function of the input supply voltage (for our 50 mm wide cold plasma applicator)

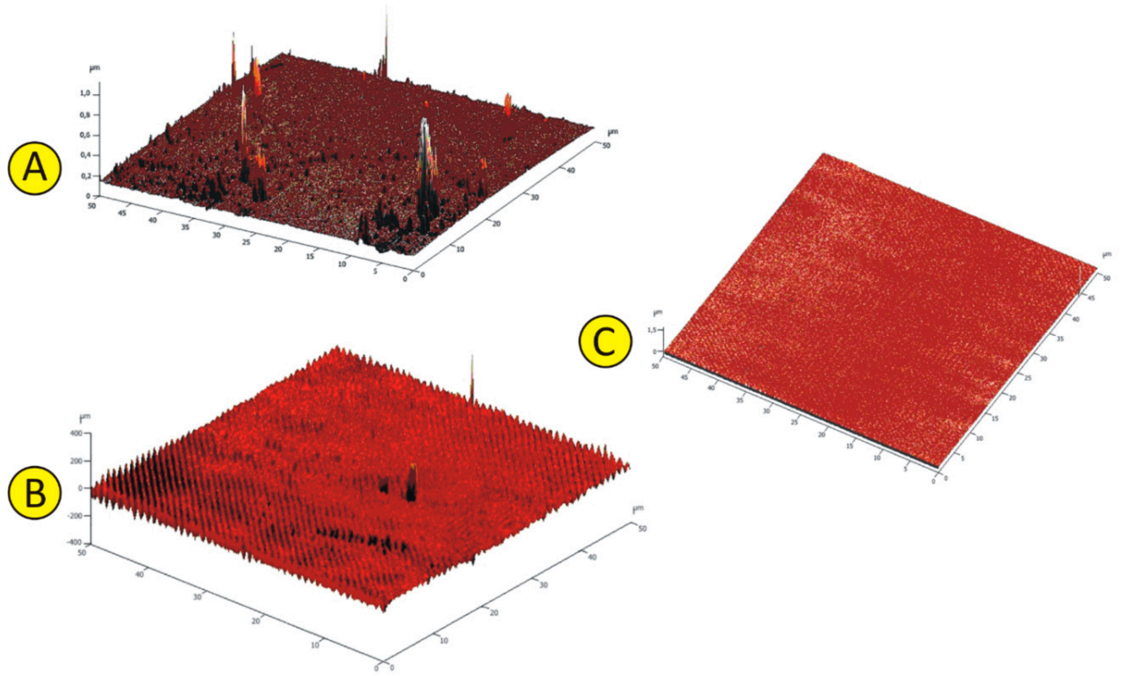

Figure S11. AFM glass surface morphology pictures of untreated glass (A), after 5 seconds of plasma treatment (B) and after 5 minutes of plasma treatment (C), @ 50W input power

The surface roughness of the untreated and plasma treated glass was examined at ambient temperature by atomic force microscopy (AFM) with a NT-MDT NTEGRA Spectra microscope.