materials

MDPI

Supplementary Materials

Threshold-Voltage Extraction Methods for Atomically Deposited Disordered ZnO Thin-Film Transistors

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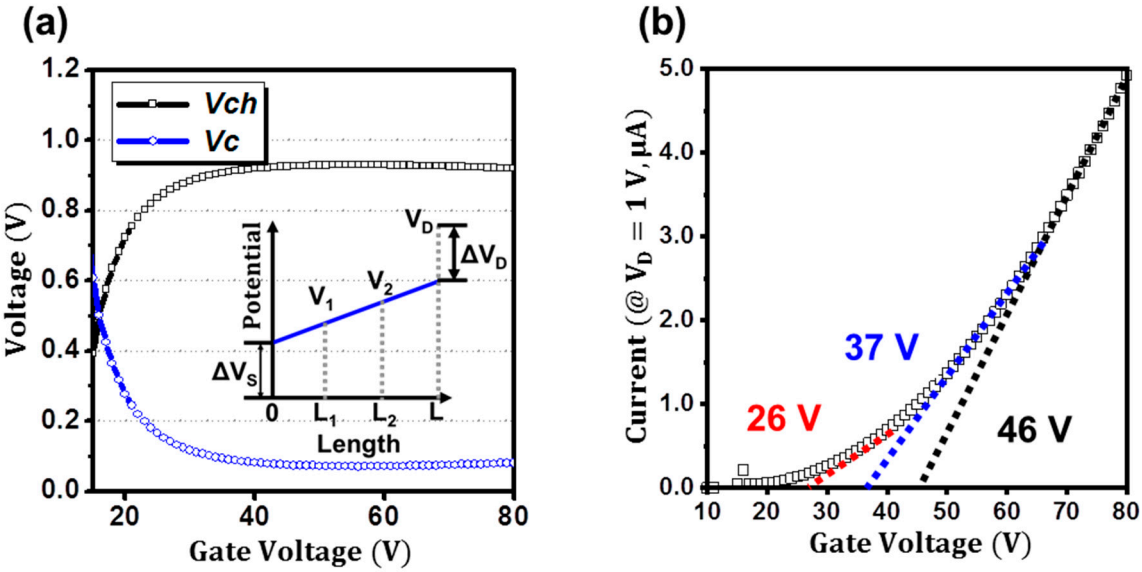

Figure S1. (a) Potential distribution of the ZnO TFTs with a four-point probe configuration. Inset: Schematic illustration of the four-point probe method. (b) The threshold voltage extraction using the intrinsic current–voltage characteristics with the gate bias range of 40 (red), 60 (blue), and 80 V (black).

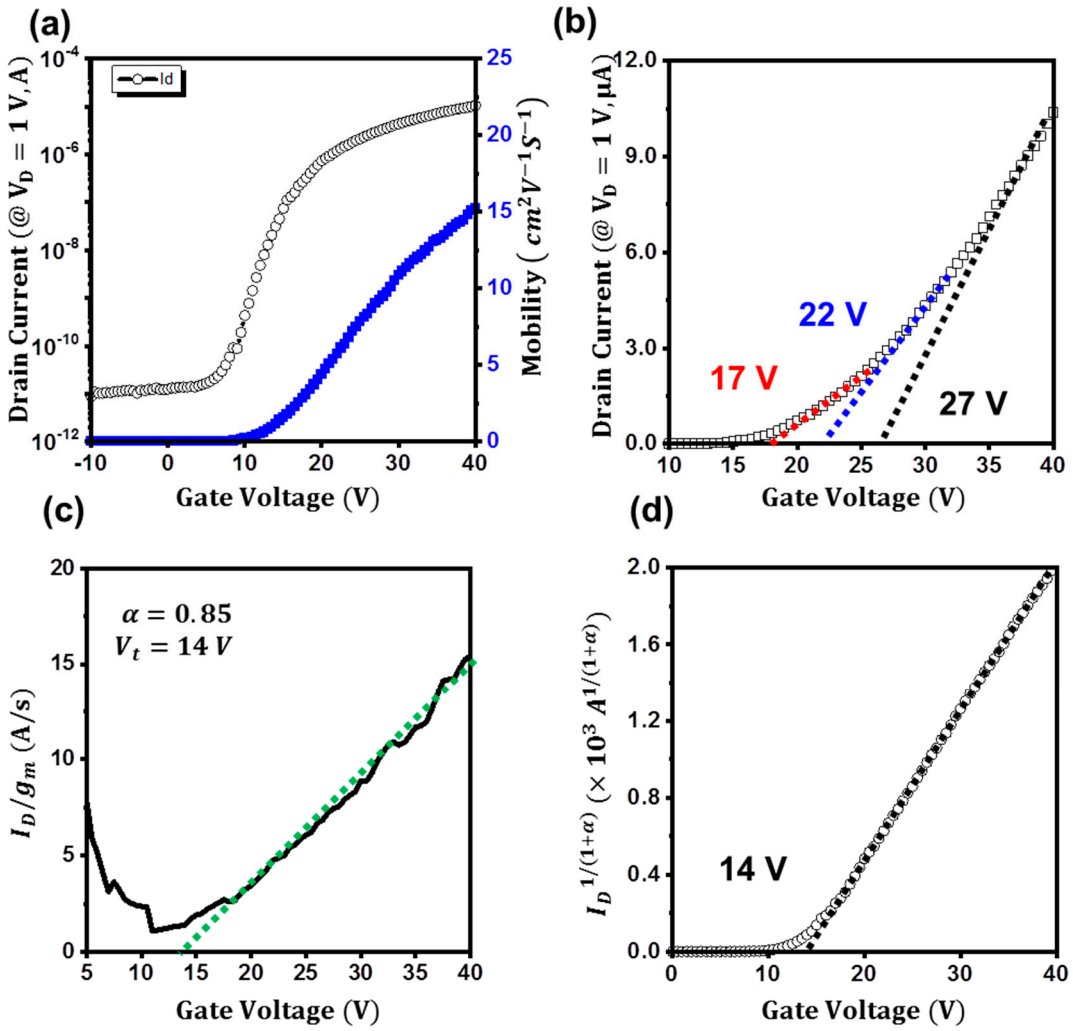

Figure S2. (a) Transfer characteristics (I_{ds} vs. V_{gs}) of the IGZO TFTs. (b) The threshold voltage extraction of the IGZO FET with the gate bias range of 25 (red), 30 (blue), and 40 V (black). (c) The modified plot of *Ids*/*gm* for the IGZO TFTs. (d) The modified threshold voltage extraction of the IGZO TFTs.