Supplementary Materials for «Neurosynaptic core prototype for memristor crossbar arrays diagnostics»

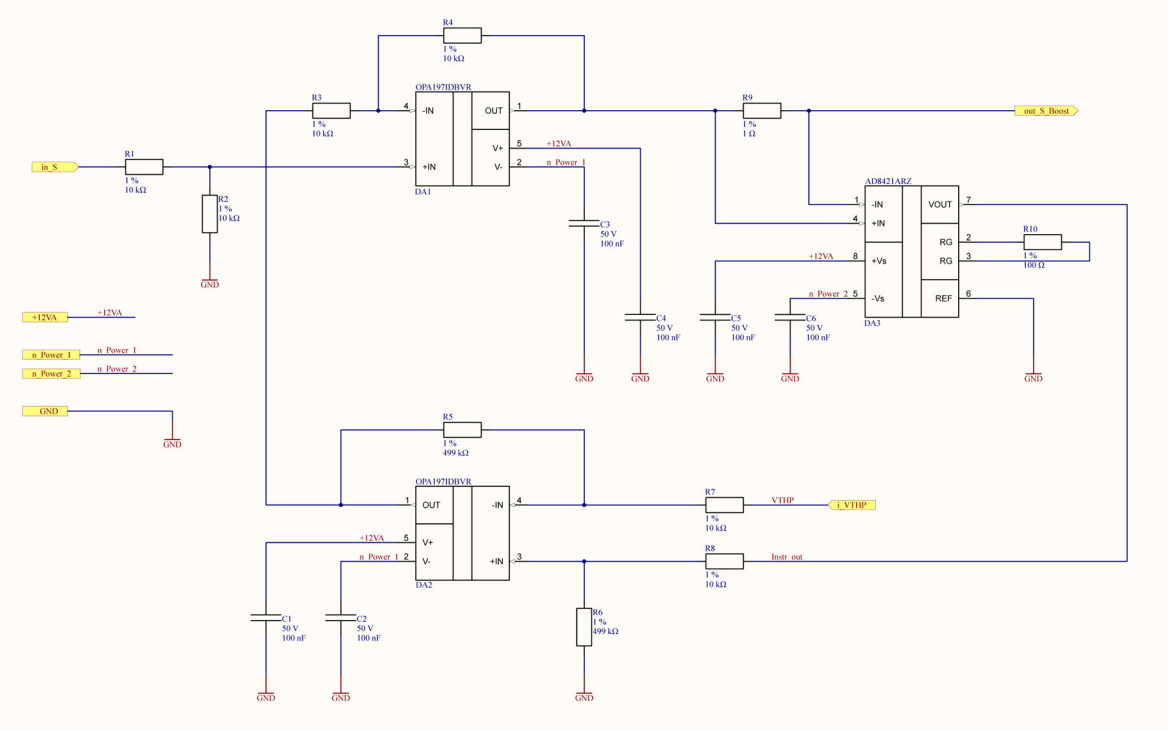

Figure S1. Final schematic of the current control module, designed in the Altium Designer CAD environment (version 23.8.1).

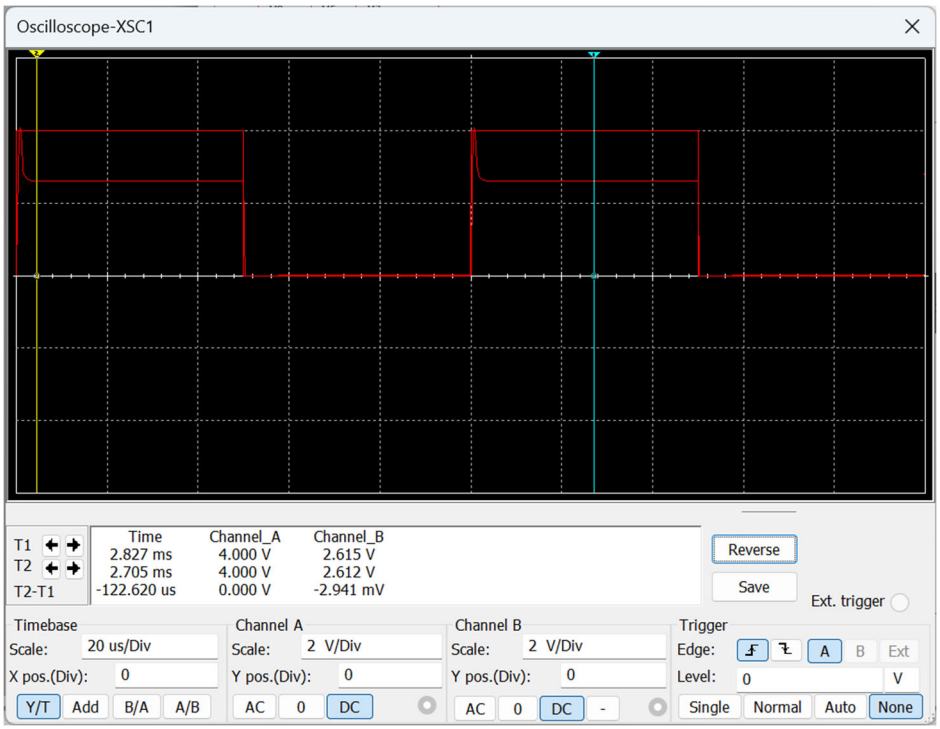

Figure S2. A screenshot of the current control module simulation within the NI Multisim environment (National Instruments, Austin, TX, USA) version 14.2. The simulation validated the module's performance under the following test conditions: a 4 V input pulse, a 500 Ω load resistor, and a current threshold set to 5 mA (via a 0.5 V control voltage).

The measured voltage of 2.6 V across the load resistor corresponds to a regulated current of 5.2 mA, confirming proper circuit operation.

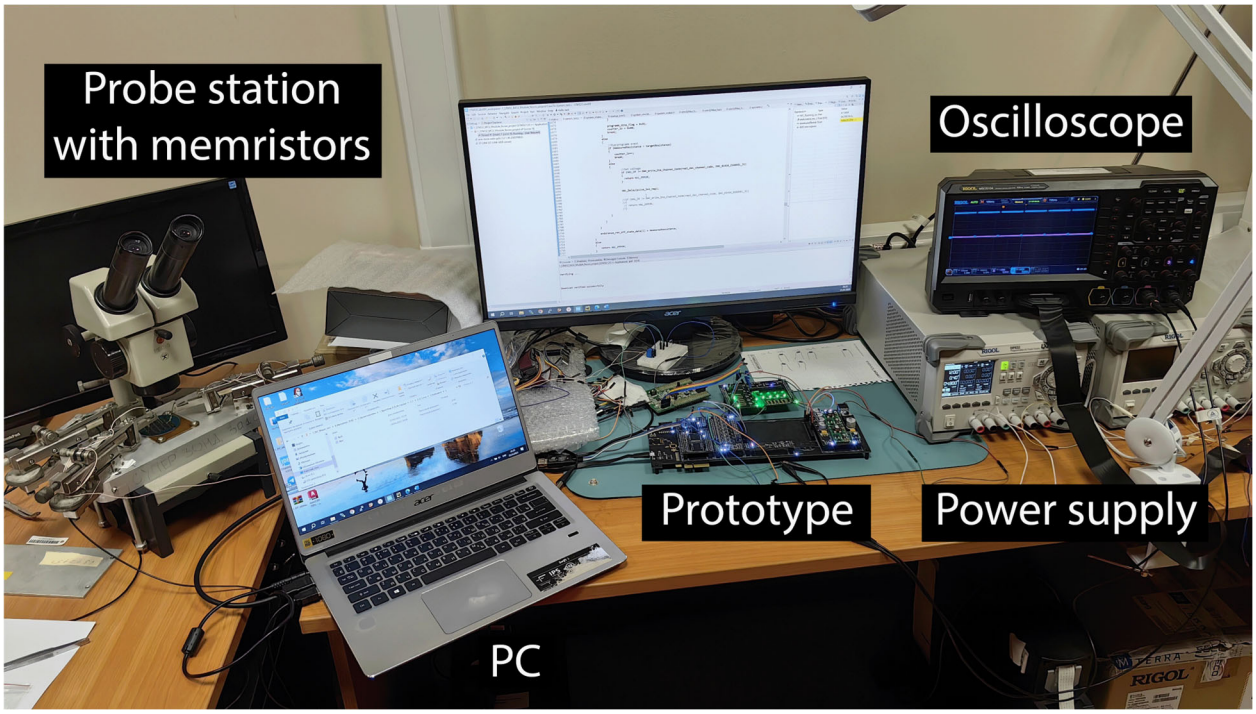

Figure S3. Neurosynaptic core prototype test bench configuration. A probe station interfaced with the memristors, with DAC control signals visualized on a Rigol MSO5104 oscilloscope and a Rigol DP832 unit powering the system (from Rigol Technologies, Suzhou, China).

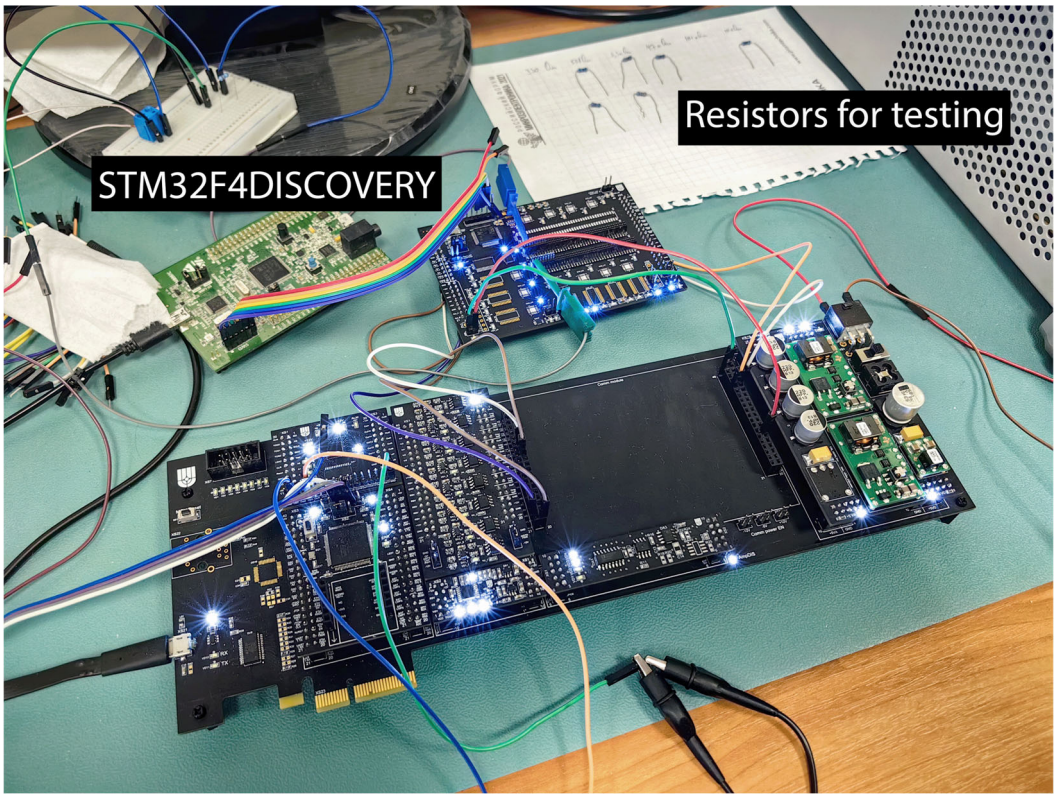

Figure S4. Testing the switching module operation. Two STM32CubeIDE (version 1.14.1) projects were run: for the switching module's microcontroller and the core's main controller. They were debugged using the built-in ST-LINK of

the STM32F4DISCOVERY board and a standalone ST-LINK/V2, respectively (all software and hardware from STMicroelectronics, Geneva, Switzerland). A set of precision resistors used for validating the conductance measurement accuracy is also shown.

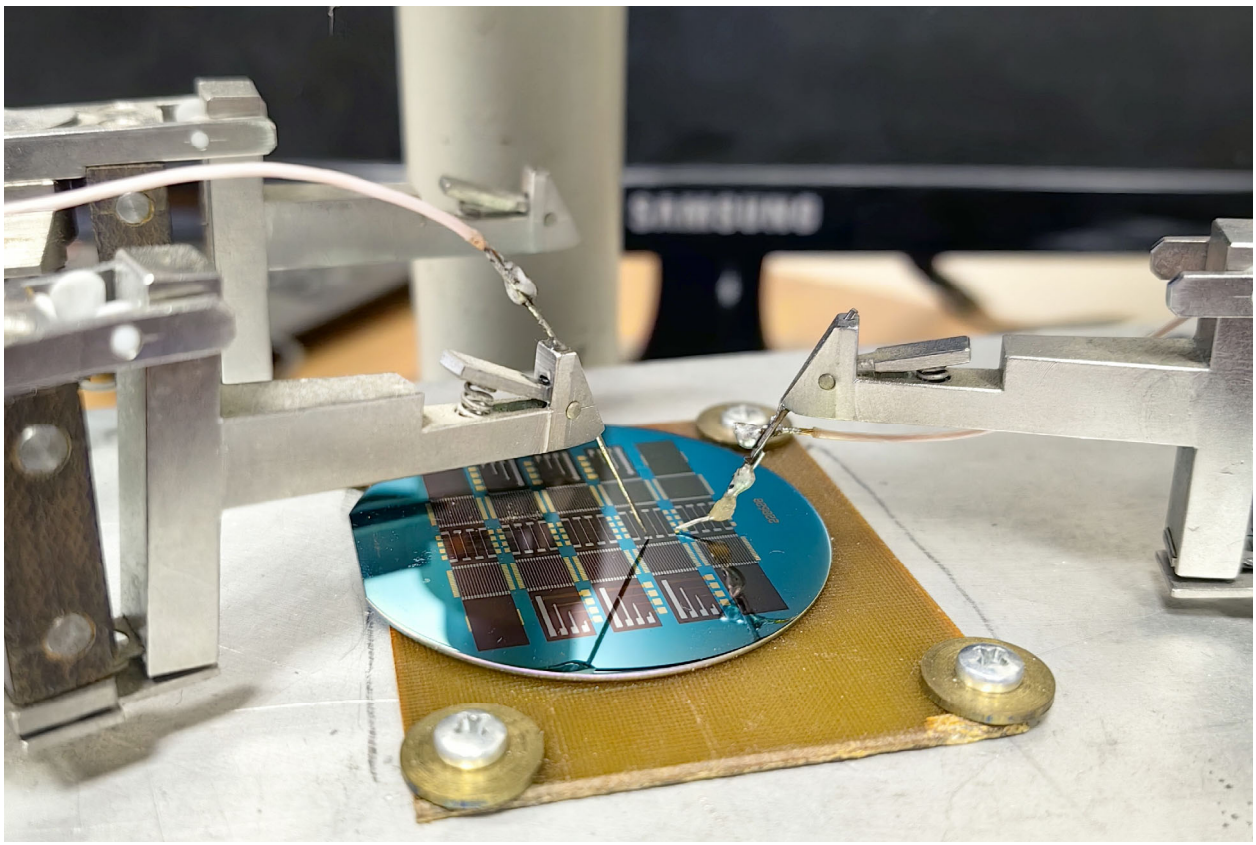

Figure S5. Memristor structures used in the study, mounted in the probe station.