Supplementary Material

for "A Wideband Hybrid Envelope Tracking Supply Modulator with Slew-Rate-Enhanced Linear Amplifier"

AC analysis of the linear amplifier (LA) with the proposed SRE circuit

The proposed LA circuit, which is shown in Figure 5 in our manuscript, is shown as Figure 1. Some necessary labels like voltage node names and transistor names have been added for convenience to aid the AC analysis.

1. The small-signal model of the proposed SRE circuit

The SRE circuit in Figure 1(b) can be extracted to a corresponding small-signal model, as shown in Figure 2. In the small-signal models below, unless otherwise specified, g_{mi}, R_{Oi} and C_i are used to represent the transconductance g_m, output resistance r_{ds}, and output capacitance C_d of transistor Mi, respectively, where i denotes the subscript of the transistor.

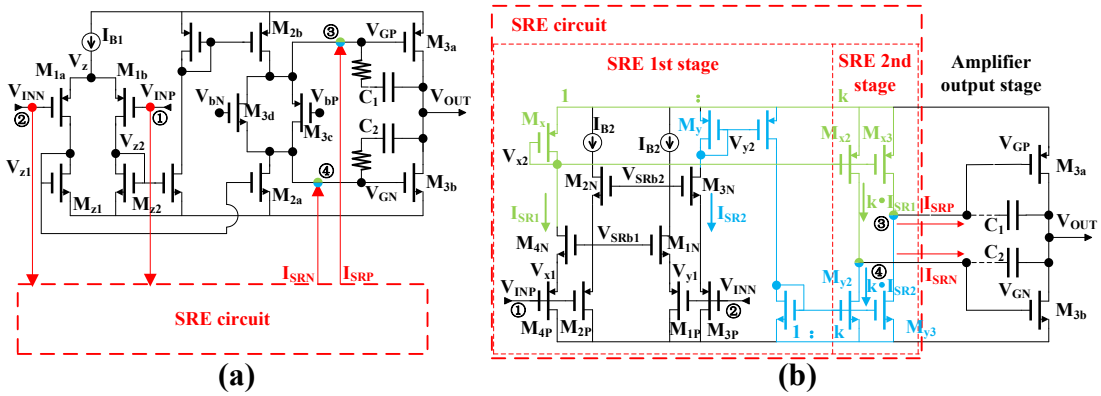


Figure 1. The proposed LA circuit: **(a)** the entire LA circuit; **(b)** the proposed SRE circuit.

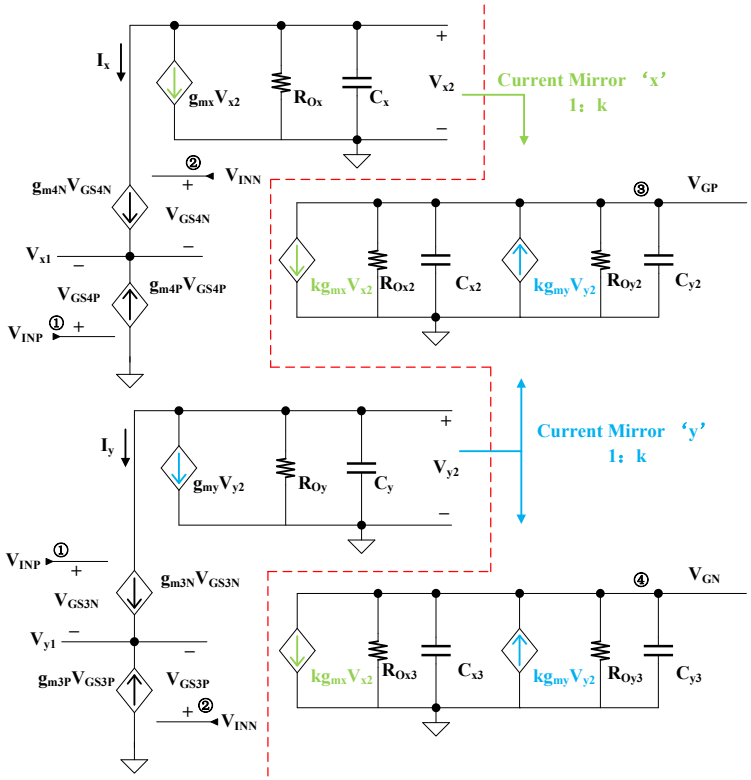


Figure 2. A small-signal model of SRE circuit.

At the top of Figure 2, the left side of the SRE circuit's input stage from Figure 1(b) is displayed. We can obtain the following equations:

$$I_x = g_{m4N}(V_{INN} - V_{x1}) = -g_{m4P}(V_{INP} - V_{x1}) \tag{1}$$

and

$$-I_x = g_{mx}V_{x2} + V_{x2}\frac{1}{R_{Ox}} + V_{x2}C_x s \tag{2}$$

We can simplify Equation (1) and Equation (2) by eliminating V_{x1} and I_x:

$$V_{x2} = \frac{1}{g_{mx} + \frac{1}{R_{Ox}} + C_x s}\frac{g_{m4P}g_{m4N}}{g_{m4P} + g_{m4N}}(V_{INP} - V_{INN}) \tag{3}$$

Note that in the current mirror 'x', $g_{mx}R_{Ox} >> 1$ and $f_T = \frac{g_{mx}}{2\pi C_x} >> f$, where f represents the frequency we are concerned with. So, we can further simplify Equation (3) as follows:

$$V_{x2} = \frac{1}{g_{mx}}\frac{g_{m4P}g_{m4N}}{g_{m4P} + g_{m4N}}(V_{INP} - V_{INN}) \tag{4}$$

Actually, C_x includes the C_{gs} of all the transistors in this current mirror (including M_x, M_{x2} and M_{x3}). For the sake of calculation convenience, we have omitted this pole, which

can be expressed as $\frac{g_{mx}}{(1+2k)C_{gsx}}$. We will adjust it separately when it arises during the later simulation and analysis. In the same way, we can calculate the expression of V_{y2}:

$$V_{y2} = \frac{1}{g_{my}} \frac{g_{m3P} g_{m3N}}{g_{m3P} + g_{m3N}} (V_{INN} - V_{INP}) \tag{5}$$

After the amplification of the current mirrors, the SRE current injected into the gate in the output stage can be expressed as $kg_{my}V_{y2}$-$kg_{mx}V_{x2}$. Due to the symmetrical design of the circuit, $g_{m3P} = g_{m4P}$ and $g_{m3N} = g_{m4N}$. Then, we can simplify the SRE circuit's small-signal model shown in Figure 3. The parameters g_{mSR}, R_{OSRP}, R_{OSRN}, C_{SRGP} and C_{SRGN} are shown below:

$$\begin{cases} g_{mSR} = 2k \dfrac{g_{m3P} g_{m3N}}{g_{m3P} + g_{m3N}} \\ R_{OSRP} = R_{Ox2} \parallel R_{Oy2}, R_{OSRN} = R_{Ox3} \parallel R_{Oy3} \\ C_{SRP} = C_{x2} + C_{y2}, C_{SRN} = C_{x3} + C_{y3} \end{cases} \tag{6}$$

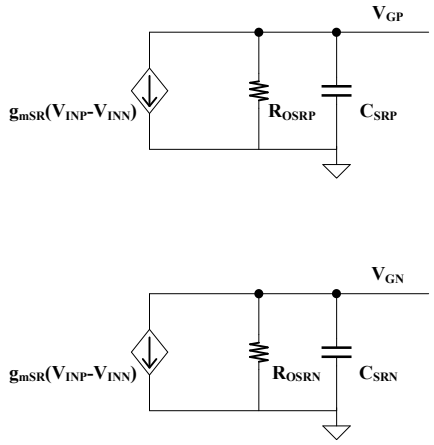


Figure 3. A simplified SRE circuit's small-signal model.

2. The input stage of the LA

When it comes to the other part of the proposed LA shown in Figure 1(a), we discuss the input stage first. We incorporate the SRE circuit model shown in Figure 3 into the input stage circuit; then, we will obtain the small-signal model of the LA's input stage, shown as Figure 4. From this, the following can be observed:

$$\begin{cases} -I_{in1N} = g_{m1a}(V_{INN} - V_z) \\ g_{m1a}(V_{INN} - V_z) = -g_{m1b}(V_{INP} - V_z) \\ -I_{in1P} = g_{m1b}(V_{INP} - V_z) \end{cases} \tag{7}$$

The currents I_{in1N} and I_{in1P} are injected into the current mirror 'za' and 'zb'.

$$\begin{cases} I_{in1N} = g_{mz1}V_{z1} + V_{z1}\dfrac{1}{R_{Oz1}} + V_{z1}C_{z1}s \\ I_{in1P} = g_{mz2}V_{z2} + V_{z2}\dfrac{1}{R_{Oz2}} + V_{z2}C_{z2}s \end{cases} \tag{8}$$

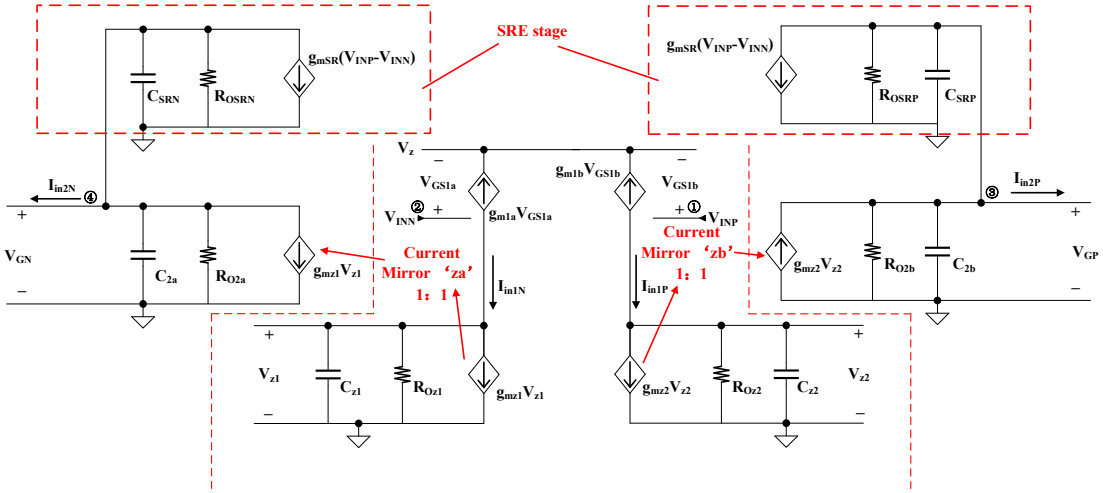


Figure 4. A small-signal model of the proposed LA's input stage.

As with the previously discussed current mirror 'x', disregarding the effect of mirror poles, we can obtain the following equations:

$$\begin{cases} V_{z1} = \dfrac{I_{in1N}}{g_{mz1} + \dfrac{1}{R_{Oz1}} + C_{z1}s} \approx \dfrac{I_{in1N}}{g_{mz1}} \\ V_{z2} = \dfrac{I_{in1P}}{g_{mz2} + \dfrac{1}{R_{Oz2}} + C_{z2}s} \approx \dfrac{I_{in1P}}{g_{mz2}} \end{cases} \tag{9}$$

By combining Equation (7) and Equation (9), we obtain the following:

$$\begin{cases} g_{mz1}V_{z1} = \dfrac{g_{m1a}g_{m1b}}{g_{m1a} + g_{m1b}}(V_{INP} - V_{INN}) \\ g_{mz2}V_{z2} = \dfrac{g_{m1a}g_{m1b}}{g_{m1a} + g_{m1b}}(V_{INN} - V_{INP}) \end{cases} \tag{10}$$

By combining the output of current mirror 'za', 'zb' and the SRE circuit, we can simplify the small-signal model of the input stage as Figure 5. The parameters g_{m1}, R_{O1P}, R_{O1N}, C_{1P} and C_{1N} are shown below:

$$\begin{cases} g_{m1} = g_{mSR} + g_{m1Conv} = 2k\dfrac{g_{m3P}g_{m3N}}{g_{m3P} + g_{m3N}} + \dfrac{g_{m1a}g_{m1b}}{g_{m1a} + g_{m1b}} \\ R_{O1P} = R_{OSRP} \parallel R_{O2b}, R_{O1N} = R_{OSRN} \parallel R_{O2a} \\ C_{1P} = C_{SRP} + C_{2b} + C_{gs3a}, C_{1N} = C_{SRN} + C_{2a} + C_{gs3b} \end{cases} \tag{11}$$

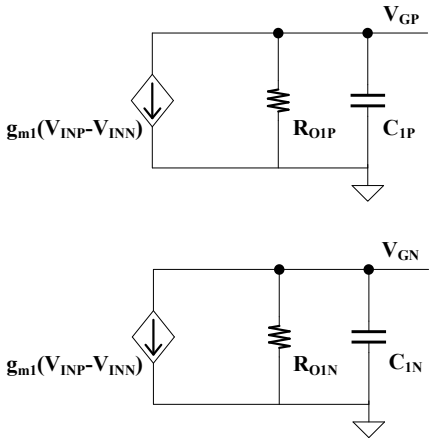


Figure 5. A small-signal model of the input stage of LA.

3.The output stage of the LA

The output stage of the proposed LA is shown in Figure 6(a). The transistors M_{3e} and M_{3f} form the bias circuit for V_{bN}, and together with M_{3d} and M_{3b}, they constitute a translinear loop, which sets the quiescent current through the output transistor M_{3b}. Similarly, M_{3e} and M_{3f} have the same function: to set the quiescent current through the output transistor M_{3a}. The small-signal model of M_{3d} and M_{3c} is shown in Figure 6(b). The impedance Z_{TL} includes the resistance and capacitance between V_{GP} and V_{GN}.

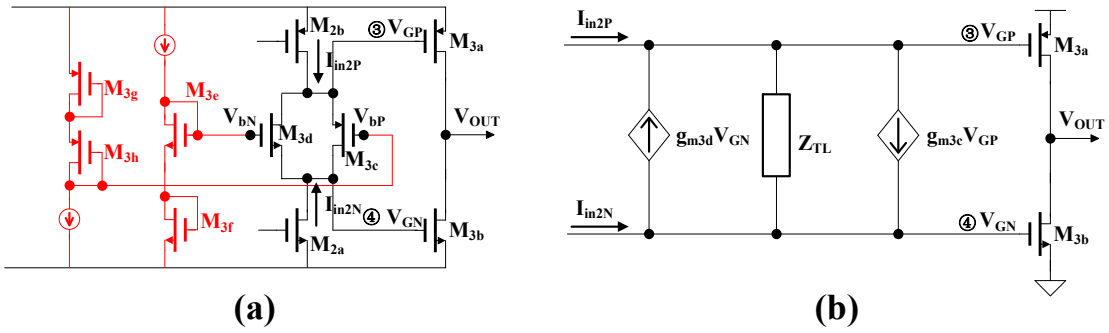


Figure 6. The output stage of the proposed LA: (a) the bias of V_{bN} and V_{bP}; (b) the small-signal model of M_{3d} and M_{3c}.

4. The small-signal model of the entire LA

Then, we can incorporate the input stage and output stage together, and we will obtain the small-signal model of the entire LA, shown as Figure 7. Note that this circuit has strong symmetry; we designed it with the intention of achieving a symmetrical circuit. We calculate the KCL (Kirchhoff's Current Law) equations of node ③ and ④ as follows:

$$\begin{cases} g_{m1}(V_{INP}-V_{INN})+V_{GP}\left(\frac{1}{R_{O1P}}+C_{1P}s\right)+g_{m3c}V_{GP}-g_{m3d}V_{GN}+\frac{1}{Z_{TL}}(V_{GP}-V_{GN})+\frac{V_{GP}-V_{OUT}}{R_1+1/C_1s}=0 \\ g_{m1}(V_{INP}-V_{INN})+V_{GN}\left(\frac{1}{R_{O1N}}+C_{1N}s\right)+g_{m3d}V_{GN}-g_{m3c}V_{GP}+\frac{1}{Z_{TL}}(V_{GN}-V_{GP})+\frac{V_{GN}-V_{OUT}}{R_2+1/C_2s}=0 \end{cases} \quad (12)$$

In our design, we set $g_{m3c}=g_{m3d}$. By letting $V_{in}=V_{INP}-V_{INN}$, we will obtain the

expression of V_{GP}-V_{GN}:

$$V_{GP}\text{-}V_{GN}=\frac{V_{out}\{\frac{1}{R_2+1/C_2s}(\frac{1}{R_{O1P}}+C_{1P}s)-\frac{1}{R_1+1/C_1s}(\frac{1}{R_{O1N}}+C_{1N}s)\}+g_{m1}V_{in}\{(\frac{1}{R_{O1N}}+C_{1N}s)-(\frac{1}{R_{O1P}}+C_{1P}s)+\frac{1}{R_2+1/C_2s}-\frac{1}{R_1+1/C_1s}\}}{k_1k_3-k_2^2} \tag{13}$$

where

$$\begin{cases} k_1=\dfrac{1}{R_{O1P}}+C_{1P}s+g_{m3c}+\dfrac{1}{Z_{TL}}+\dfrac{1}{R_1+1/C_1s} \\ k_2=g_{m3c}+\dfrac{1}{Z_{TL}} \\ k_3=\dfrac{1}{R_{O1N}}+C_{1N}s+g_{m3c}+\dfrac{1}{Z_{TL}}+\dfrac{1}{R_2+1/C_2s} \end{cases} \tag{14}$$

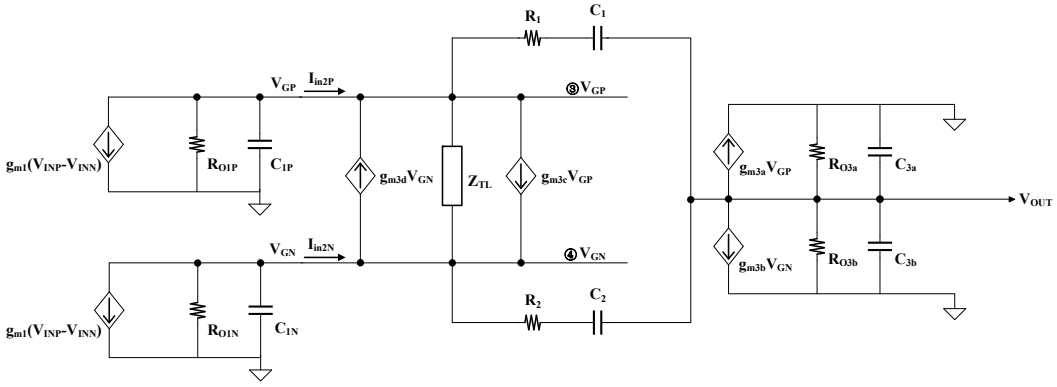


Figure 7. The small-signal model of the entire LA.

When designing the LA, our goal is to achieve V_{GP} - V_{GN} = *0*, emphasizing symmetry considerations. The following should be considered:

(1) R_{O1P} and R_{O1N} are determined by the input stage circuit;

(2) C_{1N} and C_{1P} are dominated by the C_{gs} of output transistors.;

(3) R_1/C_1 and R_2/C_2 are determined by the compensation of LA.

So, if we incorporate the following steps into the LA design, we can achieve symmetry in the circuit to a large extent:

(1) Let $k_{NP}=\dfrac{R_{O1N}}{R_{O1P}}$.

(2) Select the sizes of M_{3a} and M_{3b} such that $C_{1P} = k_{NP}C_{1N}$.

(3) Choose R_1/C_1 and R_2/C_2 values that satisfy the following relation:

$$\begin{cases} R_2=k_{NP}R_1 \\ C_2=\dfrac{1}{k_{NP}}C_1 \end{cases} \tag{15}$$

Then, we will obtain the expression of V_{GP}-V_{GN} from Equation (13)

$$V_{GP}\text{-}V_{GN}=\frac{g_{m1}V_{in}(\frac{1}{k_{NP}}-1)(\frac{1}{R_{O1P}}+C_{1P}s+\frac{1}{R_1+1/C_1s})}{k_1k_3-k_2{}^2} \tag{16}$$

Specifically, when $R_{O1N} = R_{O1P}$, $k_{NP} = 1$. In this case, we will derive that $V_{GP} - V_{GN} = 0$. From Equation (11), we know the key insight is setting $R_{O2a} = R_{O2b}$ because R_{OSRP} is equal to R_{OSRN} in our design for the same current mirror structure.

When $V_{GP} = V_{GN}$, the effects of M_{3c} and M_{3d} cancel each other out because the current $g_{m3d}V_{GN}$ equals the current $g_{m3c}V_{GP}$ in Figure 6(b), and the current through the impedance Z_{TL} equals zero. Then, due to symmetry, the LA circuit can be simplified to that shown in Figure 8. We will find that the small-signal model of the proposed amplifier can be simplified to the well-known two-stage operational amplifier model simply by substituting the parameters with those shown in parentheses in Figure 8.

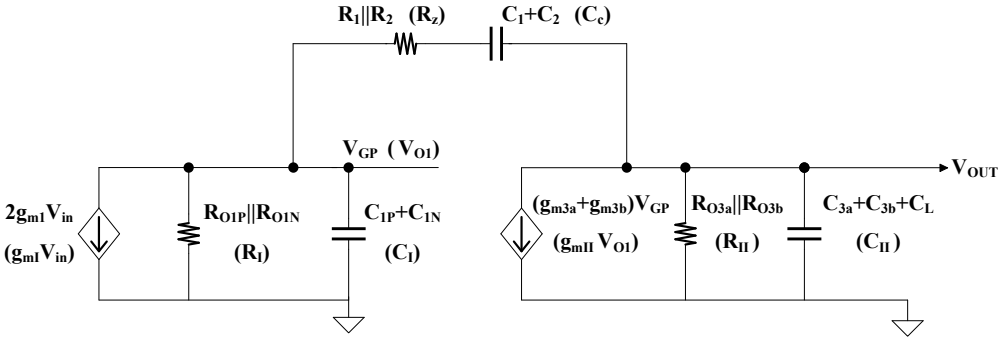


Figure 8. The simplified model of the entire LA.

The amplifier circuit has the following KCL equations:

$$\begin{cases} g_{mI}V_{in}+V_{OI}(\frac{1}{R_I}+C_Is)+(V_{O1}-V_{OUT})\frac{1}{R_c+1/C_cs}=0 \\ g_{mII}V_{O1}+V_{OUT}(\frac{1}{R_{II}}+C_{II}s)+(V_{OUT}-V_{O1})\frac{1}{R_c+1/C_cs}=0 \end{cases} \tag{17}$$

where

$$\begin{cases} g_{mI}=2g_{m1}=4k\dfrac{g_{m3P}g_{m3N}}{g_{m3P}+g_{m3N}}+2\dfrac{g_{m1a}g_{m1b}}{g_{m1a}+g_{m1b}} \\ R_I=R_{O1N}\parallel R_{O1P}=(R_{OSRN}\parallel R_{O2a})\parallel(R_{OSRP}\parallel R_{O2b}) \\ C_I=C_{1P}+C_{1N}=(C_{SRP}+C_{2b}+C_{gs3a})+(C_{SRN}+C_{2a}+C_{gs3b}) \\ R_c=R_1\parallel R_2, C_c=C_1\parallel C_2 \\ g_{mII}=g_{m3a}+g_{m3b} \\ R_{II}=R_{O3a}\parallel R_{O3b}, C_{II}=C_{3a}+C_{3b}+C_L \end{cases} \tag{18}$$

If the poles are widely spaced, then the roots of Equation (17) can be approximated as

$$p_1\cong\frac{-1}{g_{mII}R_{II}R_IC_c} \tag{19}$$

$$p_2 \cong \frac{-g_{mII}}{C_{II}} \tag{20}$$

$$p_3 = \frac{-1}{R_z C_I} \tag{21}$$

and

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)} \tag{22}$$

So, as can be seen, the recommended LA in this paper can be simplified into a general two-stage operational amplifier small-signal model. In the AC analysis, the recommended SRE circuit is equivalent to a stage that is parallel to the input stage of the amplifier and can be integrated into the input stage circuit. Therefore, when selecting the compensation capacitor and resistor to adjust the stability of the amplifier, the impact of the SRE circuit must be considered.