Table S1. Design parameters for the proposed quantum integration chip.

	Width (nm)	**Thickness (nm)**	**Length (μm)**	**Period (nm)**	**duty cycle**	**Etch depth (nm)**
grating coupler	500	300	25	580	0.5	240
	Width(nm)	**Thickness (nm)**	**Straight waveguide length (μm)**	**width of the gap (nm)**	**Radius (μm)**	**Gap(μm)**
directional coupler	500	3300	50	200	300	2.75
	Width (nm)	**Thickness(nm)**	**Length(μm)**			
GaAs waveguide	370	130	21.2894			
	Width (nm)	**Thickness (nm)**	**Length (nm)**	**oxide thickness (μm)**	**Silica oxide thickness (μm)**	
$LiNbO_3$ waveguide	719	300	130	2.4	7	
	Width1 (nm)	**Width2 (nm)**	**Thickness (nm)**	**Length (μm)**		
GaAs taper	370	50	130	50		
	Width(μm)	**Thickness(μm)**				
electrode	30	1				