microelectronics

MDPI

Article

An 18–40 GHz Current-Reuse Low-Noise Amplifier Employing Bandwidth Extension Techniques in 150 nm GaAs Process

Sujin Yoo †, Seonyeong Hwang † and Dae-Woong Park *

Department of Semiconductor Engineering, Seoul National University of Science and Technology, 232 Gongneung-ro, Nowon-gu, Seoul 01811, Republic of Korea; sujin020614@seoultech.ac.kr (S.Y.); tjsdud0035@seoultech.ac.kr (S.H.)
* Correspondence: dwpark@seoultech.ac.kr
† These authors contributed equally to this work.

Abstract

This work presents a wideband current-reuse low-noise amplifier (LNA) implemented in a 150 nm GaAs pHEMT process. To extend the operating bandwidth, the frequency-dependent source degeneration effect introduced by the source capacitors in the current-reuse topology is exploited to suppress the low-frequency gain while enhancing the high-frequency gain, thereby compensating for the intrinsic high-frequency gain roll-off of the common-source (CS) stages. Resistive negative feedback is subsequently employed to further suppress the remaining excessive low-frequency gain and improve circuit stability. The fabricated LNA achieves a peak gain of 17.3 dB, a 3 dB bandwidth of 18.4–39.8 GHz, and a minimum noise figure (NF) of 2.6 dB, while maintaining unconditional stability over the operating frequency range. The LNA consumes only 40 mW from a 5 V drain supply and occupies a chip area of 1.8 × 0.8 mm^2.

Keywords: gallium arsenide; amplifier; low-noise amplifier; current-reuse; low-power; feedback; wideband; millimeter-wave; integrated circuits

1. Introduction

The increasing demand for high data rate wireless communication has driven growing interest in the K (18–26.5 GHz) and Ka (26.5–40 GHz) bands, where the large available spectrum can support high-capacity communication systems [1]. In these frequency bands, the low-noise amplifier (LNA) is a key component of the receiver front end and is required to achieve a low noise figure (NF), sufficient gain, wide operating bandwidth, adequate input/output matching, and low DC power consumption [2]. Among the semiconductor technologies for millimeter-wave (mm-wave) LNAs, gallium arsenide (GaAs) offers high electron mobility and carrier injection velocity, enabling high-speed and high-frequency operation [3]. Furthermore, the low minimum NF attainable with GaAs technologies at mm-wave frequencies makes them particularly attractive for high-frequency low-noise applications [4].

Several multistage cascaded GaAs mm-wave MMIC LNAs have employed bandwidth extension techniques, including resistive feedback, inductive peaking, active loading, and coupled line networks [5–10]. These wideband LNAs typically employ multistage architectures to provide sufficient gain across the operating bandwidth, with each stage requiring its own DC bias current, which can result in relatively high DC power consumption. Current-reuse techniques have therefore been widely employed in CMOS LNAs to reduce DC power consumption by allowing multiple amplification stages to share the

Check for updates

Academic Editor: Filippo Giannazzo

Received: 18 September 2026
Revised: 13 November 2026
Accepted: 16 November 2026
Published: 21 November 2026

Copyright: © 2026 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license.

same bias current [11–13]. Although current-reuse LNAs have also been demonstrated in GaAs technologies [14–18], their reported operating bands are primarily limited to lower frequency ranges. In current-reuse architectures, source capacitors are employed to provide AC paths to ground without disturbing the shared DC current path, while their frequency-dependent impedance introduces source degeneration that affects the gain characteristics of the individual stages. Therefore, extending current-reuse LNAs toward broadband K/Ka-band operation requires careful control of these frequency-dependent gain characteristics while maintaining low DC power consumption.

To address this limitation, this work presents a low-power broadband GaAs LNA based on a three-stage common-source (CS) current-reuse architecture. Rather than using the source capacitors only to provide AC grounding, the proposed design exploits their frequency-dependent characteristics to suppress excessive low-frequency gain and enhance high-frequency gain, thereby compensating for the intrinsic high-frequency gain roll-off of the CS stages. Resistive feedback networks are subsequently applied only to the second and third stages to further suppress the remaining low-frequency gain and improve circuit stability, while no resistive feedback is used in the first stage, whose noise contribution dominates the overall NF. By analyzing the proposed core, which combines capacitive source degeneration and resistive feedback, this work provides a comprehensive design guideline for broadband current-reuse LNAs. Using this design approach, the proposed LNA achieves a measured 3 dB bandwidth of 18.4–39.8 GHz and a minimum measured NF of 2.6 dB, while consuming only 40 mW of DC power from a 5 V drain supply voltage.

The remainder of this paper is organized as follows: Section 2 presents the circuit design and operating principles of the proposed LNA, including the capacitive source degeneration, resistive feedback, and three-stage current-reuse architecture. Section 3 describes the circuit implementation and presents the measurement results of the fabricated LNA. Finally, Section 4 concludes the paper.

2. Circuit Design

2.1. Frequency-Dependent Capacitive Source Degeneration for Bandwidth Extension

To investigate the bandwidth extension mechanism of the source capacitor in the current-reuse architecture, the frequency-dependent effective transconductance G_m of the CS core is analyzed. Figure 1a shows the schematic of the CS core employing the source degeneration capacitor C_{SD2}, and Figure 1b presents its small-signal equivalent circuit.

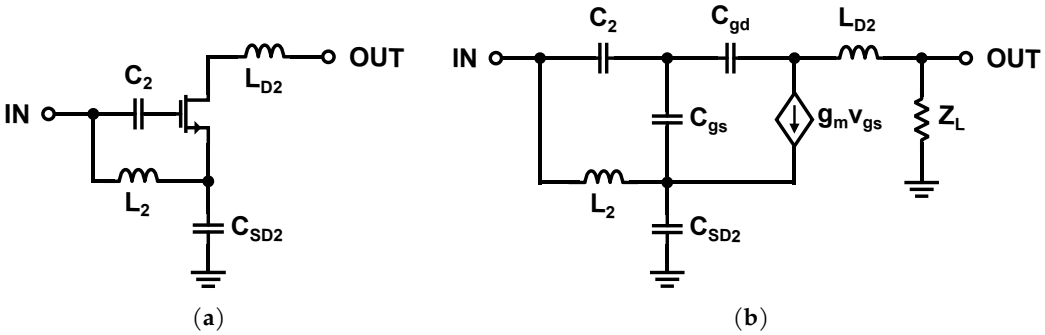


Figure 1. (**a**) Schematic of the CS core employing the source degeneration capacitor C_{SD2} and (**b**) its equivalent small-signal model.

From the equivalent circuit in Figure 1b, G_m can be expressed as

$$G_m = -\frac{g_m C_{gd} + C_{gd}\left(C_2 + C_{gs}\right)s + n_2 s^2 + n_3 s^3}{C_2 + C_{gs} + C_{gd} + g_m\left\{L_2\left(C_2 + C_{gd}\right) + L_{D2}C_{gd}\right\}s + d_2 s^2 + d_3 s^3 + d_4 s^4} \quad (1)$$

where g_m denotes the intrinsic transconductance of the transistor, and the n_2, n_3, d_2, d_3, and d_4 are given by

$$n_3 = C_2 L_2 C_{gd}\left(C_{gs} + C_{SD2}\right), \tag{2}$$

$$n_2 = g_m C_2 L_2\left(C_{gd} - C_{SD2}\right), \tag{3}$$

$$d_4 = L_2 L_{D2}\left\{C_{SD2} C_{gd}\left(C_2 + C_{gs}\right) + C_2 C_{gd} C_{gs}\right\}, \tag{4}$$

$$d_3 = g_m C_{gd} L_2 L_{D2}(C_2 + C_{SD2}), \tag{5}$$

$$d_2 = L_{D2} C_{gd}\left(C_2 + C_{gs}\right) + L_2 C_{gs}\left(C_2 + C_{gd}\right) + L_2 C_{SD2}\left(C_2 + C_{gs} + C_{gd}\right). \tag{6}$$

To clarify the effect of C_{SD2} on the frequency response of G_m, the expression in (1) is analyzed separately in the low- and high-frequency regions.

In the lower-frequency region of interest, the higher-order terms proportional to $n_3 s^3$, $d_3 s^3$, and $d_4 s^4$ are much smaller than the lower-order terms. Substituting $s = j\omega$ into (1) therefore gives

$$|G_{m,LF}(j\omega)| \approx \frac{\sqrt{\left(g_m C_{gd} - n_2\omega^2\right)^2 + \left\{C_{gd}\left(C_2 + C_{gs}\right)\omega\right\}^2}}{\sqrt{\left(C_2 + C_{gs} + C_{gd} - d_2\omega^2\right)^2 + \left[g_m\left\{L_2\left(C_2 + C_{gd}\right) + L_{D2} C_{gd}\right\}\omega\right]^2}}. \tag{7}$$

In (7), the effect of C_{SD2} is mainly determined by n_2 and d_2. From $C_{SD2} > C_{gd}$, (3) gives $-n_2\omega^2 = g_m C_2 L_2\left(C_{SD2} - C_{gd}\right)\omega^2$, which decreases as C_{SD2} is reduced and thus reduces the numerator of (7).

Equation (6) shows that reducing C_{SD2} decreases d_2, as its only C_{SD2}-dependent component is $L_2 C_{SD2}\left(C_2 + C_{gs} + C_{gd}\right)$. This increases $\left(C_2 + C_{gs} + C_{gd} - d_2\omega^2\right)$ in the denominator of (7) and hence increases the denominator magnitude over the low-frequency range. Therefore, a smaller C_{SD2} reduces the numerator magnitude and increases the denominator magnitude, lowering $|G_{m,LF}|$. This result can also be explained from the circuit-operation perspective. As C_{SD2} decreases, its impedance, $1/(j\omega C_{SD2})$, increases. Thus, the source node is less effectively shunted to AC ground, resulting in a smaller v_{gs} for a given input voltage and hence a lower G_m of the core.

In the higher-frequency region of interest, L_2, L_{D2}, C_2, C_{SD2}, and the device parasitic capacitances form a resonant network. By setting the imaginary part of the denominator in (1) to zero, the approximate resonance frequency ω_0 is obtained as

$$\omega_0 = \sqrt{\frac{L_2\left(C_2 + C_{gd}\right) + L_{D2} C_{gd}}{C_{gd} L_2 L_{D2}(C_2 + C_{SD2})}}. \tag{8}$$

With the other circuit parameters fixed, (8) gives $\omega_0 \propto 1/\sqrt{C_2 + C_{SD2}}$. Therefore, decreasing C_{SD2} increases ω_0, shifting the resonance associated with the high-frequency G_m peak to a higher frequency. To examine the effect of C_{SD2} on the magnitude of G_m around this resonance, G_m near ω_0 can be approximated by neglecting the lower-order terms, which have only a minor effect in this frequency region, as

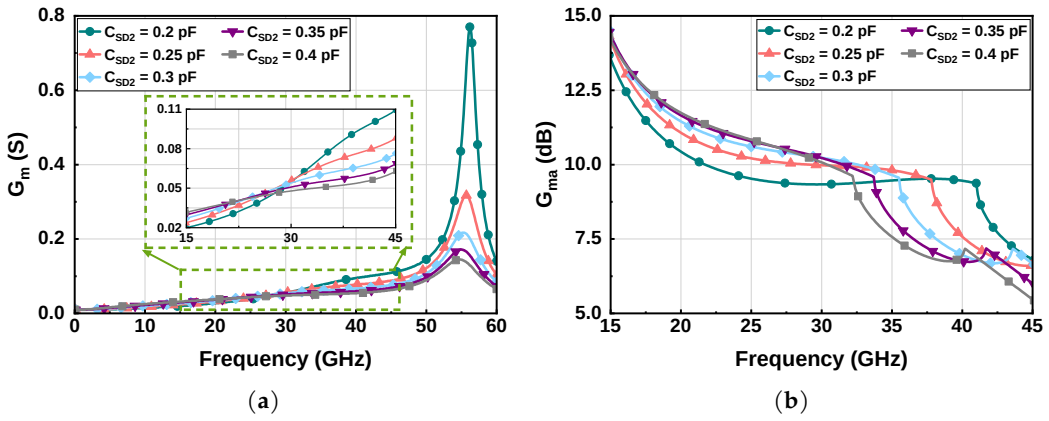
$$|G_{m,HF}(j\omega_0)| \approx \frac{|-n_2\omega_0^2 - jn_3\omega_0^3|}{|-d_2\omega_0^2 + d_4\omega_0^4|} = \frac{\sqrt{n_2^2 + n_3^2\omega_0^2}}{|-d_2 + d_4\omega_0^2|}. \tag{9}$$

In the numerator of (9), $|n_2|$ and n_3 decrease as C_{SD2} is reduced, while the increase in ω_0 partially offsets the reduction in the $n_3\omega_0$ term. Since the denominator magnitude approaches its minimum near ω_0, its variation with C_{SD2} contributes more significantly to the G_m peak than the corresponding variation in the numerator. Substituting (4), (6), and (8) into the denominator of (9) gives

$$|D_{eff,HF}(j\omega_0)| = \frac{L_2\left(C_2 + C_{gs} + C_{gd}\right)C_{SD2}^2 + L_2 C_2 C_{gs} C_{SD2} + L_{D2} C_2^2 C_{gd}}{C_2 + C_{SD2}}. \tag{10}$$

Within the investigated range, (10) shows that reducing C_{SD2} decreases $|D_{eff,HF}|$. Consequently, the reduced denominator magnitude increases the G_m peak magnitude, while the corresponding increase in ω_0 shifts the peak toward a higher frequency.

Figure 2 shows the simulated G_m and maximum available gain G_{ma} of the CS core for different C_{SD2} values. As shown in Figure 2a, reducing C_{SD2} decreases low-frequency G_m, consistent with (7), while increasing the magnitude of high-frequency G_m peak, as predicted by (9) and (10). It also shifts the corresponding resonance peak toward a higher frequency in accordance with (8). Although the simplified small-signal analysis may have limited accuracy due to high-frequency parasitic effects, the derived approximations are consistent with the frequency-dependent trends observed in Figure 2a. As shown in Figure 2b, the C_{SD2}-dependent behavior of G_m is reflected in G_{ma}, where a smaller C_{SD2} suppresses the low-frequency gain and compensates for the high-frequency gain degradation, thereby extending the operating bandwidth. Accordingly, C_{SD2} = 0.2 pF, the minimum implementable value in the process, is selected for the single-stage analysis to maximize low-frequency gain suppression and high-frequency gain enhancement. The corresponding responses are shown as the green curves with circular markers in Figure 2. Although C_{SD2} suppresses the low-frequency gain, Figure 2b shows that the CS core still exhibits higher gain at low frequencies than at the high-frequency end of the operating band. This remaining excess gain can compromise the stability margin. Therefore, resistive feedback is introduced in the following subsection to further suppress the low-frequency gain and improve the stability of the core.



(**a**) (**b**)

Figure 2. Simulated (**a**) effective transconductance G_m and (**b**) maximum available gain G_{ma} of the CS core for different C_{SD2} values.

2.2. Resistive Feedback for Gain Flattening and Stability Enhancement

Figure 3 shows the second-stage CS core with a resistive feedback network composed of R_{F2} and C_{F2} connected between the output and gate nodes. Capacitor C_{F2} provides DC isolation and is set to a sufficiently large value of 1 pF such that its impedance remains low over the target frequency range. The resulting low impedance maintains an effective AC feedback path, while R_{F2} primarily determines the feedback strength [9].

The CS stage introduces a 180° phase inversion between the input and output, allowing the predominantly resistive feedback path to return an inverted output component to the gate and thereby provide negative feedback over the target frequency range. Resistive feedback has been widely used in broadband LNAs for gain shaping and broadband impedance matching, although it generally reduces the forward gain [5,10,19,20]. In particular, a resistive-dominant frequency-dependent feedback path can preferentially suppress low-frequency gain and thereby improve gain flatness over the operating band [21]. In the proposed core, this characteristic is exploited specifically to suppress the remaining exces-

sive low-frequency gain and improve the stability margin. The feedback strength should be appropriately selected because an excessively strong or weak feedback network can result in excessive gain reduction or insufficient stability improvement, respectively [20,22]. In addition, the feedback resistor contributes thermal noise, which should be considered when incorporating resistive feedback networks into a multistage LNA [5,19,20].

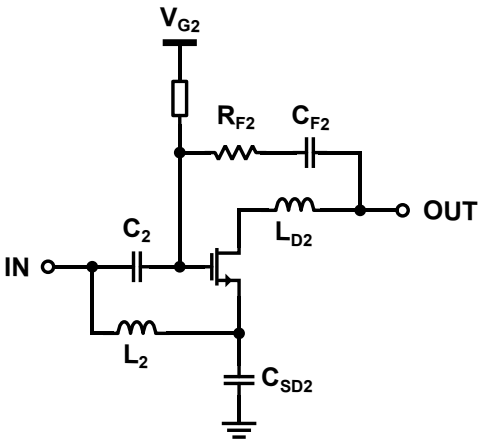
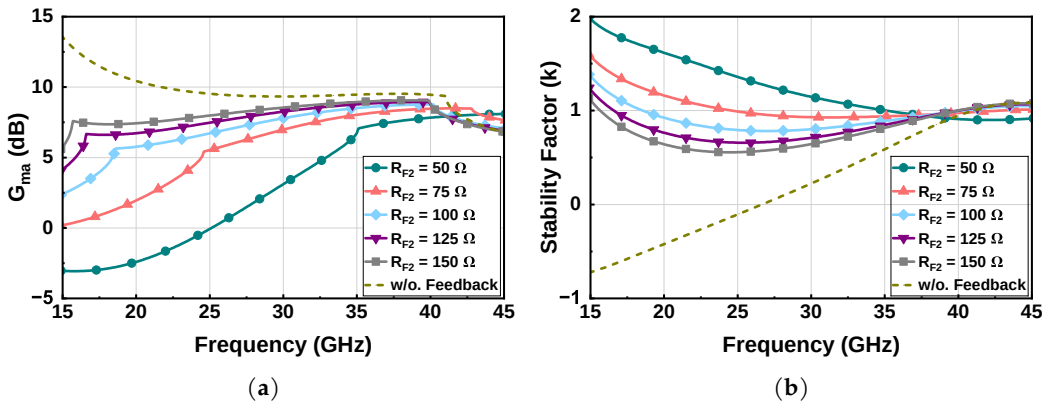


Figure 3. Schematic of the CS core with the resistive feedback.

Figure 4 presents simulated G_{ma} and Rollett stability factor k of the CS core for different values of R_{F2}, with C_{SD2} fixed at 0.2 pF to investigate the effect of resistive feedback. As shown in Figure 4a, resistive feedback suppresses G_{ma} at low frequencies and the suppression becomes stronger as R_{F2} decreases. The gain reduction becomes smaller toward the high-frequency end of the operating range, resulting in a flatter gain response. In contrast to the gain reduction in Figure 4a, Figure 4b shows that k increases as R_{F2} decreases, with stability improvement being more pronounced at low frequencies. Therefore, the feedback strength should be carefully selected to balance gain flatness, in-band gain, and stability. An excessively small R_{F2} results in excessive gain reduction, whereas a large R_{F2} provides insufficient low-frequency gain suppression and stability improvement. Considering both the gain flatness and stability characteristics shown in Figure 4, $R_{F2} = 100\ \Omega$ is selected as the design point. Although the second-stage core is conditionally stable ($0 < k < 1$) at this design point shown in Figure 4b, the interstage networks of the complete LNA are designed to ensure that the source and load impedances presented to each stage lie within their respective stable regions. Consequently, the complete three-stage LNA achieves unconditional stability, as demonstrated in Section 3.



(**a**) (**b**)

Figure 4. Simulated (**a**) G_{ma} and (**b**) k of the CS core with the resistive feedback for different R_{F2} values.

2.3. Proposed LNA Topology and Design Considerations

Figure 5 shows the schematic of the proposed three-stage current-reuse LNA incorporating the capacitive source degeneration and resistive feedback techniques described in Sections 2.1 and 2.2. To reduce the power consumption, the proposed LNA adopts a current-reuse configuration in which the three stages share a common DC current path. As illustrated in Figure 5, L_2 and L_3 provide a shared DC current path, allowing the same bias current to flow through all three CS stages. In contrast, the interstage capacitors C_2 and C_3 block the DC component and transfer the amplified RF signal to the following stage. The source capacitors C_{SD2} and C_{SD3} provide frequency-dependent paths from the source nodes to AC ground without disturbing the shared DC current path. Although the stages share the same DC current, the gate voltages V_{G1}, V_{G2}, and V_{G3} are independently applied through their respective gate bias transmission lines to establish the operating point of each transistor. The RF loading effects of these transmission lines are neglected in the simplified core analysis to isolate the frequency-dependent gain characteristics of the proposed core. In the complete LNA, the gate bias transmission lines can also contribute to impedance matching and are therefore included in the final circuit and electromagnetic (EM) simulations.

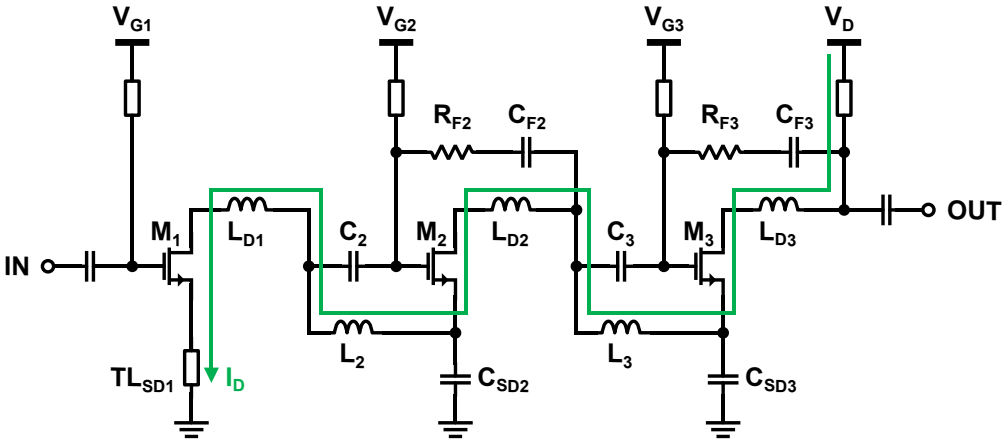


Figure 5. Schematic of the proposed three-stage current-reuse LNA.

Since the first stage largely determines the input matching and dominates the overall NF of the cascaded LNA, a source degeneration transmission line TL_{SD1} is employed instead of a resistive feedback network, thereby avoiding the additional noise associated with resistive feedback. In general, inductive source degeneration interacts with the transistor g_m and C_{gs}, modifying both the real and imaginary parts of the input impedance and facilitating a balanced design of input matching and noise performance [23]. In the proposed design, the length and characteristic impedance of TL_{SD1} are jointly optimized with the surrounding first-stage circuit parameters to achieve suitable input matching and noise performance over the target broadband frequency range. The R_{F2}–C_{F2} and R_{F3}–C_{F3} networks are applied to the second and third stages, respectively, such that their contributions to the overall NF are reduced by the gains of the preceding stages.

In the final implementation, the circuit parameters of the three stages are jointly optimized to achieve a flat overall gain over the target frequency range. The optimization is

performed using circuit simulations incorporating EM models of the passive components and interconnects to account for finite quality factors, parasitics, and coupling at high frequencies. Unlike the $C_{SD2} = 0.2$ pF used in the single-stage analysis, C_{SD2} and C_{SD3} are separately adjusted during the joint optimization to account for the different loading conditions arising from their interactions with adjacent stages and their different contributions to the overall gain response. The final values, $C_{SD2} = 0.23$ pF and $C_{SD3} = 0.3$ pF, are selected to achieve a flat overall gain while maintaining adequate stability. Following the design point selected in Section 2.2, R_{F2} and R_{F3} are both set to 100 Ω. In addition, C_{F2} and C_{F3} are set to 1 pF and 2 pF, respectively, to provide effective AC coupling in the feedback paths over the target frequency range.

3. Implementation and Measurement

The proposed three-stage current-reuse LNA was fabricated using a 150 nm GaAs pHEMT process. Figure 6 shows a chip micrograph of the fabricated LNA, which occupies an area of 1.8 × 0.8 mm^2, including the pads.

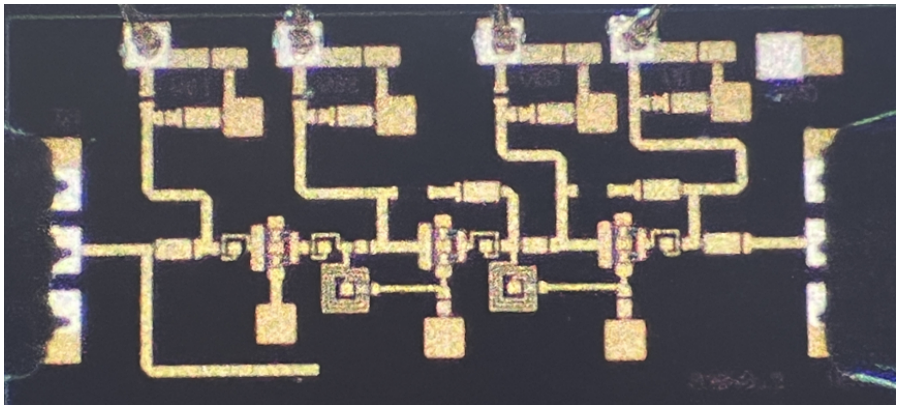
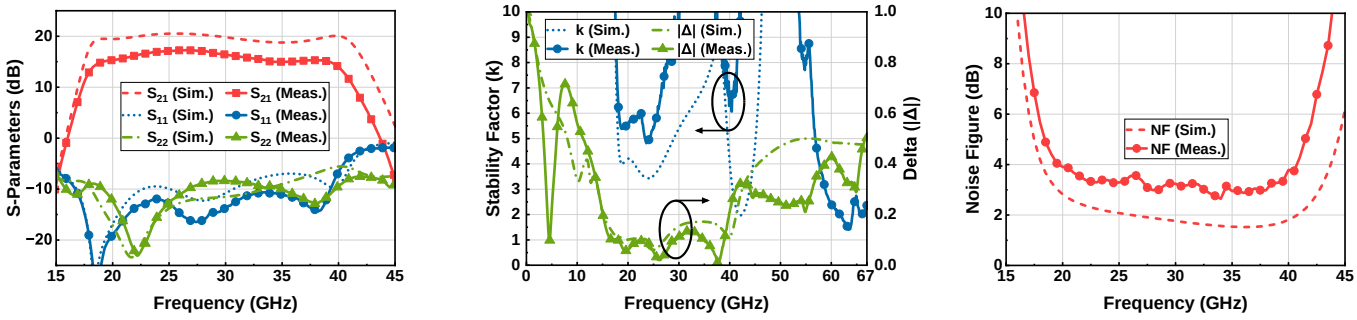


Figure 6. Chip micrograph of the proposed three-stage current-reuse LNA.

Figure 7 shows the simulated and measured S-parameters, Rollett stability factor k, determinant magnitude $|\Delta| = |S_{11}S_{22} - S_{12}S_{21}|$, and NF of the proposed LNA. The deviations between the simulated and measured results may originate from possible limitations in the accuracy of the transistor model and the EM models of passive components and interconnects. At mm-wave frequencies, these limitations and their associated parasitic effects can contribute to the observed deviations. As shown in Figure 7a, the measured LNA achieves a 3 dB bandwidth from 18.4 to 39.8 GHz with a peak gain of 17.3 dB. The measured S_{11} and S_{22} also indicate good input and output matching over the operating frequency range. Figure 7b shows the simulated and measured stability factor k on the left axis and $|\Delta|$ on the right axis. Both simulated and measured results confirm that the complete LNA satisfies the unconditional stability conditions of $k > 1$ and $|\Delta| < 1$ up to 67 GHz. As shown in Figure 7c, the measured NF reaches a minimum of 2.6 dB, and its degradation relative to the simulated NF may be associated with the model limitations discussed above and the observed gain degradation. The three stages share the same DC current of 8 mA, resulting in a total DC power consumption of 40 mW from a drain supply voltage of $V_D = 5$ V.

Table 1 shows the performance comparison with previously reported GaAs LNAs. Among the current-reuse LNAs, the proposed LNA achieves the widest 3 dB bandwidth of 21.4 GHz. Its bandwidth is also comparable to those of the non-current-reuse wideband LNAs, and the DC power consumption of 40 mW is the lowest among the compared LNAs. Although some reported LNAs achieve a higher peak gain or a lower minimum NF, the proposed LNA prioritizes broadband operation with low DC power consumption. These

results demonstrate that the proposed bandwidth extension techniques effectively extend the bandwidth of the current-reuse LNA while maintaining a balanced combination of gain, noise performance, and DC power consumption.



(**a**) (**b**) (**c**)

Figure 7. Simulated and measured (**a**) S-parameters, (**b**) k on the left axis and $|\Delta|$ on the right axis, and (**c**) noise figure of the LNA.

Table 1. Performance comparison with previously reported GaAs LNAs.

Process	Topology	$Gain_{max}$ (dB)	Bandwidth (GHz)	NF_{min} (dB)	P_{DC} (mW)	Area (mm^2)	Reference
0.1 µm	3-stage CS with feedback	23 *	25.0 (18–43)	1.8	140	2	[5]
0.1 µm	3-stage CS with source degeneration	24.2	20.0 (23–43)	2.0	118.4	3.1	[8]
0.15 µm	2-stage CS with current-reuse	25.4	4.0 (8–12)	0.75	150	0.88	[15]
0.15 µm	3-stage CS with current-reuse	23.8	15.0 (6–21)	1.03	135	1.04	[16]
0.15 µm	3-stage CS with current-reuse	27.7	8.0 (10–18)	0.5 *	125	1.21	[17]
0.15 µm	3-stage CS with current-reuse	27.1	18.0 (6–24)	0.71	130	1.04	[18]
0.1 µm	2-stage CS with adaptive bias	15.9	17.8 (18.7–36.5)	1.5	66	0.96	[24]
0.15 µm	3-stage CS with current-reuse	17.3	21.4 (18.4–39.8)	2.6	40	1.44	This work

* Graphically evaluated.

4. Conclusions

In this work, a broadband three-stage current-reuse LNA employing capacitive source degeneration and resistive feedback techniques for bandwidth extension is proposed. The source degeneration capacitors serve as the primary bandwidth extension mechanism by suppressing excessive low-frequency gain and compensating for the intrinsic high-frequency gain roll-off. The resistive feedback networks further suppress the remaining low-frequency gain to improve gain flatness and stability, with the resulting gain flattening also indirectly supporting the achievable 3 dB bandwidth. By analyzing this core, which combines capacitive source degeneration and resistive feedback, this work provides a design guideline for broadband current-reuse LNAs. The fabricated 150 nm GaAs pHEMT LNA achieves a measured 3 dB bandwidth of 18.4–39.8 GHz with a peak gain of 17.3 dB and a minimum NF of 2.6 dB. The three CS stages share the same DC current of 8 mA, resulting in a total DC power consumption of only 40 mW from a 5 V supply. These results demonstrate

that the proposed design achieves broadband operation with low DC power consumption while balancing gain flatness and stability with peak gain and noise performance.

Author Contributions: Conceptualization, D.-W.P.; methodology, S.Y. and S.H.; software, S.Y. and S.H.; validation, S.Y. and S.H.; formal analysis, S.Y. and S.H.; investigation, S.Y. and S.H.; resources, S.Y. and S.H.; data curation, S.Y. and S.H.; writing—original draft preparation, S.Y. and S.H.; writing—review and editing, S.Y., S.H. and D.-W.P.; visualization, S.Y. and S.H.; supervision, D.-W.P.; project administration, D.-W.P.; funding acquisition, D.-W.P. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by Seoul National University of Science and Technology.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: Data are contained within this article.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Camarchia, V.; Quaglia, R.; Piacibello, A.; Nguyen, D.P.; Wang, H.; Pham, A.-V. A Review of Technologies and Design Techniques of Millimeter-Wave Power Amplifiers. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 2957–2983. [CrossRef]
2. Longhi, P.E.; Pace, L.; Colangeli, S.; Ciccognani, W.; Limiti, E. Technologies, Design, and Applications of Low-Noise Amplifiers at Millimetre-Wave: State-of-the-Art and Perspectives. *Electronics* **2019**, *8*, 1222. [CrossRef]
3. Chau, R.; Datta, S.; Majumdar, A. Opportunities and Challenges of III–V Nanoelectronics for Future High-Speed, Low-Power Logic Applications. In Proceedings of the 2005 IEEE Compound Semiconductor Integrated Circuit Symposium, Palm Springs, CA, USA, 30 October–2 November 2005; pp. 17–20. [CrossRef]
4. Fukui, H. Optimal Noise Figure of Microwave GaAs MESFET's. *IEEE Trans. Electron Devices* **1979**, *26*, 1032–1037. [CrossRef]
5. Nikandish, G.; Yousefi, A.; Kalantari, M.; Medi, A. A Broadband Multistage LNA with Bandwidth and Linearity Enhancement. *IEEE Microw. Wirel. Compon. Lett.* **2016**, *26*, 834–836. [CrossRef]
6. Hu, J.; Ma, K.; Mou, S.; Meng, F. A Seven-Octave Broadband LNA MMIC Using Bandwidth Extension Techniques and Improved Active Load. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2018**, *65*, 3150–3161. [CrossRef]
7. Hu, J.; Ma, K. A 1–40-GHz LNA MMIC Using Multiple Bandwidth Extension Techniques. *IEEE Microw. Wirel. Compon. Lett.* **2019**, *29*, 336–338. [CrossRef]
8. Huang, L.; Li, Z.; Wang, Z.; Zhou, P.; Chen, J. A 23–43 GHz LNA with 2.3-dB NF in 0.1-μm GaAs pHEMT Process. In Proceedings of the 2022 IEEE MTT-S International Wireless Symposium (IWS), Harbin, China, 12–15 August 2022; pp. 1–3. [CrossRef]
9. Li, J.; Yuan, Y.; Zeng, J.; He, D.; Yu, Z. A Broadband LNA with Multiple Bandwidth Enhancement Techniques. *IEEE Microw. Wirel. Technol. Lett.* **2023**, *33*, 551–554. [CrossRef]
10. Wang, L.; Cheng, Y.J. A 2–20-GHz Ultrawideband High-Gain Low-Noise Amplifier with Enhanced Stability. *IEEE Microw. Wirel. Technol. Lett.* **2024**, *34*, 415–418. [CrossRef]
11. Lin, Y.-J.; Hsu, S.S.H.; Jin, J.-D.; Chan, C.-Y. A 3.1–10.6-GHz Ultra-Wideband CMOS Low-Noise Amplifier with Current-Reused Technique. *IEEE Microw. Wirel. Compon. Lett.* **2007**, *17*, 232–234. [CrossRef]
12. Hsieh, H.-H.; Lu, L.-H. Design of Ultra-Low-Voltage RF Frontends with Complementary Current-Reused Architectures. *IEEE Trans. Microw. Theory Tech.* **2007**, *55*, 1445–1458. [CrossRef]
13. Zhang, J.; Zhao, D.; You, X. A 20-GHz 1.9-mW LNA Using g_m-Boost and Current-Reuse Techniques in 65-nm CMOS for Satellite Communications. *IEEE J. Solid-State Circuits* **2020**, *55*, 2714–2723. [CrossRef]
14. Xie, C.; Yu, Z.; Tan, C. A Novel Three-Stage Current-Reused Low Noise Amplifier for Ku Band Applications. In Proceedings of the 2019 IEEE MTT-S International Wireless Symposium (IWS), Guangzhou, China, 19–22 May 2019. [CrossRef]
15. Wang, Y.; Wan, L.; Wang, Z.; Zhang, H.; Song, Y.; Zhang, X.; Jin, Z. An X-Band State Adjustable Low Noise Amplifier Using Current Reuse Technique. *Electronics* **2023**, *12*, 696. [CrossRef]
16. Zhang, X.; Wang, K.; Liang, X.; Yan, Y. A 6–21-GHz Wideband Novel Current-Reuse LNA with Simultaneous Noise and Input Matching. *IEEE Microw. Wirel. Technol. Lett.* **2023**, *33*, 1167–1170. [CrossRef]
17. Liu, Y.; Wang, Q.; Xu, K.-D. A 10–18 GHz Current-Reused LNA MMIC with Feedback and Gain-Compensation Techniques. *IEEE Microw. Wirel. Technol. Lett.* **2023**, *33*, 1630–1633. [CrossRef]
18. Zhang, X.; Wang, K.; Yan, Y.; Liang, X. A Compact 6–24-GHz Current-Reuse LNA with Bandwidth and Noise Enhancement. *IEEE Microw. Wirel. Technol. Lett.* **2024**, *34*, 203–206. [CrossRef]

19. Lee, J.; Cressler, J.D. Analysis and design of an ultra-wideband low-noise amplifier using resistive feedback in SiGe HBT technology. *IEEE Trans. Microw. Theory Tech.* **2006**, *54*, 1262–1268. [CrossRef]
20. Perumana, B.G.; Zhan, J.-H.C.; Taylor, S.S.; Carlton, B.R.; Laskar, J. Resistive-feedback CMOS low-noise amplifiers for multiband applications. *IEEE Trans. Microw. Theory Tech.* **2008**, *56*, 1218–1225. [CrossRef]
21. Hu, J.; Ma, K.; Mou, S.; Meng, F. Analysis and design of a 0.1–23 GHz LNA MMIC using frequency-dependent feedback. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1517–1521. [CrossRef]
22. Meaamar, A.; Boon, C.C.; Yeo, K.S.; Do, M.A. A wideband low-power low-noise amplifier in CMOS technology. *IEEE Trans. Circuits Syst. I Reg. Pap.* **2010**, *57*, 773–782. [CrossRef]
23. Nguyen, T.-K.; Kim, C.-H.; Ihm, G.-J.; Yang, M.-S.; Lee, S.-G. CMOS Low-Noise Amplifier Design Optimization Techniques. *IEEE Trans. Microw. Theory Tech.* **2004**, *52*, 1433–1442. [CrossRef]
24. Wang, Z.; Hou, D.; Li, Z.; Zhou, P.; Chen, Z.; Chen, J.; Hong, W. A Linearity-Enhanced 18.7–36.5-GHz LNA with 1.5–2.1-dB NF for Radar Applications. *IEEE Microw. Wirel. Compon. Lett.* **2022**, *32*, 972–975. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.