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Layout-Aware Analysis of Transistor Fingering Effects on Hysteresis and Reliability in CMOS Schmitt Triggers

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Abstract

Schmitt Triggers are essential building blocks in noise-resilient systems and are useful in managing switching behavior in low-power designs. Yet, as CMOS technologies scale down, their designs become increasingly challenging. This paper presents a comprehensive investigation into the performance and reliability of multiple Schmitt Trigger topologies across two CMOS technology nodes (180 nm and 45 nm), with a particular focus on transistor sizing and layout optimization through multi-finger transistor structures. A series of pre-layout and post-layout simulations reveal that fingered implementations significantly enhance hysteresis robustness, switching speed, and delay consistency in PVT variations. Notably, post-layout results in 45 nm technology demonstrate remarkable improvements in both speed and power efficiency. This highlights the inadequacy of schematic-level models to predict the true behavior of fingered transistor configurations. Additionally, we explored the implications of finger designs on reliability concerns including electromigration and IR drop to determine the tradeoff between interconnect reliability optimization and internal routing. The findings establish practical design guidelines for optimizing number of fingers based on device width and technology node, offering new insights into layout-aware Schmitt Trigger design for high-performance and area-constrained applications.

Keywords: Schmitt Trigger; hysteresis; low-power; EDA tools; fingered transistor; noise immunity

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1. Introduction

Over the past decade, the demand for low-power, highly dependable, and noise-resilient integrated circuits has steadily increased. One essential building block that has gained significant attention in this context is the Schmitt Trigger (ST), a bistable circuit renowned for its inherent hysteresis behavior, which enhances noise immunity and signal stability [1]. However, as complementary metal oxide semiconductor (CMOS) technology continues to scale down, circuits face growing challenges such as increased power density and reduced supply voltages. These constraints, while improving performance and integration, simultaneously degrade noise margins and reliability, making robust hysteresis-based solutions such as the ST increasingly critical in modern low-voltage environments [2,3].

The hysteresis phenomenon in a ST introduces two distinct threshold voltages for rising and falling transitions, allowing the circuit to reject spurious fluctuations and noise-induced jitter [4]. This characteristic is particularly valuable in systems operating in noisy environments or under low voltage conditions [5], where input signals may hover near undefined logic levels [6]. By establishing a voltage window between the logic switching thresholds, the ST reduces false toggles while preserving throughput [7]. Nevertheless, the

benefits of hysteresis come with significant design challenges. The width of the hysteresis window and the precision of the switching thresholds are highly sensitive to device mismatches, layout-induced variations, and process fluctuations. Moreover, as supply voltages continue to scale down in modern CMOS technologies, the static noise margin of digital circuits is often compromised, primarily because threshold voltages have not scaled proportionately. This imbalance renders signals more vulnerable to external noise and electromagnetic interference, further emphasizing the need for robust switching behavior [8,9].

Prior research has extensively investigated the metastable states and switching dynamics of STs through analytical models and various simulation techniques [10–12]. Several circuit-level strategies have also been proposed to achieve tunable hysteresis, such as the use of body-biasing in sub-threshold differential STs [12]. While effective in adjusting switching thresholds, these methods remain confined to schematic- or device-level solutions and do not explicitly address how physical layout strategies impact circuit behavior. Aspects such as transistor sizing and fingered implementations are expected to strongly influence performance and long-term reliability, yet systematic evaluations in this direction remain limited. This gap motivates further exploration of layout-aware considerations as a complementary design dimension for robust hysteresis control.

The versatility of STs has made them indispensable in a wide range of digital and mixed-signal applications, including waveform generators, oscillators, monostables, pulse width modulation circuits, and analog-to-digital converters [13,14]. STs also find relevance for enhancing the immunity of noise-sensitive systems, besides their use in subthreshold SRAMs [15–17]. Furthermore, in ultra-low-power systems, STs are crucial for providing stable operation in circuits such as ring oscillators, particularly in boost converter [18]. In some cases, the ability to tune hysteresis behavior, such as in power management and power amplifier circuits can lead to better energy efficiency and improved circuit responsiveness [19,20].

In addition to their role in mitigating noise in signal processing, STs are also widely employed to provide essential stabilization in level shifter circuits. These circuits are particularly common in power-oriented systems, such as gate drivers for Gallium Nitride (GaN) high electron mobility transistors (HEMTs) [21], where voltage swings may span from a few volts up to tens of volts. In such systems, the level-shifting stage is typically followed by an ST to suppress oscillations, sharpen logic transitions, and prevent unintended activation of the power device. This approach, as demonstrated in [22], employs a modified ST at the output of an 18 V level shifter to enhance signal stability and noise margins before driving the gate of a GaN HEMT. Such environments, characterized by high slew rates and capacitive loads, make the STs hysteresis and strong drive capabilities essential for mitigating ringing, overshoot, and false triggering, effects commonly observed in GaN-based gate drive systems [23]. Such effects are further emphasized in integrated GaN-based converters, where layout parasitics and switching dynamics critically define performance boundaries [24].

Moreover, when the ST interfaces with high-capacitance nodes, such as the input terminals of GaN HEMTs or silicon-based power MOSFETs, the drive capability of the circuit becomes a decisive factor. These power devices typically present input capacitances ranging from several tens to hundreds of picofarads, which impose substantial dynamic charging and discharging requirements. Under such conditions, ST drivers must employ transistors with large effective widths to achieve adequate switching performance. Fingered layouts provide a systematic approach for realizing such widths, as they not only improve switching speed and reduce propagation delay [25], but also enhance power efficiency by lowering effective gate resistance and distributing current more uniformly across the

device fingers. This layout strategy, therefore, establishes itself as an important enabler for reliable operation in high-frequency and high-power environments.

Given the importance of these circuits, this work presents a comprehensive evaluation of ST topologies implemented in two CMOS technology nodes: 180 nm and 45 nm. The study investigates how technology scaling, transistor sizing, and fingered layout structures influence critical performance metrics including hysteresis width and symmetry, propagation delay, power consumption, and robustness under process-voltage-temperature (PVT) variations. The study emphasizes the role of fingered transistor configurations in terms of absolute width scaling and finger count under a fixed effective width. This approach isolates electrical trade-offs, identifies diminishing returns, and determines optimal design points. Pre-layout and post-layout simulations are conducted to evaluate the impact of parasitic effects and validate layout-aware design considerations. Furthermore, the study attracts attention for how distributed layout strategies, including fingered transistor implementations, not only influence key performance metrics such as speed, hysteresis, and power, but also affect reliability aspects like electromigration (EM) and IR drop, often beyond the predictive scope of pre-layout models. The insights gained aim to inform the selection and optimization of ST architectures in performance-critical and area-constrained applications.

Building upon these layout-aware considerations, this work further contrasts three fundamental ST orientations; the Conventional 6 Transistor ST, the Modified ST, and the P-type ST, selected for their simplicity and prevalence in practical designs. Unlike adaptive or complex variants, these basic architectures are widely integrated in digital and mixed-signal systems, from memory elements to power interfaces, thereby making the comparative analysis broadly relevant. By systematically examining their hysteresis behavior, timing performance, and robustness across technology nodes, this study provides not only quantitative benchmarks but also qualitative insights regarding the inherent trade-offs between speed, power, and stability. Such an approach bridges the gap between schematic-level projections and the actual layouts, offering circuit designers a grounded basis for topology selection under varying performance and area constraints.

The remainder of this paper is organized as follows. Section 2 provides a comparative overview of various ST circuit topologies. Section 3 introduces a modeling framework for analyzing hysteresis behavior under fingered layout configurations. Section 4 presents simulation results, highlighting the impact of technology scaling, transistor sizing, and fingering on key performance metrics. Finally, Section 5 concludes the paper and summarizes the main findings.

2. Comparative Overview of ST Circuit Topologies

Before elaborating on three commonly used ST circuit topologies we provide an outline of the fundamental operating principles of all STs. The ST is a logic circuit that enhances noise immunity by introducing hysteresis into its voltage transfer characteristic. In contrast to a standard inverter, the switching threshold of a ST depends on the direction of the input transition. As illustrated in Figure 1a, the transfer curve exhibits two distinct switching points: V_{LH} for low-to-high input transitions and V_{HL} for high-to-low transitions. The hysteresis width, $\Delta V_{HYST} = V_{HL} - V_{LH}$, defines the voltage window in which the output remains unchanged despite fluctuations in the input. Figure 1b demonstrates the temporal response of the circuit, showing a noisy input signal (V_{IN}) and the corresponding output (V_{OUT}). The output transitions occur only when the input crosses the hysteresis boundaries, ensuring stable and clean switching behavior. This characteristic makes ST circuits essential in applications requiring robust signal conditioning or noise rejection.

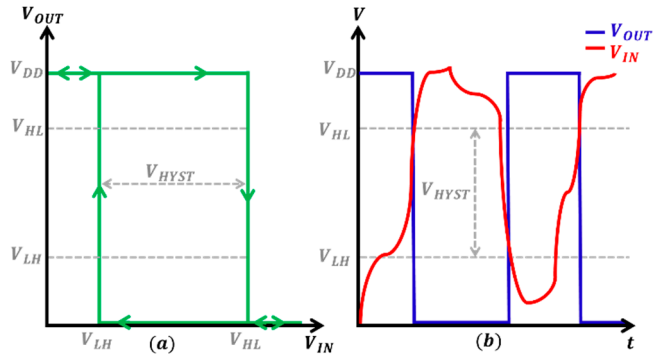


Figure 1. (**a**) Voltage transfer curve of a ST showing hysteresis window and (**b**) Time-domain response to noisy input.

Now, the structural composition and functional behavior of three specific topologies is presented. The schematic diagrams of the topologies are shown in Figure 2a–c.

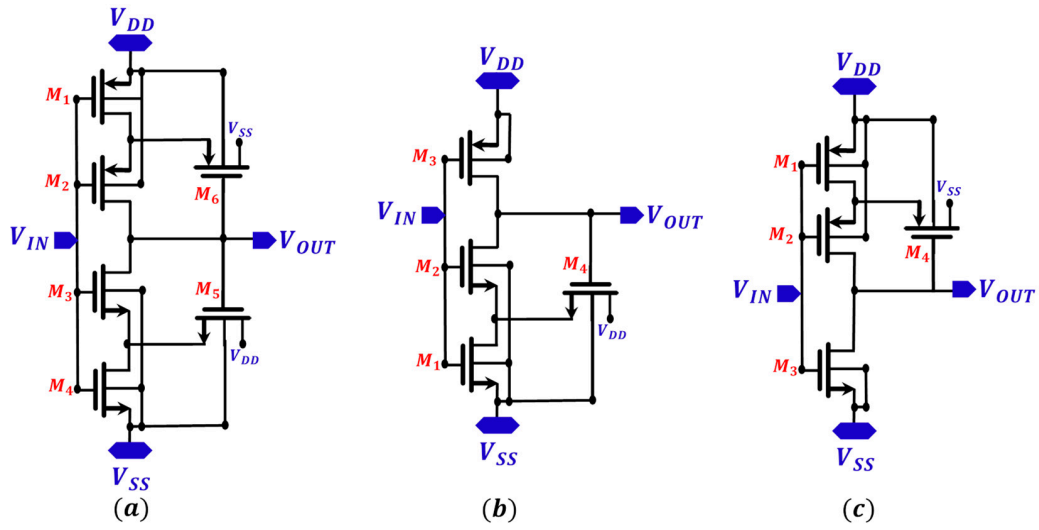


Figure 2. Schematic diagrams of three ST topologies: (**a**) Conventional 6T, (**b**) Modified, and (**c**) P-type.

2.1. Conventional 6T ST

The conventional 6-transistor (6T) ST topology is illustrated in Figure 2a. This design realizes its inherent hysteresis behavior by embedding cross-coupled feedback transistors within a standard CMOS inverter structure. The configuration distinctly defines two separate switching thresholds: V_{LH} for rising and V_{HL} for falling input transitions, effectively enhancing noise immunity and ensuring deterministic switching behavior.

When the input voltage is low, the pull-up network, made of p-channel MOS (PMOS) transistors, becomes active, charging the output node toward V_{DD}. During this phase, regenerative feedback accelerates the rise in output voltage, reinforcing the logic HIGH state as the output nears its final value. Conversely, when the input crosses V_{LH}, the pull-down network, made of n-channel MOS (NMOS) transistors, activates. Initially, the complementary feedback introduces a slight delay, preventing premature switching. However, once the output descends below V_{HL}, the feedback generates a rapid discharge, solidifying the output transition to the LOW state.

2.2. Modified ST

The modified ST topology is illustrated in Figure 2b. This configuration introduces a feedback-enhanced mechanism that allows the circuit to establish two distinct threshold

voltages for rising and falling input edges, enabling hysteresis behavior. The design builds upon a basic inverter structure while integrating additional transistors to stabilize transitions and suppress noise.

At low input voltages, the PMOS transistor conducts, charging the output node toward the supply rail. In this state, the NMOS transistors responsible for discharging are inactive, and the output remains at a HIGH logic level. As the input voltage increases and surpasses a defined upper threshold, the NMOS transistors become active, establishing a conduction path to ground. This causes the output to transition from HIGH to LOW. Simultaneously, the PMOS turns off, eliminating the charging path and reinforcing the downward transition.

A key feature of this design is the presence of a dedicated feedback transistor, which is driven by the output voltage. This element introduces positive feedback into the system, sharpening the transition and ensuring a stable state. As a result, the voltage at which the output switches from LOW to HIGH differs from the voltage recoiling from HIGH to LOW, thus forming a hysteresis window.

2.3. P-Type ST

The P-type ST, depicted in Figure 2c, represents the complementary version of the modified ST with a single NMOS transistor and three PMOS transistors. Its operation and hysteresis characteristics are analogous to the previously explained Modified ST, with threshold voltages V_{LH} and V_{HL}. The circuit exhibits a hysteresis-shaped transfer characteristic, primarily due to the interaction of transistors M_1 and M_4 (in Figure 2c). When the input is LOW, M_1 and M_2 are ON while M_3 and M_4 are OFF. Conversely, for a HIGH input, M_3 and M_4 are ON and M_1 and M_2 are OFF. In both stable states, the quiescent supply current is negligible.

3. Hysteresis Modeling of ST Topologies Under Fingered Layouts

This section develops a layout-aware analytical framework for predicting hysteresis in ST topologies with fingered transistor implementations. The section begins with a description of how finger segmentation modifies intrinsic device parameters, followed by the baseline hysteresis formulations for the conventional 6T, Modified, and P-type STs. The models are then extended through the definition of an effective transconductance parameter that compactly incorporates gate resistance relief, parasitic capacitances, and statistical matching. Using this framework, analytical predictions are derived for delay, power, hysteresis behavior, statistical robustness, PVT sensitivity, and EM/IR implications. Thus, the section connects ideal transistor-level models with layout-aware corrections, clarifying how segmentation strategies reshape hysteresis characteristics across different ST topologies.

3.1. Fingered Transistor Implementation

As the width of a transistor increases, the layout area and gate resistance also increase. The fingered layout technique mitigates these limitations by splitting a wide transistor into N_f narrower segments connected in parallel, preserving the total width W_{Total} while improving layout compactness and electrical performance. This approach is especially beneficial in high-current, high-speed circuits such as power-oriented ST drivers, where parasitic effects and drive capability must be balanced.

Figure 3 illustrates the principle of implementing fingers. Figure 3a depicts a transistor with a total width W which is considered a basic orientation. Figure 3b shows the same transistor split into three narrower sections, each with a width of W/3, connected in parallel to implement the finger technique. Consequently, the total effective width is preserved. Beyond the advantages of moderating the dimensions of the physical layout, the technique

of finger transistors also impacts key electrical parameters. For instance, while the overall transconductance coefficient (β) theoretically remains unchanged due to the preserved W/L ratio, transistors with more finger structures reduce statistical variation and improve matching, leading to more predictable switching thresholds. A minor downside is that the effective gate-source capacitance (C_{GS}) may slightly increase due to additional fringing and overlapping capacitances between adjacent fingers. Nonetheless, the lower gate resistance per unit width reduces RC delay and enhances switching improving the hysteresis behavior. ST topologies in particular benefit from finger designs where even minor deviations in β or threshold voltage (V_{TH}) can shift the hysteresis window significantly.

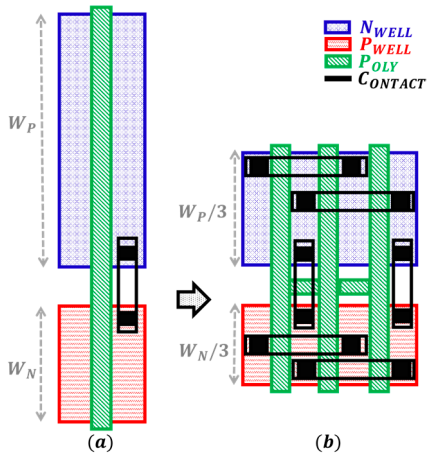


Figure 3. CMOS layout implementations comparing basic and fingered orientations: (**a**) basic CMOS orientation, (**b**) three-finger equivalent orientation preserving the W/L ratio.

For a MOS device implemented with N_f fingers, the ideal transconductance parameter is given by

$$\beta_f = N_f \cdot \mu \cdot C_{OX} \cdot (W_f/L) = \mu \cdot C_{OX} \cdot (W_{Total}/L) \quad (1)$$

where $W_f = W_{Total}/N$, L is the channel length, μ is the carrier mobility, and C_{OX} is the oxide capacitance per unit area.

3.2. Analytical Formulation of Hysteresis in ST Topologies

Following the transistor-level current-balance models in [10,26], the hysteresis window ΔV_{HYST} can be expressed for each topology as a function of current ratios derived from the transconductance parameters $\beta_i = \mu \cdot C_{OX} \cdot (W_i/L_i)$ of devices M_i.

- Conventional 6T ST:

$$\Delta V_{HYST} = \left(\frac{1}{(1+\alpha_2)}\right) \cdot \left(\frac{(\alpha_2 \cdot (V_{DD} - V_{THn}))}{(1+\alpha_3)} + \frac{(V_{DD} - |V_{THp}|)}{(1+\alpha_1)}\right) \quad (2)$$

where α_i are current ratios defined as

$$\Delta\alpha_1 = \sqrt{\frac{\beta_1}{\beta_6}},\ \alpha_2 = \sqrt{\frac{(\beta_3 \cdot \beta_4)/(\beta_3 + \beta_4)}{(\beta_1 \cdot \beta_2)/(\beta_1 + \beta_2)}}, \alpha_3 = \sqrt{\frac{\beta_4}{\beta_5}} \quad (3)$$

- Modified ST:

$$\Delta V_{HYST} = \frac{\gamma_2 \cdot (V_{DD} - V_{THn})}{(1+\gamma_1)(1+\gamma_2)} \quad (4)$$

where γ_i are current ratios defined as

$$\gamma_1 = \sqrt{\frac{\beta_1}{\beta_4}},\ \gamma_2 = \sqrt{\frac{(\beta_1 \cdot \beta_2)/(\beta_1 + \beta_2)}{\beta_3}} \tag{5}$$

- P-type ST:

$$\Delta V_{HYST} = \frac{V_{DD} - V_{THp}}{(1+\delta_1)(1+\delta_2)} \tag{6}$$

where δ_i are current ratios defined as

$$\delta_1 = \sqrt{\frac{\beta_1}{\beta_4}},\ \delta_2 = \sqrt{\frac{\beta_3}{(\beta_1 \cdot \beta_2)/(\beta_1 + \beta_2)}} \tag{7}$$

3.3. A First-Order Physical Picture of Hysteresis in ST Topologies

Finger segmentation alters three dominant mechanisms:

1. Distributed gate resistance relief. Splitting the gate reduces the effective R_G and homogenizes the longitudinal charging of the inversion channel, improving switching drive on fast edges.
2. Added fringing/overlap and routing capacitance. Gate segmentation increases edge/overlap surfaces and introduces wiring overhead; at large N_f or dense routing, these parasitics can offset the R_G benefit.
3. Statistical matching. Parallel slices average local process variations (e.g., threshold dispersion), which stabilizes positive-feedback switching in ST networks; exceptions exist for PMOS-dominated paths where mobility and edge parasitics can bias the effect.

To capture these effects compactly, we introduce for each device M_i an effective transconductance:

$$\beta_{i,eff}(N_f) = \beta_i \cdot \phi_R(N_f) \cdot \phi_C(N_f) \cdot M(N_f) \tag{8}$$

where $\phi_R > 1$ models R_G relief (most pronounced for moderate N_f), $\phi_C < 1$ penalizes added parasitics when they dominate, and $M(N_f) \approx 1 \pm \varepsilon$ reflects matching-driven corrections.

Replacing intrinsic β_i with their effective counterparts, $\beta_{i,eff}\left(N_f\right)$, in the current ratios (α, γ, δ) of Equations (3), (5) and (7) yields a layout-aware expression for hysteresis. Denoting the set of effective ratios for each topology by $\acute{X}\left(N_f\right)$, the resulting hysteresis is given by

$$\Delta V_{HYST}\left(N_f\right) = F_T\left(\acute{X}\left(N_f\right); V_{DD},\ V_{THn},\ V_{THp}\right) \tag{9}$$

For clarity, the effective current ratios for the 6T topology are shown below; other topologies follow analogous definitions using the corresponding current ratios α, γ, δ:

$$\begin{gathered} \acute{\alpha}_1\left(N_f\right) = \sqrt{\frac{\beta_{1,eff}\left(N_f\right)}{\beta_{6,eff}\left(N_f\right)}} \\ \acute{\alpha}_2\left(N_f\right) = \sqrt{\frac{\left(\beta_{3,eff}\left(N_f\right) \cdot \beta_{4,eff}\left(N_f\right)\right)/\left(\beta_{3,eff}\left(N_f\right) + \beta_{4,eff}\left(N_f\right)\right)}{\left(\beta_{1,eff}\left(N_f\right) \cdot \beta_{2,eff}\left(N_f\right)\right)/\left(\beta_{1,eff}\left(N_f\right) + \beta_{2,eff}\left(N_f\right)\right)}} \\ \acute{\alpha}_3\left(N_f\right) = \sqrt{\frac{\beta_{4,eff}\left(N_f\right)}{\beta_{5,eff}\left(N_f\right)}} \end{gathered} \tag{10}$$

First-order sensitivity around a nominal N_f highlights which devices govern the trend. Sensitivity is computed with respect to the current ratios of the chosen topology only, capturing the dominant devices that affect hysteresis:

$$\frac{\partial \Delta V_{HYST}}{\partial \beta_i} \approx \sum_k \left(\frac{\partial F_T}{\partial \alpha_k}\right)\left(\frac{\partial \alpha_k}{\partial \beta_i}\right) \tag{11}$$

If a device M_i lies on the positive-feedback conduction path, an increase in $\beta_{i,eff}$ tends to expand the hysteresis window; if M_i sits on a heavily loaded or limiting branch, the effect can saturate or even reverse once ϕ_C dominates. This explains why the same fingering strategy produces different hysteresis trends across 6T, Modified, and P-type STs.

3.4. Analytical Predictions

The framework above yields the following falsifiable hypotheses:

1. Delay. For fixed W_{Total}, propagation delay (T_{PD}) decreases with N_f until saturating when parasitic capacitance offsets R_G relief.
2. Power. Dynamic power slightly increases due to added capacitance; however, in symmetric layouts (notably the Modified ST) post-layout routing can reduce effective switching energy so that average power remains similar or even decreases
3. Modified ST, ΔV. With more symmetric positive feedback and stronger R_G relief, ΔV_{HYST} grows modestly for small-to-medium W_{Total} and then plateaus.
4. 6T ST, ΔV. In 6T, asymmetry and a more heavily loaded internal node may cause a mild decrease in ΔV_{HYST} at large W_{Total}; at small widths a short-gate advantage can still yield a local increase.
5. P-type ST, ΔV. PMOS-centric paths are prone to mobility/fringing sensitivity under segmentation, leading to a noticeable reduction in ΔV_{HYST} and skewed distributions.
6. Statistical effects. The standard deviation (σ) of key metrics such as the propagation delay $\sigma(T_{PD})$ and, the ΔV_{HYST}, decreases with increasing N_f in NMOS-weighted designs due to averaging of local mismatches. In contrast, P-type dominated paths can exhibit non-Gaussian tails, where mobility degradation and edge parasitics bias the distribution.
7. PVT. Fingering narrows PVT spread of T_{PD} and ΔV_{HYST}, especially under Slow-Slow corners or at high temperature, R_G is most penalizing.
8. EM/IR. Current spreading across fingers improves J/J_{MAX} and IR drop on global and output nets, but dense internal routes can become local bottlenecks, worsening EM/IR on specific critical segments.

These hypotheses outline the expected behavior of ST circuits under fingered layouts and provide a foundation for analyzing performance trends across different technology nodes and configurations in the next section.

4. Case Study

All experimental evaluations were conducted using the Cadence Virtuoso Analog Design Environment (ADE), targeting two CMOS technology nodes: gpdk45 (45 nm) and TSMC180HV (180 nm). The gpdk45 process denotes Cadence generic predictive Process Design Kits (PDK), commonly utilized in academic and research environments for circuit design and comparative technology analysis. A 10 MHz pulse signal was applied in all simulations to emulate high-speed digital transitions. The supply voltages were set to 1 V and 1.8 V for the 45 nm and 180 nm nodes, respectively. For the 180 nm node, 1.8 V aligns with the nominal operating voltage defined by the TSMC180HV PDK. For the 45 nm node,

a slightly reduced voltage of 1 V (below the typical 1.1 V) was intentionally selected to explore layout-dependent performance behaviors under conservative voltage scaling.

This section presents the simulation-based evaluation of the proposed analytical framework, aiming to verify the hypotheses introduced in Section 3 and quantify the impact of layout strategies on circuit performance.

The simulations were structured to investigate the influence of

- Transistor layout strategy;
- Statistical process variations;
- Temperature-dependent behavior;
- Reliability phenomena including EM and IR drop.

The results are presented in the following dedicated subsections. To ensure consistency and isolate the impact of layout and process factors, all transistors within a given ST topology were assigned identical sizes. While this approach may not yield optimal performance for each device's role, it enables a controlled and systematic comparison across layout styles and technology nodes, eliminating complexity caused by making sizing a variable.

While the inherent differences in supply voltage and threshold voltage between the 45 nm and 180 nm nodes dictate the absolute performance values, this analysis focuses strictly on intra-technology comparison. Our methodology is designed to isolate the relative impact of the fingered layout topology (versus the non-fingered layout) on all ST topologies under each node's nominal conditions, thereby avoiding a cross-node comparison.

4.1. Influence of Fingered Layout on ST Topologies

The first experiment examines the influence of transistor layout structure, specifically the presence or absence of fingered devices, on the three ST topologies mentioned above: the conventional 6T ST, a modified ST, and a P-type ST. The analysis is performed using both 45 nm and 180 nm CMOS technologies. For each technology, the total transistor width is swept from the minimum allowed width up to 10 µm, using uniform increments (120 nm for 45 nm, 220 nm for 180 nm).

In the fingered configurations, the number of fingers is chosen to make the width of each finger correspond to the minimum manufacturable width permitted by the technology. This ensures that, for any given total transistor width, both the fingered and non-fingered layouts maintain identical overall sizing (W_{Total}), allowing layout effects to be isolated and fairly compared. For example, for a transistor with a total width of 0.69 µm, implemented in the 45 nm technology, eight fingers are used, each 120 nm wide.

Each combination of technology, and layout configuration is subjected to transient simulations, from which three key performance metrics are extracted: hysteresis width ΔV_{HYST}, T_{PD}, and average power consumption. The results are presented in Figures 4–6, which illustrate the comprehensive comparison of each ST architecture to layout style across a range of transistor widths.

Figure 4 shows that fingered configurations lead to a noticeable widening of the hysteresis window, especially at lower transistor widths. This effect is prominent in the 45 nm technology at $W_{Total} \approx 0.69$ µm, where ΔV_{HYST} increased by 7–8% across 6T and modified ST variants. Comparable improvements were observed in the 180 nm node, albeit from a higher baseline hysteresis. The benefit of fingered designs beyond approximately 2 µm in 45 nm and 5 µm in 180 nm is not observed, suggesting that the contribution of fingering becomes negligible at larger device sizes.

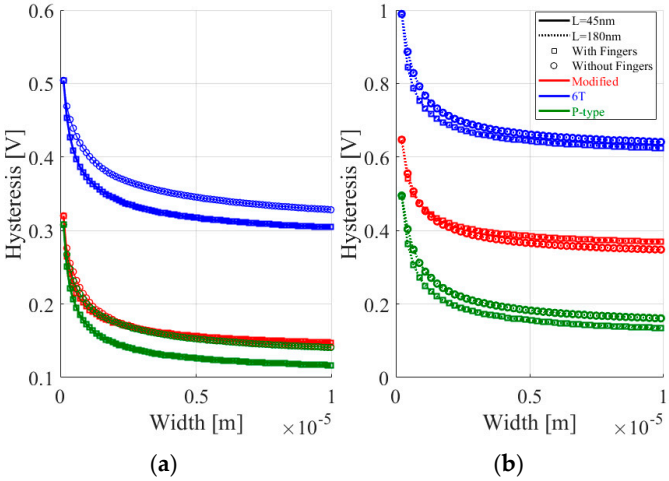


Figure 4. Hysteresis window versus transistor width for three ST topologies with and without fingered layout: (**a**) 45 nm, (**b**) 180 nm.

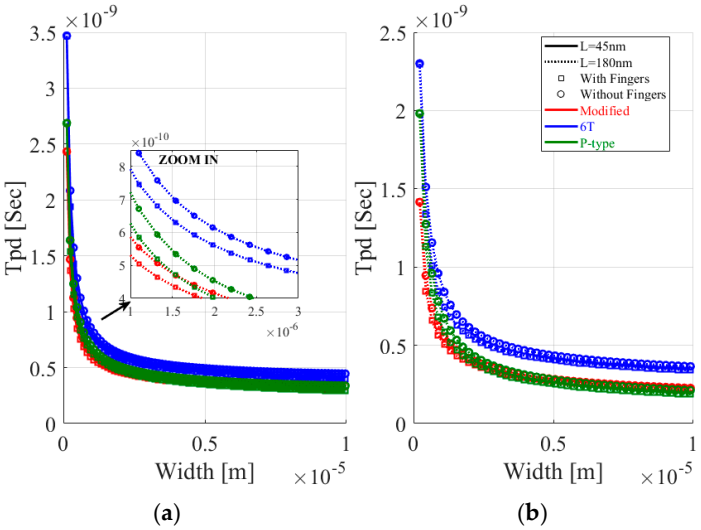


Figure 5. Propagation delay versus transistor width for three ST topologies with and without fingered layout: (**a**) 45 nm, (**b**) 180 nm.

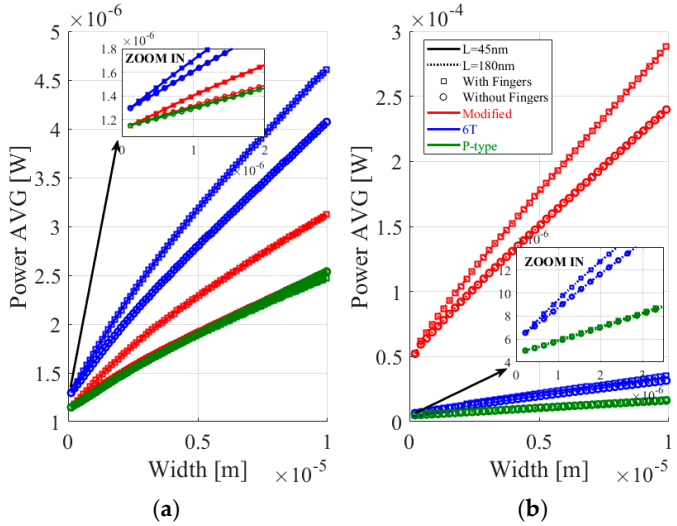


Figure 6. Average power consumption versus transistor width for three ST topologies with and without fingered layout: (**a**) 45 nm, (**b**) 180 nm.

Propagation delay results (Figure 5) show a consistent reduction in delays when fingers are applied, particularly within the small-to-moderate width range. In 6T 45 nm topologies, fingered devices achieved up to 12% reduction in delay compared to their monolithic counterparts. This speed increase is linked to a reduction in effective gate resistance and improved charge distribution along the gate structure. Similar trends are observed in 180 nm, confirming the scalability of the improvements across the nodes.

These performance improvements come with a slight increase in average power consumption (Figure 6), typically within 10–20%, depending on topology and node. This overhead is primarily due to additional routing complexity and parasitic capacitance introduced by fingered layouts.

Among the topologies, the P-type ST demonstrates the largest relative hysteresis enhancement under fingering, likely due to higher variability in PMOS behavior. Meanwhile, the modified ST consistently exhibits the fastest absolute switching speeds, indicating a synergistic interaction between its symmetrical structure and the distributed geometry of the fingered layout.

4.2. Statistical Robustness Analysis of ST Topologies Using Monte Carlo Simulations Across Technology Nodes

To evaluate the statistical robustness of ST circuits under inherent process variations, a second set of simulations is performed using Monte Carlo analysis. This technique provides a probabilistic understanding of circuit behavior by randomly sampling device parameters across manufacturing tolerances, thereby capturing the spread and likelihood of various outcomes under realistic fabrication conditions. The three mentioned ST topologies are analyzed both in 45 nm and in 180 nm technologies. Each topology is simulated using both fingered and non-fingered transistor configurations. A constant total transistor width is chosen for both cases to ensure a fair comparison. For 45 nm, a width of 6 µm is used and implemented with 50 fingers to match the minimum finger width. In the 180 nm technology, the transistor width is set to 5.96 µm, corresponding to 27 fingers. The basic configurations are constructed using the same total width without segmentation. All simulations are performed at room temperature (27 °C), with 500 randomized runs per configuration. The variation model includes all process and mismatch sources, using a random sampling method. Three key performance metrics are extracted from the simulation data: ΔV_{HYST}, average power consumption, and T_{PD}. The complete statistical results for each topology and configuration are summarized in Tables 1–3. To further analyze the distribution of hysteresis behavior, histograms are plotted for the fingered configurations in the 45 nm and 180 nm technologies, as shown in Figure 7. Additionally, Table 4 presents the hysteresis behavior of the quantitative statistical descriptors, including Jarque–Bera, kurtosis, and skewness. The Jarque–Bera statistic assesses the deviation of the distribution from normality, kurtosis indicates the sharpness or flatness of the distribution, and skewness reflects asymmetry.

Table 1. Monte Carlo results for the conventional 6T ST topology.

Tech	Fingered	ΔV_{HYST} [mV]	Power AVG [mW]	T_{PD} [ps]
45 nm	Without	340 ± 3	3.06 ± 0.04	478 ± 2.4
45 nm	With	313.88 ± 4.4	3.52 ± 0.13	442 ± 6.9
180 nm	Without	655 ± 7.98	22.1 ± 0.75	413 ± 8.73
180 nm	With	640.6 ± 10.3	25.4 ± 1.39	394 ± 11.5

Table 2. Monte Carlo results for the modified ST topology.

Tech	Fingered	ΔV_{HYST} [mV]	Power AVG [mW]	T_{PD} [ps]
45 nm	Without	150 ± 1.69	2.04 ± 0.014	368 ± 1.73
45 nm	With	154 ± 1.44	2.48 ± 0.19	336 ± 1.69
180 nm	Without	361 ± 9.39	172 ± 7.13	270 ± 7.18
180 nm	With	382 ± 13.9	206 ± 14.1	263 ± 9.33

Table 3. Monte Carlo results for the P-type ST topology.

Tech	Fingered	ΔV_{HYST} [mV]	Power AVG [mW]	T_{PD} [ps]
45 nm	Without	149 ± 6.44	2.03 ± 0.074	373 ± 3.77
45 nm	With	123 ± 9.61	2.02 ± 0.143	334 ± 9.32
180 nm	Without	175 ± 9.59	11.8 ± 0.554	260 ± 9.62
180 nm	With	151 ± 12.8	12.5 ± 0.889	240 ± 13.2

Table 4. Statistical metrics of ΔV_{HYST} Monte Carlo distributions for fingered ST configurations.

Tech	Topology	Jarque–Bera	Kurtosis	Skewness
45 nm	Conventional 6T	5.449	58.775 m	254.037 m
45 nm	Modified	5.22	−79 m	−247.149 m
45 nm	P-type	86.229 m	−23.785 m	29.888 m
180 nm	Conventional 6T	1.175	−172.796 m	81.533 m
180 nm	Modified	239.408 m	−39.11 m	49.904 m
180 nm	P-type	7.633	145.489 m	293.793 m

The results of the Monte Carlo in terms of hysteresis behavior (Tables 1–3), fingered layouts collectively present a modest upward shift in the mean hysteresis width for the modified STs. Specifically, at 45 nm, ΔV_{HYST} increases from 150 mV to 154 mV. A similar trend is observed in the 180 nm node. These gains are accompanied by a slight reduction in σ, suggesting improved statistical consistency. However, the P-type ST deviates from this trend: fingering reduces both the mean ΔV_{HYST} (by ~17% in 45 nm and ~14% in 180 nm) and distribution symmetry, pointing to potential mismatch amplification due to mobility variations inherent in segmented PMOS devices.

Propagation delay exhibits a consistent reduction of approximately 8–10% across all topologies when using fingered devices, while average power consumption increases by 15–20%. Among the tested configurations, the modified ST achieves the lowest delays, and the P-type ST sustains the least power overhead.

Statistical distribution analysis, detailed in Table 4, further supports these trends. The Jarque–Bera test values for fingered conventional and modified STs remained low (≈5.2–5.4), indicating mild deviation from normality and suggesting predictable statistical behavior. In contrast, the P-type ST shows significant non-Gaussian characteristics, with a skewed and heavy-tailed distribution. Figure 7 illustrates these differences visually, highlighting the tighter and more centralized ΔV_{HYST} distributions in fingered NMOS-based designs relative to their P-type counterpart. Following the statistical characterization provided by the Monte Carlo analysis, which emphasizes the impact of random local variations on ST behavior, a third set of simulations are designed to systematically assess deterministic variations stemming from global process conditions and environmental factors. This analysis is carried out for the 45 nm technology, using a fixed transistor width of 6 μm.

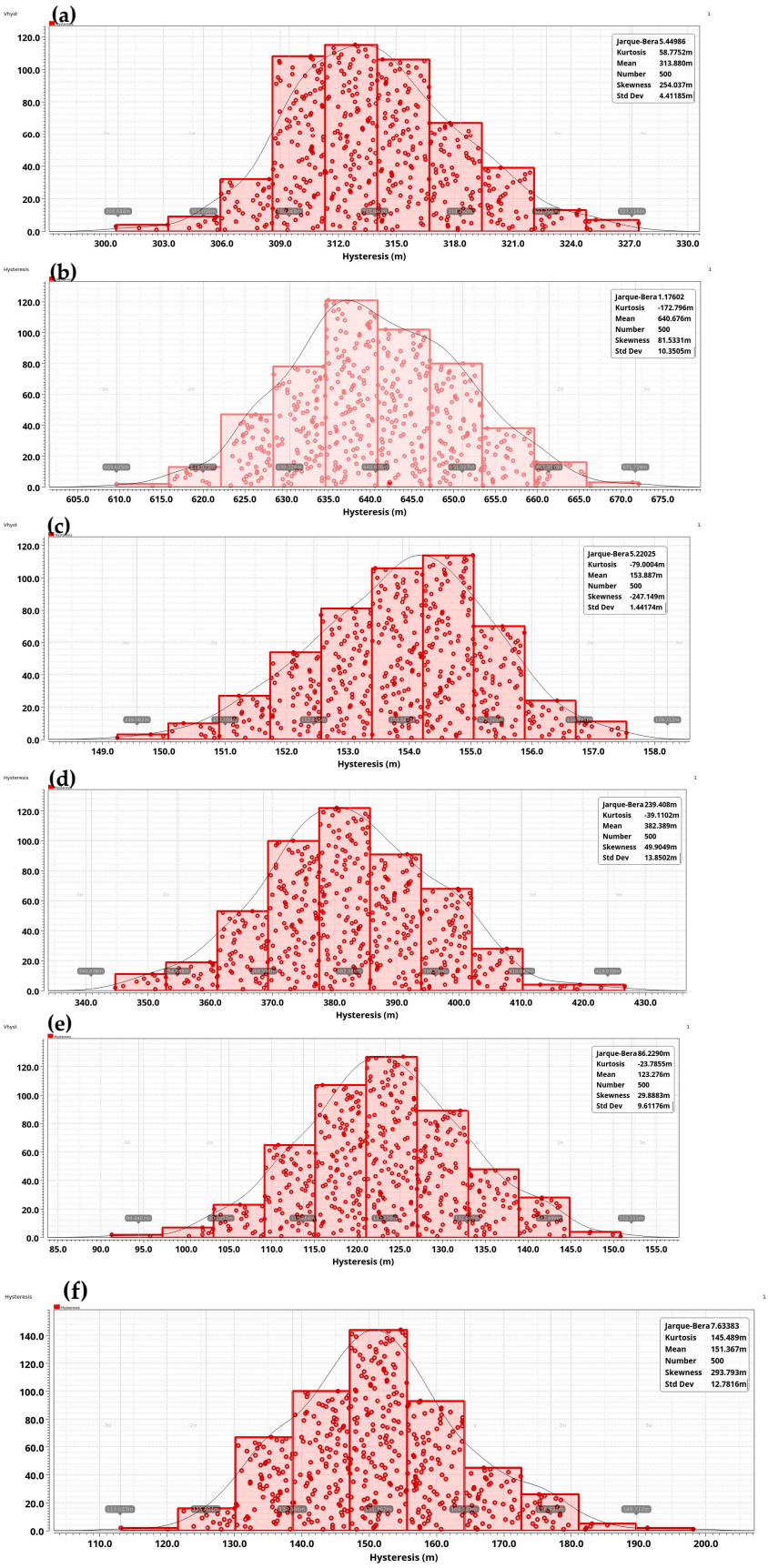


Figure 7. Histogram distributions of ΔV_{HYST} for fingered ST circuits: (**a**) conventional 6T ST 45 nm, (**b**) conventional 6T ST 180 nm, (**c**) modified ST 45 nm, (**d**) modified ST 180 nm, (**e**) P-type ST 45 nm and (**f**) P-type ST 180 nm.

4.3. Process Corner and Temperature Stress Testing of ST with and Without Fingered Topologies in 45 nm Technology

As the width of a transistor increases, the layout area and gate resistance also increase. The fingered layout technique mitigates these limitations by splitting a wide transistor into N_f narrower segments connected in parallel, preserving total width while W_{Total} improving layout compactness and electrical performance. This approach is especially beneficial in high-current, high-speed circuits such as power-oriented ST drivers, where parasitic effects and drive capability must be balanced. For each aforementioned ST topology, performance is evaluated under five standard process corners: typical-typical (TT), fast-fast (FF), slow-slow (SS), slow-fast (SF), and fast-slow (FS). Within each corner, simulations were conducted at three operating temperatures: −40 °C, 27 °C, and 120 °C, representing cold, nominal, and hot conditions, respectively. These temperature points are chosen to stress the circuit under realistic and extreme conditions. Specifically, simulations at 120 °C exacerbate the limitations of SS devices, further reducing carrier mobility and highlighting worst-case performance. Conversely, −40 °C accelerates device operation, particularly in FF conditions, emulating scenarios with active cooling, as seen in high-performance systems. The inclusion of the nominal 27 °C provides a reference for standard operating environments.

To assess the impact of layout structure, both fingered and non-fingered transistor implementations were included in the study. This yielded six configurations per process corner, combining all layout and temperature variants. Three performance metrics were extracted from each simulation: ΔV_{HYST}, average power consumption, and T_{PD}. The complete set of results is visualized using grouped bar charts for each topology (Figures 8–10), where the x-axis corresponds to the process corner and each group contains six bars for the respective layout and temperature conditions.

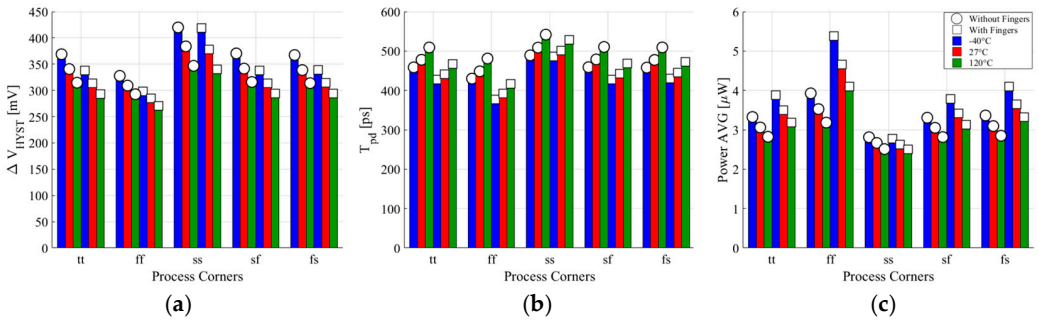


Figure 8. Corner and temperature stress testing for the conventional 6T ST: (**a**) hysteresis, (**b**) delay and (**c**) power metrics.

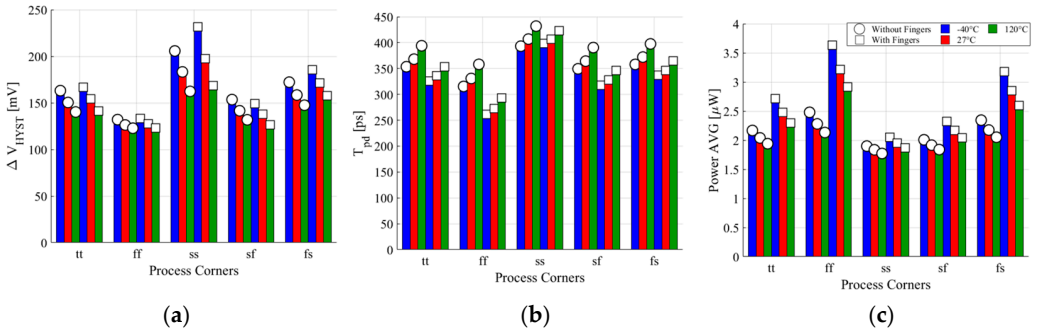
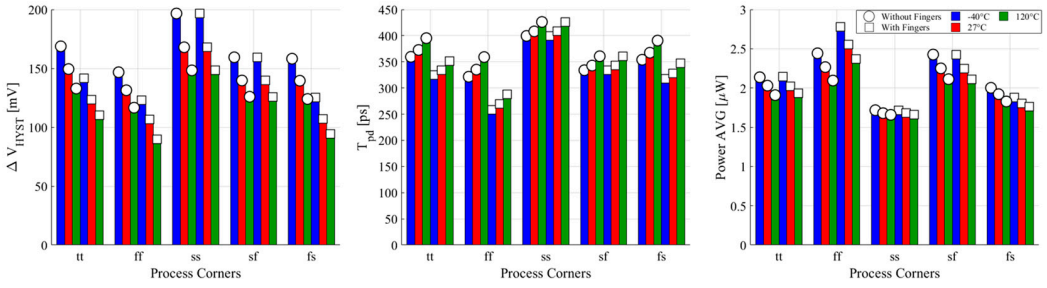


Figure 9. Corner and temperature stress testing for the modified ST: (**a**) hysteresis, (**b**) delay and (**c**) power metrics.



(**a**) (**b**) (**c**)

Figure 10. Corner and temperature stress testing for the P-type ST: (**a**) hysteresis, (**b**) delay and (**c**) power metrics.

Across all topologies, ΔV_{HYST} exhibits substantial variation in the non-fingered configurations, with spreads reaching up to $\pm 12\%$ between extreme corners (SS at 120 °C vs. FF at -40 °C). In contrast, fingered implementations show a reduced span of approximately $\pm 8\%$, demonstrating improved stability of the switching threshold under process and temperature stress.

Propagation delay follows a similar trend. Non-fingered STs ranged from 250 ps under FF at -40 °C conditions to over 520 ps at SS at 120 °C, highlighting sensitivity to both mobility degradation and threshold shifts. Fingered layouts effectively reduce this variability, confining delays to the 270–460 ps range. The worst-case slowdown is mitigated by approximately 12%, while high-speed performance under FF corners is only marginally affected ($\sim$8% overhead), preserving rapid response in favorable conditions.

Power consumption exhibits broader fluctuations driven by temperature dependence, with both configurations showing swings of approximately $\pm 25\%$ across the PVT space. Fingered implementations consistently consume 10–15% more power than their non-fingered counterparts across all conditions. Notably, however, the peak power at the SS at 120 °C corner is slightly reduced in the fingered case, likely due to improved channel uniformity limiting subthreshold leakage.

4.4. Post-Layout Impact of Fingered Layout on Modified ST in 45 nm Technology

To evaluate the combined effects of layout parasitics and fingered transistor structures, a detailed simulation is conducted on the Modified ST topology implemented in 45 nm technology. Simulations are performed both before and after post-layout extraction. In the layout extraction process, parasitic elements are extracted via Quantus. Two layout variants are compared: one using a layout without a fingered transistor structure and another employing fingered transistors with equivalent total width, as visually depicted in Figure 11. To ensure a consistent comparison, dummy transistors are intentionally omitted from both layouts, allowing a direct evaluation of the electrical and parasitic differences between fingered and non-fingered implementations without introducing layout-dependent artifacts. For this comparison, a total transistor width of 6 µm is used for both variants, with 50 fingers chosen for the variant with fingers. Performance metrics including ΔV_{HYST}, average power consumption, T_{PD}, and rise/fall times are measured and summarized in Table 5.

As the width of a transistor increases, the layout area and gate resistance also increase. The fingered layout technique mitigates these limitations by splitting a wide transistor into N_f narrower segments connected in parallel, preserving total width while W_{Total} improving layout compactness and electrical performance. This approach is especially beneficial in high-current, high-speed circuits such as power-oriented ST drivers, where parasitic effects and drive capability must be balanced. Prior to parasitic extraction, fingered and non-fingered layouts exhibited similar performance trends, with the fingered version offering a

modest increase in ΔV_{HYST} (150.4 mV → 154 mV) and a slight reduction in propagation delay (368 ps → 335.7 ps), albeit at a higher power cost (2.039 µW → 2.479 µW). However, post-layout results reveal a striking performance divergence. While the non-fingered design maintains roughly the same delay (~367 ps), the fingered layout achieves a dramatic reduction in propagation delay to just 90.5 ps, over 75% faster.

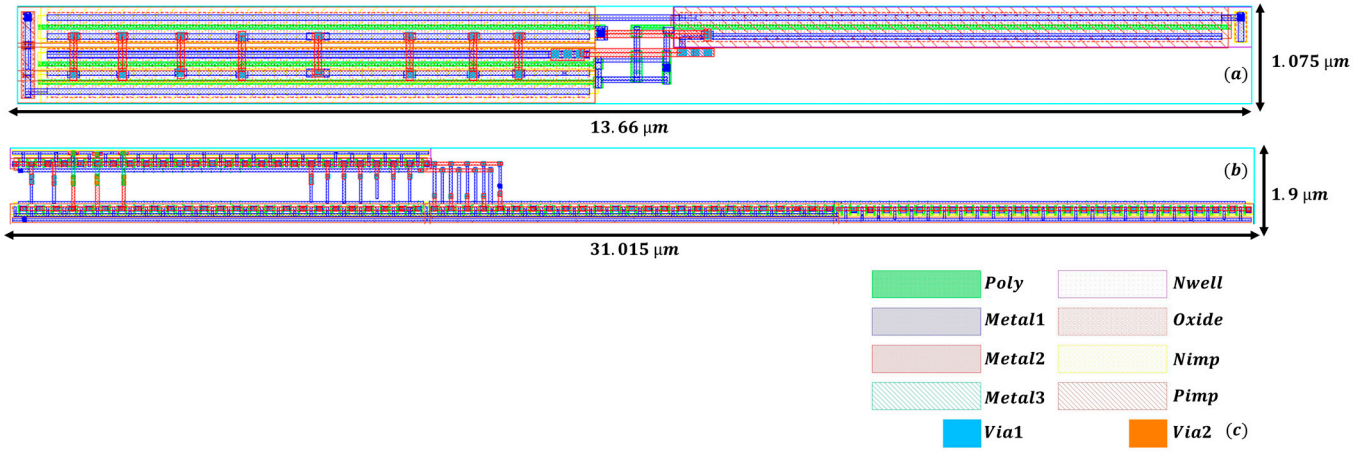


Figure 11. Layout of the modified ST (**a**) without fingers, rotated 90° clockwise for display clarity, (**b**) with fingers and (**c**) layer key showing active, poly, diffusion, and metal regions.

Table 5. Pre- and post-layout performance metrics of modified ST in 45 nm technology for non-fingered and fingered layouts.

Layout Type	Fingered	ΔV_{HYST} [mV]	Power AVG [mW]	T_{PD} [ps]	T_{RISE} [ps]	T_{FALL} [ps]
Pre	Without	150.4	2.039	368	368	232.3
Pre	With	154	2.479	335.7	335.7	224.8
Post	Without	142.9	1.987	367.4	367.4	239.4
Post	With	154.7	1.658	90.49	90.49	88.22

This substantial speed gain is attributed to the more uniform and symmetric parasitic distribution inherent in fingered structures, which balances interconnect and gate capacitances and shortens critical paths. Additionally, average power consumption in the post-layout fingered design drops below that of the non-fingered variant (1.658 µW vs. 1.987 µW), suggesting that the fragmented gate architecture helps suppress effective switching energy once full routing capacitance is included.

The hysteresis window widens further in the fingered layout post-extraction, reaching 154.7 mV an 11% improvement over the pre-layout baseline. This confirms that layout uniformity and symmetry not only enhance performance but also reinforce noise margins and switching robustness.

4.5. Post-Layout EM/IR Characterization and Layout-Aware Reliability Analysis of the Modified ST

To evaluate the impact of layout and reliability, an EM and IR-drop analysis is conducted on the modified ST topology using 45 nm CMOS technology, under post-layout conditions with extracted parasitic. The analysis is conducted using a total transistor width of 6 µm, with the fingered version implemented using 50 fingers. Three critical nets are examined: the power supply (V_{DD}), the output node (V_{OUT}), and the internal interconnect (Net 1) connecting the source of M_2 to the drain of M_1, as illustrated in Figure 2b. For each net, the number of extracted resistive segments (R Count), the normalized current density

(J/J_{MAX}), and the maximum IR voltage drop are evaluated with and without the use of a fingered layout.

The results, summarized in Table 6, show that fingered segmentation significantly improves reliability at the global and output nets. For V_{OUT}, J/J_{MAX} drops by nearly 80%, and IR drop decreases by 75% (1.59 µV → 0.40 µV), enhancing signal integrity and mitigating EM stress. Similar trends are observed for V_{DD}. These improvements arise from the wider lateral distribution of current paths and the higher R Count (e.g., V_{OUT}: 15 → 474), which reduce localized current crowding.

Table 6. Comparison of EM/IR analysis metrics for the modified ST under fingered and non-fingered layouts in 45 nm technology.

Net	Fingered	R Count	J/J_{MAX} [m]	MAX Drop [µV]
V_{DD}	Without	2	8.271	1.259
V_{DD}	With	183	10.6	4.06
V_{OUT}	Without	15	4.04	1.587
V_{OUT}	With	474	0.848	0.401
Net 1	Without	31	0.373	0.155
Net 1	With	346	23	33

However, for Net 1, located along the critical internal signal path, fingering results in a sharp degradation in reliability indicators: J/J_{MAX} spikes from 0.373 to 23, and IR drop increases from 0.155 µV to 33 µV. This is due to current concentration through densely routed, narrow channels introduced by segmentation, indicating a routing bottleneck.

Physical area analysis further reveals that the fingered layout expands from 14.68 μm^2 to 58.93 μm^2, trading vertical compactness for horizontal spread. While this incurs a 4× area increase, the benefits in speed, power, hysteresis margin, and reliability, especially at the output stage, outweigh the spatial cost for high-performance applications.

4.6. Optimizing Finger Count in Modified ST

To deepen the analysis of layout-related trade-offs in ST design, an experiment is conducted to determine the optimal number of transistor fingers (N_f) under a fixed total transistor width (W_T). The experiment focuses on the modified ST topology, implemented in both 45 nm and 180 nm CMOS technologies. Three representative transistor widths are selected to represent small, medium, and large device configurations: 1.32 µm, 3.96 µm, and 5.28 µm. These widths are carefully chosen to be divisible by the minimum allowable finger width in each technology node, 120 nm for 45 nm and 220 nm for 180 nm, ensuring valid layout generation for all N_f values.

For each configuration, N_f is swept from a single finger up to the maximum allowable value such that individual fingers remained within the minimum manufacturable width constraint. For instance, in the 45 nm process, up to 33 fingers are used for the 3.96 µm width, while the corresponding 180 nm implementation reached up to 18 fingers. Both technologies utilize the same total widths per configuration to isolate the influence of N_f while maintaining consistent device sizing. Transient simulations are performed for each case, extracting three key performance metrics ΔV_{HYST}, average power consumption, and T_{PD}. The performance metrics for each transistor width and technology combination are presented in Figures 12–14.

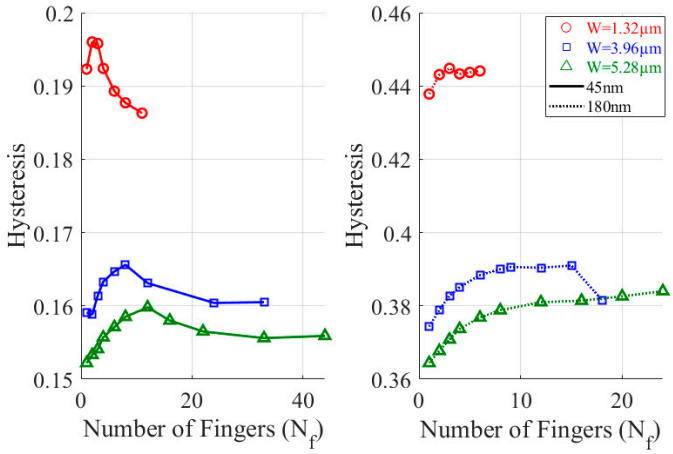


Figure 12. Hysteresis window versus number of fingers in modified ST topology for different total transistor widths. The results are presented for (**a**) 45 nm and (**b**) 180 nm.

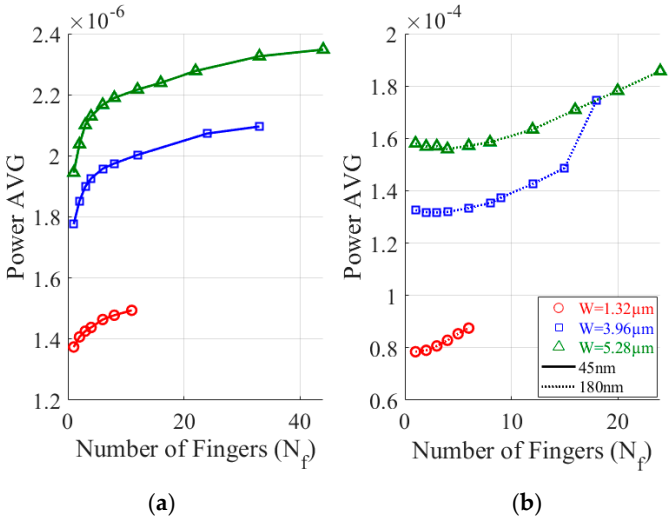


Figure 13. Average power consumption versus number of fingers in modified ST topology for different total transistor widths. The results are presented for (**a**) 45 nm and (**b**) 180 nm.

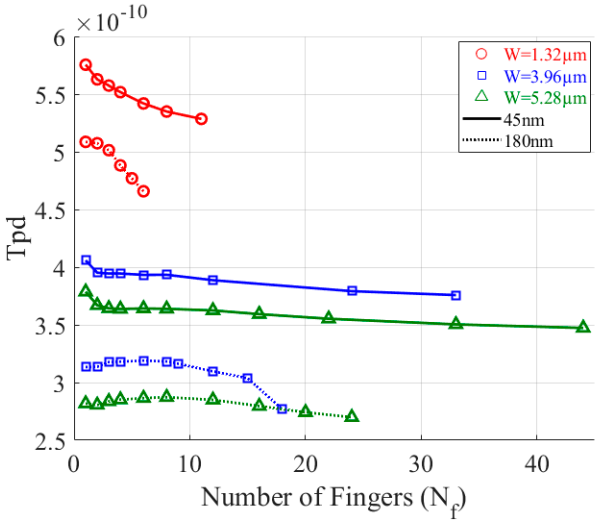


Figure 14. Propagation delay versus number of fingers in modified ST topology for different total transistor widths.

The optimal number of fingers N_f are found to be highly dependent on the total transistor width W_T and the technology node. A consistent trend emerges across all configurations:

- For small devices W_T = 1.32 µm:
  45 nm: Optimal at N_f = 4–6, where delay improves notably with minimal hysteresis degradation and ~9% power increase.
  180 nm: Best results at N_f = 5–6, maximizing all key metrics before diminishing returns.
- For medium widths W_T = 3.96 µm:
  45 nm: Optimal range N_f = 12–24; delay drops by ~35%, hysteresis peaked near N_f = 8, and power rise moderately.
  180 nm: N_f = 12–15 balanced delay and hysteresis effectively, before plateauing performance.
- For large devices W_T = 5.28 µm:
  45 nm: Minimum delay (~347 ps) and hysteresis (~0.16 V) achieved at N_f = 16–22.
  180 nm: Peak hysteresis (~0.384 V) and low delay at N_f = 20–24, despite a ~17% power increase.

Overall, segmentation beyond ~70% of the maximum legal N_f yields diminishing returns across all metrics, often degrading hysteresis due to parasitic dominance. Designers are therefore advised to target 60–75% of the maximum finger count per technology for optimal performance/power trade-offs.

5. Conclusions

This study thoroughly investigated ST topologies, focusing on their performance under technology scaling and the impact of fingered transistor implementations. Our findings consistently show that fingered layouts enhance both hysteresis robustness and switching speed across various ST configurations. While these improvements are most pronounced at smaller transistor widths and gradually diminish with increasing size, the associated modest power penalty is generally justified by the significant functional gains, especially in high-speed or noise-sensitive applications demanding sharper hysteresis.

A key insight from our Monte Carlo analysis is the nuanced effect of fingered layouts on statistical robustness. These layouts primarily improve stability in NMOS-based ST topologies, enhancing delay jitter and hysteresis margins under manufacturing variations. Conversely, in P-type implementations, fingered segmentation can degrade robustness, suggesting the need for tailored design strategies to mitigate variability in layouts. This benefit extends to deterministic robustness, where fingered layouts, despite a modest power overhead, significantly reduce variation in both delay and hysteresis, offering an advantage for timing-critical and high-reliability applications.

The analytical framework developed in Section 3 demonstrates consistent agreement with the simulation results reported in Section 4. Specifically, the observed hysteresis increases for moderate fingering and its saturation at larger widths (Figure 4), the delay reduction associated with distributed gate resistance (Figure 5), and the modest power overhead due to parasitic capacitance (Figure 6) match the model's expectations. Moreover, the Monte Carlo analysis confirms the predicted reduction in hysteresis variability for NMOS-weighted designs, while the P-type implementations exhibit the anticipated sensitivity linked to hole mobility and edge parasitics. These correlations reinforce the validity of the analytical model and highlight its ability to predict the performance of fingered ST circuits across technology nodes.

A significant, counterintuitive discovery of this research is that fingered configurations in the 45 nm modified ST circuit show substantial performance improvements post-layout extraction. We observed a remarkable 75% reduction in T_{PD}, alongside improved rise/fall

times and even a decrease in power consumption. This striking result underscores the limitations of schematic-level models in fully capturing the benefits of fingered structures. It unequivocally emphasizes that the true performance of fingered transistors is inherently tied to the physical layout, making post-layout simulations essential early in the design flow for optimized circuit realization. Significant efforts have been made to ensure that the layout designs are of optimal density and placement. In any case, there is room for improvement. The authors acknowledge that different transistor arrangements can substantially impact the results. Future studies will facilitate high precision in this area.

Furthermore, our reliability analysis demonstrates that finger segmentation significantly enhances EM and IR drop robustness in global and output interconnects. However, this benefit does not uniformly apply to internal signal paths, where aggressive fingering can lead to localized current concentration and degraded reliability. This dichotomy stresses the importance of applying finger segmentation judiciously, considering both parasitic effects and reliability concerns. In essence, while fingered layouts universally improve ST performance, the optimal selection of N_f is paramount. Our study provides a data-driven framework, showing that well-planned optimization of finger count, precisely tailored to specific device width and technology nodes, is indispensable for balancing speed, hysteresis, and power, thereby enabling high-performance and power-efficient ST implementations in advanced CMOS applications.

Finally, it should be acknowledged that layout-dependent phenomena such as Work-function Poly Etching and Shallow Trench Isolation have become increasingly significant in advanced technology nodes such as the 45 nm nodes. These effects can substantially influence key device parameters, including threshold-voltage variability, leakage behavior, and parasitic capacitances. Their interaction with fingered transistor layouts may further impact both performance and reliability in complex and nonlinear ways. Similarly, advanced layout strategies such as common-centroid structures would significantly help mitigate mismatch and enhance layout symmetry, particularly in hysteresis-critical designs. Although these mechanisms were beyond the scope of the present study, future work will aim to incorporate their influence within the analytical and experimental framework, enabling a more comprehensive understanding of layout-induced variability in scaled CMOS technologies.

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