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A Novel Reconfigurable Gate-Biasing Technique for Extending Dynamic Range in CMOS RF-DC Rectifiers Targeting RFEH Applications

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Abstract: This paper presents a novel fully integrated radio frequency (RF) rectifier tailored for a wide power dynamic range (PDR) with multiband adaptability to efficiently convert AC RF power into DC power. The proposed rectifier utilizes the strength of interstage gate biasing to achieve high power conversion efficiency (PCE) across a broad range of input power levels. Through its reconfigurable mode, the circuit seamlessly transitions between a low-power path and high-power path to ensure optimal performance across a wide PDR. Simulated using CMOS 65 nm technology, the post-layout assessment reveals a peak PCE of 48.8% at 900 MHz and 46.4% at 1800 MHz, with an extensive PDR of 20 dB for PCE exceeding 20% at both frequencies.

Keywords: RF energy harvesting; RF-DC rectifier; PDR; PCE; multiband

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1. Introduction

The Fourth Industrial Revolution (IR 4.0) has catalyzed advancements in IoT systems, pushing a greater demand for energy-efficient, low-power devices that can operate autonomously over extended periods [1]. In IoT and wireless sensor networks (WSN), low-power nodes are increasingly being deployed in remote locations or hard-to-reach environments, where the traditional battery-powered solutions are not viable due to maintenance and replacement challenges. This has led to the development of innovative technologies, like radio frequency energy harvesting (RFEH), which enables battery assist to these low-power devices, effectively extending their operational lifetimes or reducing the dependency on conventional power sources [2,3]. The flexibility of RFEH systems allows IoT devices to be deployed in diverse applications, such as biomedical sensors, wearables, and consumer electronics. Hence, it requires features, like a wide input power range and multiband adaptability, to ensure reliable energy harvesting and power conversion in dynamic and unpredictable conditions.

In radio frequency energy harvesting (RFEH) systems, the ability to operate efficiently across a wide input power range is crucial due to the variable nature of ambient RF energy sources. In fact, recent studies [4–7] have extensively explored the potential of RFEH systems operating in the microwatt power range, which is critical for enabling self-powered devices in applications. These works demonstrate that even under ultra-low input power conditions, efficient rectifier design and energy management techniques can make RFEH a

viable solution for long-term autonomous operation without battery replacement. Ambient RF power levels can fluctuate significantly based on factors, such as distance from the source, environmental conditions, and the presence of obstacles [7]. A wide input power dynamic range (PDR) in RFEH systems also has direct impact on low-power devices. Since energy availability fluctuates based on RF conditions, a system that can operate over a broad power range allows devices to remain functional even when RF power levels momentarily drop. This is particularly useful for IoT sensors and wireless sensor networks, where stable operation of the RFEH system across different locations is essential for mobility and adaptability [8].

Multiband adaptability is a crucial feature in RF energy harvesting (RFEH) rectifier design, as ambient RF signals are inherently distributed across multiple frequency bands, creating a dynamic and unpredictable energy environment. A single-band rectifier has restricted performance in such dynamic environments as it becomes inefficient when the rectifier target frequency is unavailable, experiences fluctuations, or has low-power density. In contrast, a multiband rectifier [8–10] can capture and combine energy from various frequency sources—such as GSM (900 MHz, 1800 MHz), Wi-Fi (2.4 GHz, 5 GHz), and 4G/5G networks [6]—maximizing harvested power and ensuring consistent operation. This adaptability is particularly important in real-world scenarios where signal strength varies due to environmental factors, user density, and RF consumption patterns. For instance, in urban areas, 900 MHz and 1800 MHz bands are often highly saturated [11] due to widespread mobile communication usage, making them ideal reference frequencies for multiband rectifier design. By supporting multiple frequency bands, RFEH systems can maintain optimal power conversion efficiency (PCE) across diverse conditions, enhancing reliability for IoT devices, wireless sensor networks, and other low-power applications when energy availability is sporadic [10].

On-chip integration enhances circuit compactness, minimizes parasitic effects, and improves overall system efficiency by eliminating the need for external components [12]. This approach is particularly beneficial for miniaturized and low-power applications, such as biomedical implants and IoT devices, where space and power efficiency are critical. A fully integrated CMOS rectifier can be realized using CMOS technology, enabling efficient RF-to-DC conversion while maintaining a small footprint, PCE, and extended PDR [13].

There are many types of CMOS rectifier configurations in the RFEH system. The commonly used configurations are Dickson and cross-coupled differential drive (CCDD) rectifiers, as shown in Figures 1a and 1b, respectively. Due to the voltage drop of diode configuration, Dickson rectifier suffers from poor sensitivity at low RF input power, which will affect the overall performance for low-power devices [14]. CCDD was first introduced by [15], reporting good energy conversion efficiency PCE up to 67.5% at 953 MHz. Unlike single-ended topology, like the Dickson rectifier, the differential configuration is evaluated to be more effective as it eliminates the diode voltage and uses the CMOS transistors as switches, giving low ON-resistance in forward bias, thus improving the sensitivity. Therefore, CCDD topology has a relatively high PCE in low-power regions but suffers from dropped efficiency in high-power regions due to leakage currents.

Prior rectifier designs employed body-biasing techniques by modulating the bulk voltage to decrease the threshold voltage of CMOS transistors in conventional CCDD to improve sensitivity [16]. However, this approach is constrained by the maximum V_{sb}, leading to very narrow PDR at 8 dB [17,18]. While [19] achieves a high sensitivity of −38 dBm using feedback self-adaptive body biasing, its performance is degraded significantly at high input power levels, limiting its practical applicability.

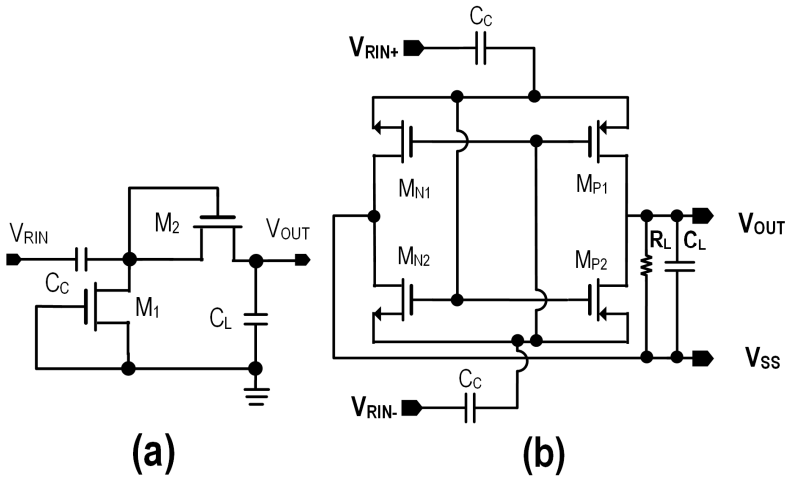


Figure 1. Commonly used CMOS rectifier topologies: (**a**) Dickson, (**b**) CCDD.

Other than body biasing, gate biasing is another considerable way to improve the performance of CCDD rectifiers. Referring to the CCDD rectifier architecture in Figure 1b, CMOS transistors' source terminal is tied to the RF input (RF+/RF−), and the drain is connected to the output (V_{out}). Hence, gate biasing is the most suitable approach as it can be independently controlled without interfering with RF signals or the DC output, whereas biasing the source or drain is impractical as it would disrupt the RF input signal or introduce unwanted loading effects on the output. The self-gate biasing mechanism is introduced to dynamically adjust V_{GS}, enhancing conduction during positive rectification. Key methods include using feedback resistors [20,21], diodes [22], diode-connected MOSFETs [23–26], and non-linear self-gate biasing [27], which suppress reverse leakage current at high output power, thereby extending PDR to the high power side. Interstage gate-biasing is also employed by [28,29] to enhance conduction at low RF amplitudes, but the biasing voltage increases proportionally with the number of rectifying stages that results in large V_{GS} swings on the high power side, leaving narrow PDR at a low input power level. Another gate-biasing technique is the bootstrapping circuit [30,31], which employs capacitors to store and transfer a more negative bias voltage to the gates of PMOS rectifying transistors, enabling high power conversion efficiency (PCE) at low input power levels. Ref. [31] advanced this prior design by incorporating a bootstrapping clamper with the dynamic threshold reduction (DTR) technique, thereby extending high PCE operation from 60 MHz in [30] up to 402 MHz and 953 MHz, showing multiband adaptability. However, a key limitation is their narrow power dynamic range (PDR), making them less suitable for ambient energy harvesting applications where input power can vary significantly. In this work, the proposed design introduces reconfigurable operation modes by employing the interstage gate-biasing technique, which can dynamically switch between low-power and high-power paths to maintain optimal efficiency across a wide PDR. This adaptability ensures robust performance in real-world scenarios with fluctuating RF energy availability.

The purpose of this work is to improve the PDR of the CMOS rectifier to be suitable for a multiband environment with dynamic input power. To enhance PDR, a few studies propose reconfigurable mode rectifiers, such as stage variation, dual-path, and hybrid topologies. Stage variation rectifiers [32–35] dynamically configure the number of active rectifier stages to boost the DC voltage in low-power mode and minimize conduction loss in high-power mode. Dual-path rectifiers [36,37] integrate low-power and high-power rectification paths into a system to maximize the PCE at both regions. Three-mode reconfigurable rectifiers [38] employ stacked CCDD architectures, dynamically modulating transistors' length to suppress the leakage current across low-, medium-, and high-power zones, further

extending the PDR. It is observed that most of the reconfigurable rectifiers primarily focus on optimizing the high-power zone by reducing conduction loss or mitigating leakage. This approach inherently limits the power conversion efficiency (PCE) at low input power due to the minimum sensitivity threshold of the CCDD architecture, where the rectifier fails to efficiently convert RF energy below a certain input power level. However, due to the structural constraints of CCDD, there are no significant architectural modifications to enhance performance at low power levels. As a result, the PDR extension remains limited on the low-power side, restricting their effectiveness in ambient energy harvesting environments where ultra-low power operation is essential for reliable energy conversion.

This paper proposes an enhanced fully integrated reconfigurable rectifier, using dual-mode single-path interstage gate-biasing technique to extend the high PCE range (or PDR) at both low and high input power. Section 2 explains the working principle of the proposed work and the realization of the circuit. Section 3 presents the experimental results. Lastly, a conclusion is drawn in Section 4.

2. Proposed Work

2.1. Background

Figure 2 illustrates how CCDD rectifiers suffer from current leakage at high RF input power, limiting their PDR. This occurs when the PMOS has sufficient V_{SG} to turn on the transistors while the output voltage exceeds the RF signal amplitude, causing current reverse flow from the output back to RF input, through the PMOS. To address this issue, gate biasing on the PMOS is introduced as an optimal solution to extend PDR, as it provides better control over the transistor's conduction characteristics. In the CCDD architecture, the drain-to-source current (I_{DS}) follows Equation (1) when it is in saturation region, where the gate-to-source source voltage (V_{GS} for NMOS or V_{SG} for PMOS) plays a crucial role in determining conduction behavior.

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2 \quad (1)$$

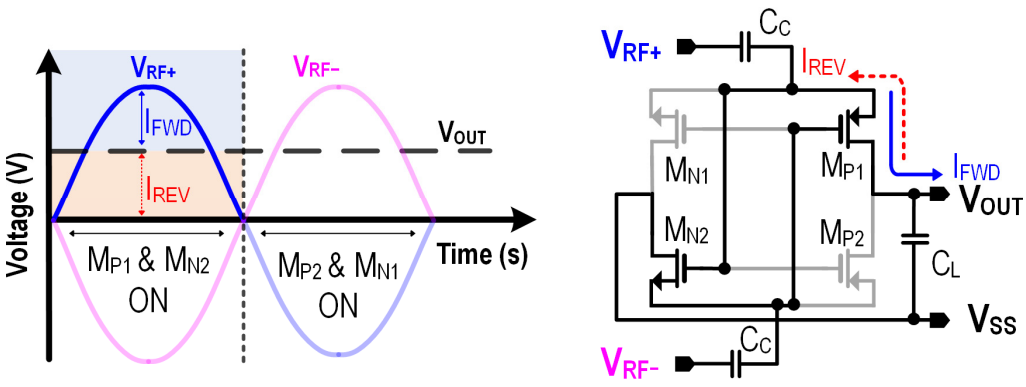


Figure 2. Illustration of reverse leakage current on CCDD rectifiers when $V_{OUT} > V_{RF}$.

At low RF power, a large V_{SG} for PMOS is required to lower the effective threshold voltage (V_{TH}), ensuring strong conduction despite the weak RF input. Conversely, at high RF power, excessive V_{SG} swings can lead to reverse conduction, where transistors turn ON while the output terminal has higher potential, causing reverse leakage current which reduces efficiency. By dynamically adjusting V_{GS} or V_{SG} based on input power, gate biasing enhances conduction at low power and suppresses leakage at high power, significantly extending the PDR. As mentioned in the introduction, source or drain biasing lacks adaptability, gate biasing offers precise control over conduction characteristics, making it the most effective approach for improving PCE and overall rectifier performance in CCDD.

The gate-biasing technique can affect the ON resistance of the CMOS transistors, as given by Equation (2):

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})} \quad (2)$$

where: μ_n is the carrier mobility, C_{OX} is the gate oxide capacitance, W/L is the transistor ratio, V_{GS} is the gate-to-source voltage, V_{TH} is the threshold voltage. By increasing $V_{GS} - V_{TH}$, R_{ON} could be lowered and thus less RF input power is required to turn on the transistors. At low input power, this technique ensures $V_{GS} - V_{TH}$ remains sufficient for conduction, improving rectifier sensitivity. However, at high input power, a high gate-biased voltage will cause larger $V_{GS} - V_{TH}$ swings which will lead to exponential growth in reverse leakage current, as described by Equation (3):

$$I_{rev} = \mu_n C_{ox} \frac{W}{L} V_t^2 exp(\frac{V_{GS} - V_{TH}}{nV_t})(1 - exp(\frac{-V_{DS}}{V_t})) \quad (3)$$

where: V_t is the thermal voltage and V_{DS} is the drain-to-source voltage. Thus, gate-biasing requires adaptive bias control to increase/decrease the gate voltage applied to the PMOS transistors to improve sensitivity at low power and mitigate the reverse leakage current at high power.

In this work, a novel interstage gate-biasing technique is used to regulate the gate voltage, V_G of PMOS transistors in the rectifier circuit by using the signals from different rectifier stages. This paper will present a dual-mode single-path reconfigurable rectifier that integrates preceding and succeeding interstage gate-biasing configuration within a single rectification path to ensure wide PDR across low and high input power. Detailed circuit architecture and working principles are described in Section 2.2.

2.2. Architecture and Working Principle

Figure 3 shows the conceptual design architecture of the proposed dual-mode single-path reconfigurable fully integrated rectifier, which consists of a main novel rectifier for RF-DC conversion, and a comparator circuit to compare between low and high input power for adaptive switching control. The idea is to compare a target output voltage with a switching point voltage. If the target output voltage is lower than the switching point voltage, the input power is considered low, prompting the rectifier circuit to use Path 1 for rectification. Conversely, if the target voltage exceeds the switching point voltage, the circuit will use Path 2 for rectification. Building on this understanding, the proposed rectifier operates in two distinct modes: Mode 1 engages the preceding stage configuration at low input power, while Mode 2 activates succeeding stage at high input power. This approach effectively addresses both the capped sensitivity and reverse leakage issues in the CCDD rectifier.

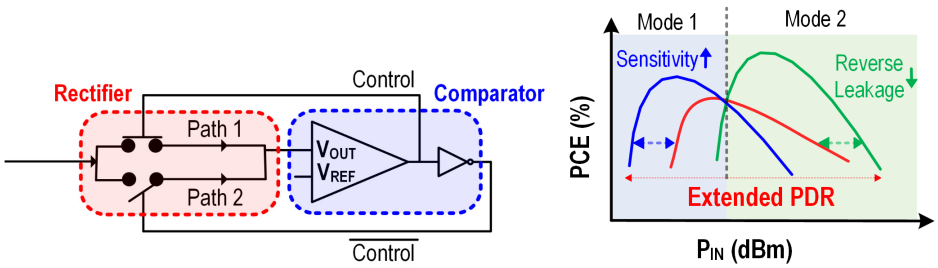


Figure 3. Design framework for the proposed dual-mode single path reconfigurable rectifier design with an adaptive control for mode switching to achieve wide PDR.

At the preceding stage, PMOS transistors are biased by the V_G of previous rectifier stage while the source V_S is still tied to the current rectifier stage. Since the V_G at the previous rectifier stage is low, V_{SG} at the current stage becomes relatively high that makes PMOS transistors easier to turn on, thereby improving the sensitivity. When the rectifier switches to the succeeding stage, PMOS transistors will be biased by the V_G of the next rectifier stage while V_S remains at the current rectifier stage, similar to the preceding biasing approach. The V_G at the next rectifier stage is higher, which will lower the V_{SG} and prevent the reverse leakage of PMOS transistors.

Preceding interstage gate-biasing can enhance the sensitivity of CCDD by providing a lower V_G from the previous rectifier stage, giving higher V_{SG} for better forward conduction at low input power. However, this alone does not effectively suppress the leakage current at a high input power because static gate biasing increases, causing larger $V_{GS} - V_{TH}$ swings in the end, which lead to exponential growth in the reverse leakage current. Hence, succeeding interstage gate-biasing topology is used at a high input power to reduce the V_{GS} voltage swing, keeping transistors in the optimal conduction region.

The simulation result in Figure 4 shows that preceding and succeeding interstage gate biasing appears as a promising configuration for low and high input power rectification, respectively.

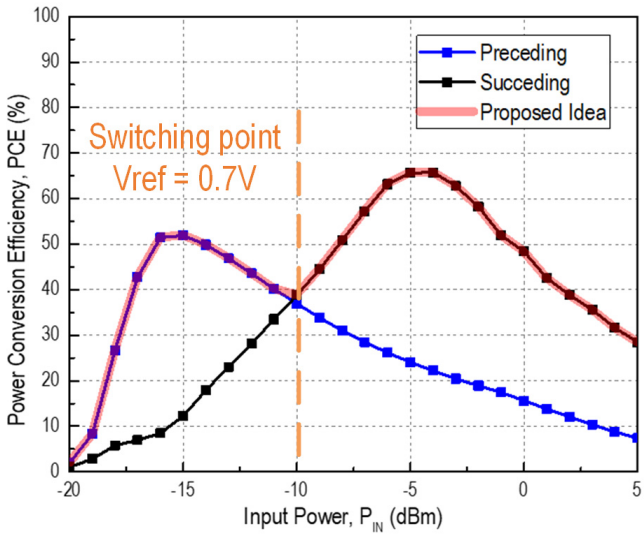


Figure 4. Simulated PCE graph from preceding and succeeding interstage gate biasing.

From Figure 4, it is observed that a narrow PDR could be obtained from either one of the gate-biasing topologies. Reconfigurable mode rectifier is proposed to combine both graphs to extend the PDR. An additional comparator circuit is introduced, making it more complex but significantly more efficient and adaptable to wide input power level. The switching point between 2 modes can also be determined from the PCE graph above, where preceding interstage gate-biasing configuration achieves wide PDR when the target output voltage is lower than 0.7 V while the succeeding interstage gate-biasing configuration is has better performance at the target output voltage higher than 0.7 V. Hence, Vref = 0.7 is selected as the switching point voltage. This mechanism ensures that the rectifier dynamically reconfigures itself to operate in the mode that provides higher efficiency, depending on the input power and load conditions.

This innovative approach addresses the limitations of the base model, making it suitable for applications requiring wide PDR and reliable rectification performance. Besides, the proposed dual-mode single-path rectifier architecture also eliminates the need for parallel rectifier architectures, which would otherwise increase chip size and power

consumption. By integrating multiple configurations into a single design using simple wiring, the design complexity can be minimized, thereby preventing degradation of the rectifier's overall efficiency.

2.3. Realization of Circuit

In TSMC 65 nm CMOS process, low-threshold-voltage transistors (LVT) are chosen to optimize the rectifier's PCE as it requires smaller gate-to-source voltage (V_{GS}) to turn on. The NMOS has the width of 1 µm while the PMOS widths are 2 µm with both having the same channel length of 60 nm. The same transistor sizing is used for both the rectifier and comparator blocks. Figure 5 shows the three-stage rectifier that integrates both preceding and succeeding circuit architecture. The circuit consists of three stages labelled as Stage A, Stage B, and Stage C. The switches in between every cascaded stage (S_1, S_2, S_3, S_4 for Mode 1 and S_A, S_B, S_C, S_D for Mode 2) are MOSFET switches, which will be controlled by the comparator logic circuit, as shown in Figure 6. For easier understanding, the circuit schematic in Figure 5 has been restructured in Figure 7 to illustrate the circuit architecture during low power (Mode 1) and high power (Mode 2).

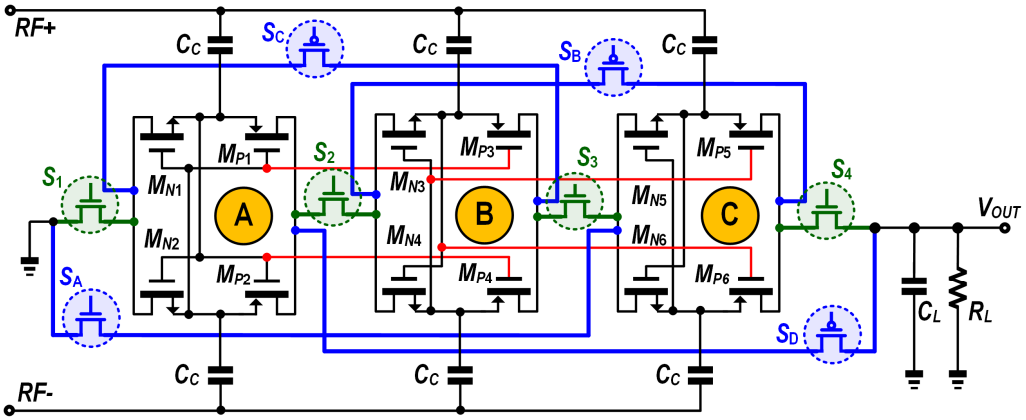


Figure 5. Schematic of the 3-stage dual-mode single-path reconfigurable interstage rectifier.

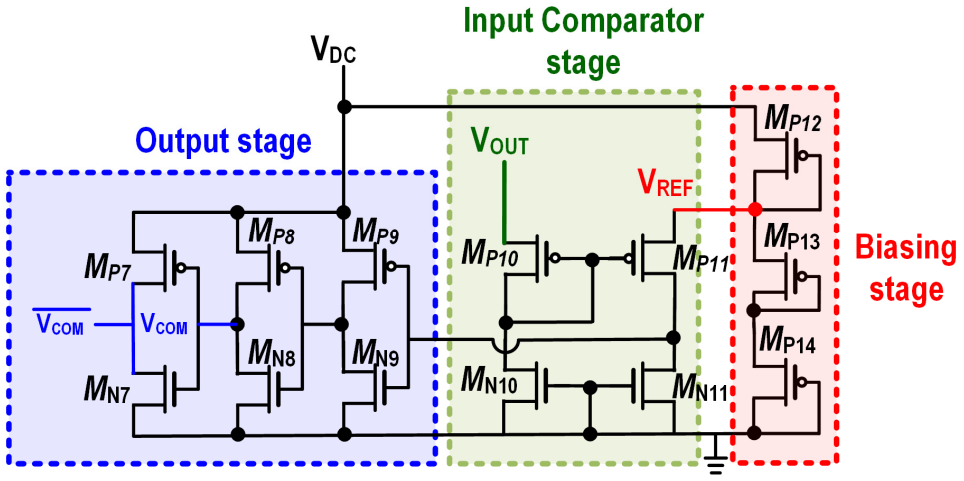


Figure 6. Schematic of comparator circuit.

At low input power, the circuit operates in Mode 1, where green switches (S_1, S_2, S_3, S_4) are turned on, while Path 2 (blue switches) remains off, ensuring that current flows only through the active switches. In this configuration, the rectifier follows a preceding interstage connection (A → B → C). Initially, Stage A begins the rectification process, followed by Stage B and Stage C, which progressively boost the rectified voltage using the stored charge

from the previous stage. Stage C completes the rectification, generating a higher DC voltage for low-power energy harvesting applications. In this mode, the PMOS transistors are gate-biased with a higher V_{SG}, reducing ON-resistance and enhancing forward conduction, thereby improving rectifier sensitivity.

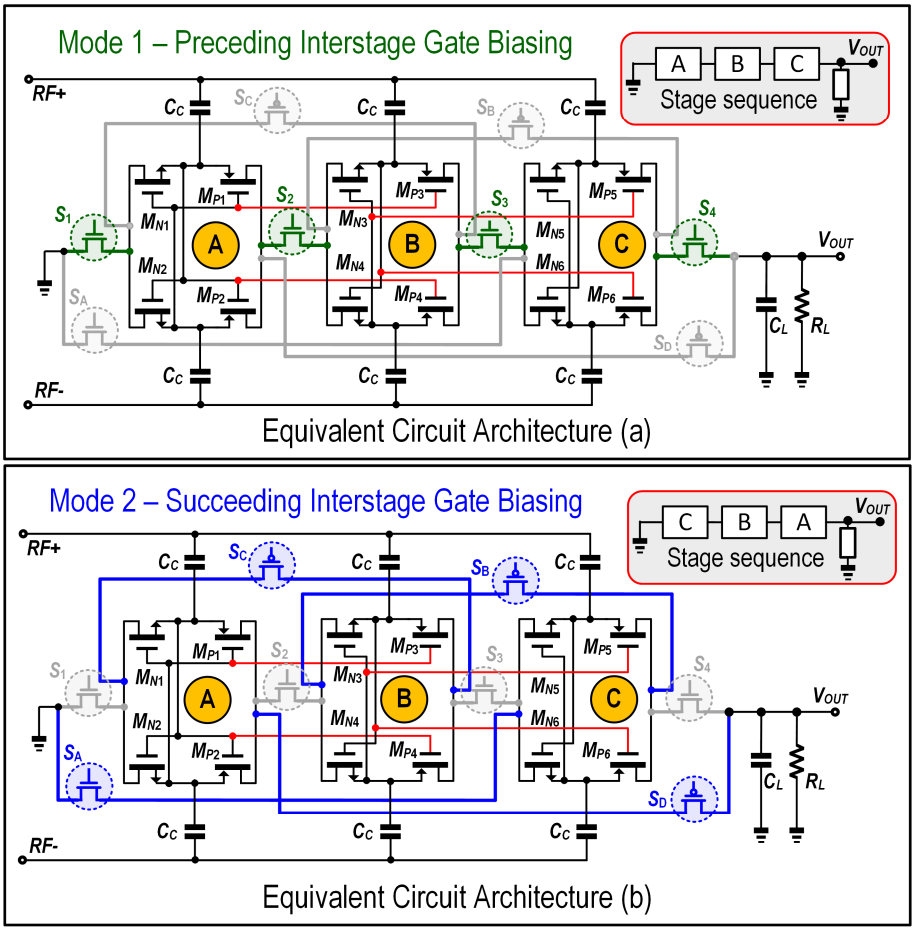


Figure 7. Equivalent circuit during (**a**) Mode 1 (for low power) and (**b**) Mode 2 (for high power).

At high input power, Mode 2 is activated as switches S_A, S_B, S_C, and S_D turn on, transitioning the circuit into a succeeding interstage configuration (C → B → A). Here, the rectification sequence is reversed, with Stage C handling the initial rectification step at high power levels using stored charge from the next rectifier stage. This prevents the early stages from overcharging and leaking current back to the RF input, effectively extending the PDR to the low-power region while maintaining efficiency at high power. Since higher input power naturally enables transistor conduction, reverse leakage current increases compared to Mode 1. To mitigate this, the rectifying PMOS transistors are biased with a lower V_{SG}, effectively reducing leakage current and ensuring stable operation at high input power levels.

Referring to Figure 6, the comparator circuit functions as a switch controller because its output will generate two main control signals, Vcom and $\overline{\text{Vcom}}$ to activate or deactivate the 8 MOSFET switching elements, S_1 to S_4 and S_A to S_D. CMOS Op-Amp is used to compare the rectifier output voltage, V_{out} with the reference voltage, Vref of 0.7 V. This reference voltage is generated using a voltage divider circuit, ensuring a stable and consistent bias point for accurate comparison. At the output stage, an inverter is added to the comparator output; this can allow two complementary switching controls to happen simultaneously. Vcom and $\overline{Vcom}$ will change based on the comparison of Vout with Vref to determine which

set of switches (Mode 1 or Mode 2) is active. The detailed control states for each mode are summarized in Table 1.

Table 1. Control signal logic for mode switching.

Switches	Control Signals	Mode 1 (Low Power) Vcom = 1.2 V Vcom = 0 V	Mode 2 (High Power) Vcom = 0 V Vcom = 1.2 V
S_1 (NMOS)	V_{COM}	ON	OFF
S_2 (NMOS)	V_{COM}	ON	OFF
S_3 (NMOS)	V_{COM}	ON	OFF
S_4 (NMOS)	V_{COM}	ON	OFF
S_A (NMOS)	$\overline{Vcom}$	OFF	ON
S_B (PMOS)	V_{COM}	OFF	ON
S_C (PMOS)	V_{COM}	OFF	ON
S_D (PMOS)	V_{COM}	OFF	ON

In this design, we utilize the TSMC 65 nm low-power (LP) CMOS process, where the threshold voltages, V_{TH} of LVT NMOS and PMOS transistors are approximately 400–500 mV. To ensure reliable switching, a VDC = 1.2 V supply is selected to power the comparator, allowing the control signals to swing between 0 V and 1.2 V. During Mode 1 operation, for example, switch S_4 must be remained "ON" before V_{out} reaches a switching point voltage of 0.7 V. At this point, the control signal corresponding to S_4 is VCOM = 1.2 V; therefore, a sufficient V_{GS} swing is still sufficient to turn on the switch when the source voltage, Vs of the switch S_4 lies within the 0–0.7 V range.

3. Experimental Results

The proposed design is implemented using 65 nm CMOS node, which occupies an effective chip area of 0.0183 mm^2, excluding the bond pad. Figure 8 shows the overall layout of the fully integrated on-chip rectifier design. In the post layout simulation, the same transistor sizing was used for both 900 MHz and 1.8 GHz operations. The detailed transistor and other device parameters are tabulated in Table 2.

Table 2. Transistor sizing table.

Devices	Type	Width/Length
M_{N1}–M_{N6}	LVT	1 µm/60 nm
M_{P1}–M_{P6}	LVT	2 µm/60 nm
S_1–S_4, S_A	LVT	1 µm/60 nm
S_B-S_D	LVT	2 µm/60 nm
M_{N7}–M_{N10}	LVT	1 µm/60 nm
M_{P7}–M_{P10}, M_{N12}–M_{N14}	LVT	2 µm/60 nm
M_{N11}, M_{P11}	LVT	600 nm/60 nm
R_L	-	100 kΩ
C_C	MIM	1 pF
C_L	MIM	5 pF

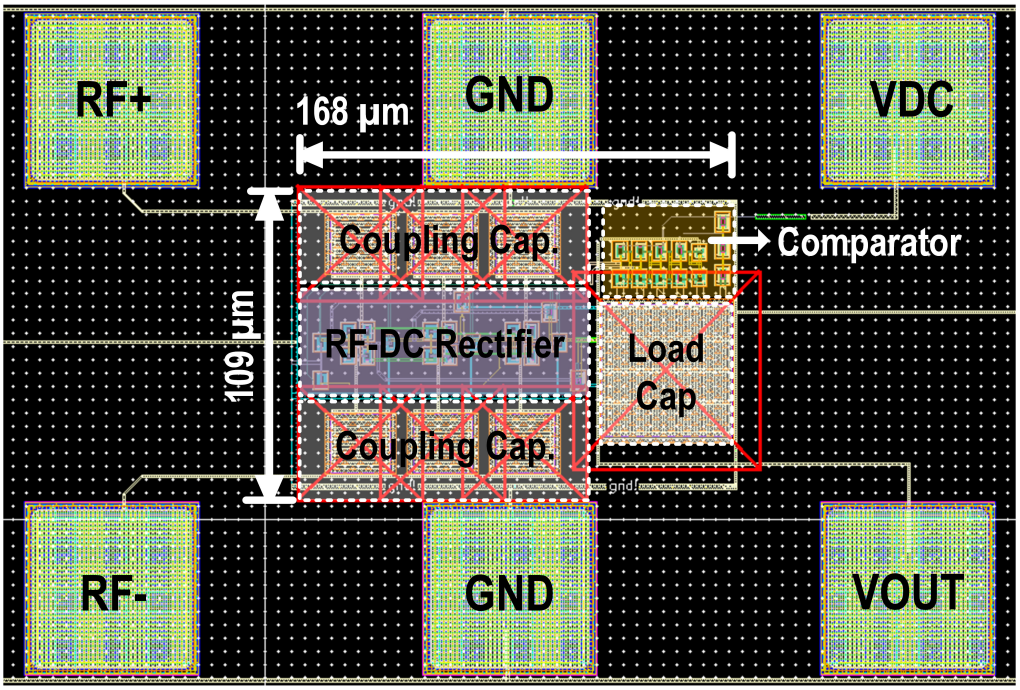


Figure 8. Layout of the proposed rectifier design.

The input power fed into the rectifier is determined by using the equation below:

$$P_{in,\,REC} = P_R - P_{Reflect} = P_R\left(1 - |S_{11}|^2\right) \tag{4}$$

$$|S_{11}|^2 = |\Gamma|^2, \tag{5}$$

$$where\ \Gamma = \frac{Z_{REC} - Z_{antenna}}{Z_{REC} + Z_{antenna}}$$

P_R is the input RF incident power received from the antenna and $|S_{11}|^2 = |\Gamma|^2$ is the power reflection coefficient. Taking the output from the comparator as Pout, the PCE of the rectifier can be calculated by:

$$PCE_{rectifier} = \frac{P_{out,\,DC}}{P_{in,\,REC}} \tag{6}$$

Conducting post-layout simulations under 900 MHz and 1.8 GHz with 100 kΩ load resistor and 5 pF load capacitor, the simulated graphs of PCE versus Pin of the proposed design are shown in the Figure 9a,b. The performance result at both operating frequencies was compared respectively with a conventional cross-coupled differential drive (CCDD) rectifier and which uses with the same design parameters. In post-layout simulation, the proposed idea achieved PDR of 20 dB with peak PCE of 48.6% at −13.48 dBm in Mode 1 while peak PCE achieves 53.4% at −3.48 dBm in Mode 2 at a 900 MHz operating frequency.

At a 1.8 GHz operating frequency, there is a drop in PCE across the range of input power, giving 41.4% at −13 dBm in Mode 1, while peak PCE achieves 46.4% peak PCE at −5 dBm in Mode 2. However, the PDR still can be maintained at 20 dB, which is consistent despite varying ambient RF conditions. Figure 9 compares the proposed rectifier with the conventional CCDD [15], operating at 900 MHz and 1.8 GHz, respectively. The proposed dual-mode single-path gate-biasing technique successfully improved the PCE in a low-power region, achieving wider PDR compared to the conventional CCDD.

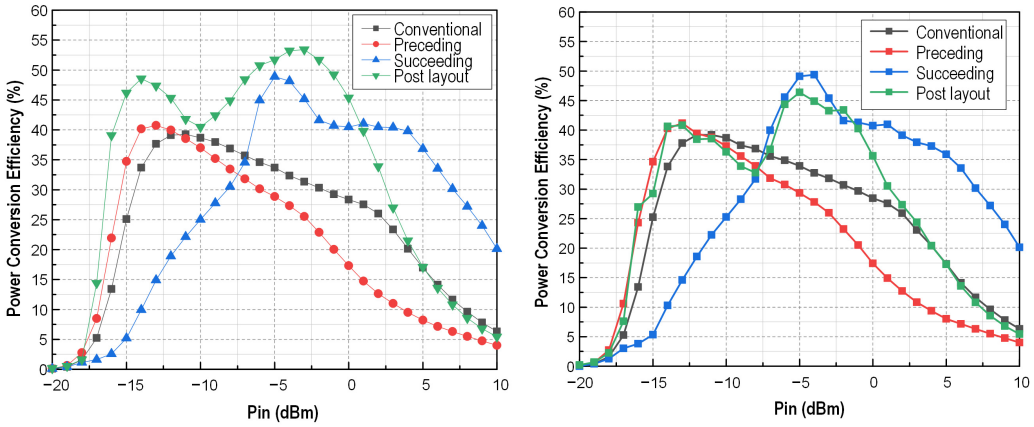


Figure 9. Post layout simulation graph of PCE in (**a**) 900 MHz and (**b**) 1.8 GHz.

Besides, additional analyses were performed to evaluate the rectifier's robustness under varying load conditions. Based on simulation analysis, the optimal load range falls between 10 kΩ and 150 kΩ as the proposed rectifier exhibits a higher PCE, more than 20%, and achieve PDR around 20 dB. A value of 100 kΩ was selected for our primary analysis as it lies within this optimized region and is commonly adopted in CMOS rectifier designs [14,15,39,40] for performance benchmarking. The performance of the proposed rectifier at 900 MHz and 1.8 GHz under various loads is shown in Figure 10 below.

Table 3 presents a comprehensive summary of rectifier's performance and comparison with previous state-of-the-art designs. Although the proposed rectifier does not achieve the highest peak PCE among the compared works, it outperforms others by offering the widest PDR, which is 20 dB. This extended PDR allows the rectifier to efficiently operate across a broader range of input power levels, making it more versatile and suitable for various RF energy harvesting applications, including ultra-low-power IoT devices and higher-power RF environments. The ability to maintain stable performance over a wide input power range highlights the robustness and adaptability of the proposed design, even if its peak efficiency is slightly lower than some prior works.

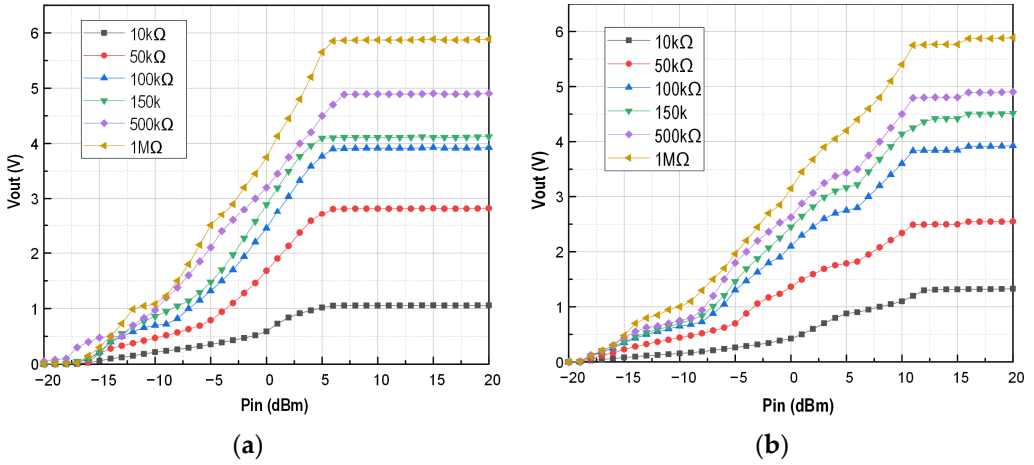


Figure 10. *Cont.*

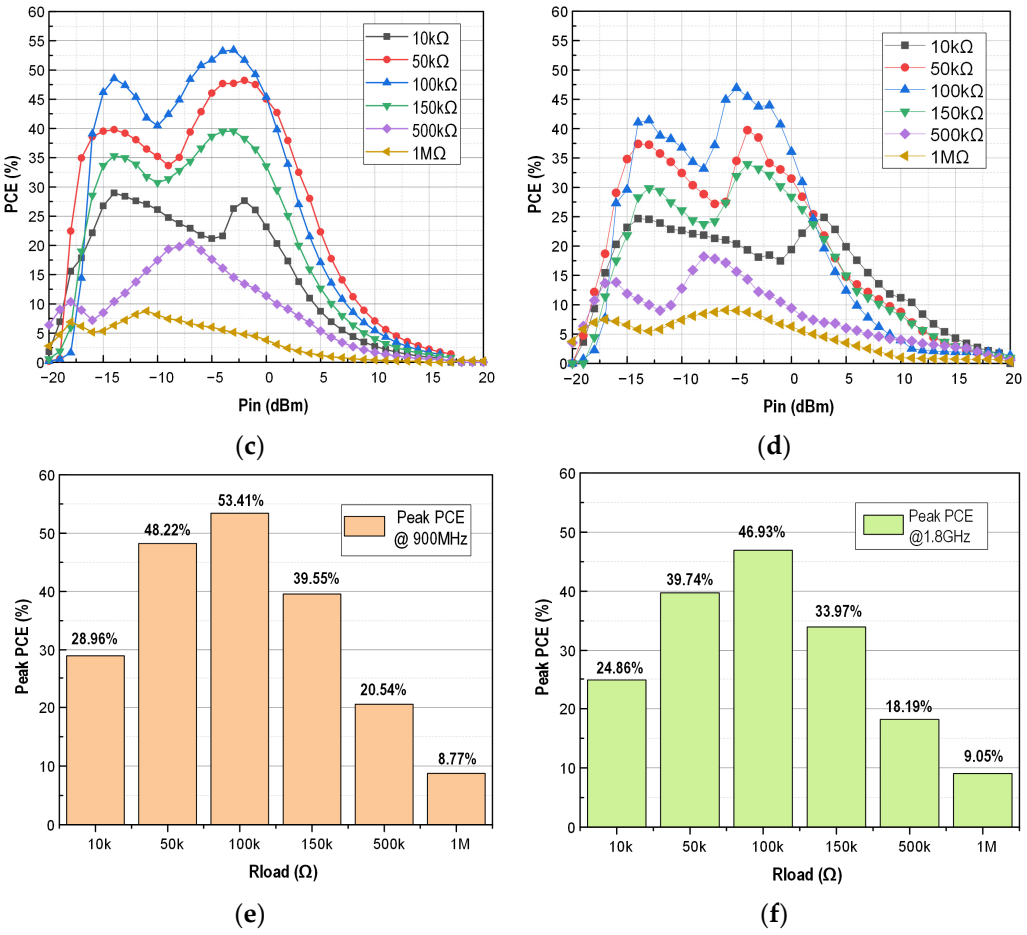


Figure 10. Performance graphs of the proposed rectifier under various loads. Simulated Vout against Pin in (**a**) 900 MHz and (**b**)1.8 GHz. Graphs of PCE against Pin in (**c**) 900 MHz and (**d**) 1.8 GHz. Peak PCE performance at (**e**) 900 MHz and (**f**) 1.8 GHz.

Observing the table above, the proposed rectifier design achieves a balanced trade-off between performance metrics. While its peak PCE (48.8% @ 900 MHz, 46.4% @ 1800 MHz) is lower than in some works (e.g., [34] at 66%), it offers the widest PDR of 20 dB, ensuring stable efficiency across varying input power levels. The design also supports dual-band operation (900/1800 MHz), enhancing flexibility for applications, like IoT and RFID. Although the sensitivity (−15.4 dBm @ 900 MHz and −15.8 dBm @ 1800 MHz) is competitive, though not the best, and the effective area (0.0183 mm^2) strikes a balance between performance and integration. By prioritizing PDR and frequency adaptability over peak PCE, this design is well-suited for dynamic environments where consistent performance is critical. The objective of this research is to extend PDR in multiband scenarios; hence, the proposed circuit trades off peak efficiency for wide adaptability, making it suitable for dynamic and multiband harvesting.

Table 3. Performance benchmark with state-of-the-art CMOS rectifiers.

	[15]	[17]	[32]	[26]	[28]	**This Work** #
CMOS Tech. (nm)	180	180	130	180	130	65
Frequency (MHz)	953	915	900	900	915	900/1800
Rectifier Topology	CCDD	CCDD	Dickson	CCDD	CCDD	CCDD
Proposed Technique	Conventional	Deep-n-well Body-Biasing	Reconfigurable Stages No.	Diode-Connected Gate-Biasing	Interstage Gate-Biasing	Reconfigurable Gate-Biasing
Rectifier Stages	3	1-2-4	6–12	1	10	3
Effective Area (mm^2)	-	-	0.039	0.0088	0.029	0.0183
Output Load, R_L	100 kΩ	2.6 kΩ	100 kΩ	100 kΩ	450 kΩ	100 kΩ
Sensitivity at 1 V (dBm)	−14 @ 100 kΩ	−10 @ ∞ Ω	−21.7 @ 1 MΩ	−18.2 @ 100 kΩ	−25.5 @ 5 MΩ	−15.4 @ ∞ Ω for 900 MHz −15.8 @ ∞ Ω for 1800 MHz
Peak PCE	39.25% * @ −8.73 dBm	56.7% @ 2 dBm	34.93% @ −10 dBm	66% @ −18.5 dBm	42.4% @ −16 dBm	48.8% @ −13.48 dBm for 900 MHz # 46.4% @ −14.02 dBm for 1800 MHz #
PDR (PCE > 20%)	18 dB *	8 dB	14 dB	15 dB	12 dB	20 dB # at 900 MHz 19 dB # at 1800 MHz

* Estimated from graph; # Post-layout Simulation.

4. Conclusions

This work introduces a novel wide power dynamic range rectifier designed for RF energy harvesting systems. The rectifier can achieve a wide PDR by reconfiguring into two different topologies based on the input voltage. At low input power, it adopts a CCDD topology with preceding interstage gate-biasing configuration, leveraging low conduction loss from the cross-coupled transistor pairs. For higher input power, it switches to a succeeding interstage gate-biasing topology to minimize reverse current leakage. Using 65 nm CMOS technology, the rectifier design is fully integrated, resulting in a total effective chip area of 0.0183 mm^2. Overall, the proposed topology significantly extended the PDR to 20 dB over a wide input range from −17 dBm to 3 dBm, with multiband adaptability at 900 MHz and 1.8 GHz. At 900 MHz, the rectifier achieves 48.8% peak PCE, while at 1.8 GHz, it demonstrates a peak PCE of 46.4%.

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Abbreviations

CCDD	Cross-coupled differential drive
PCE	Power conversion efficiency
PDR	Power dynamic range
CMOS	Complimentary metal oxide semiconductor
RF	Radio frequency
DC	Direct current
V_{TH}	Threshold voltage
V_{out}	Rectifier output voltage
V_{GS}	Gate-to-source voltage
V_{sb}	Source-to-body voltage
V_{DC}	External voltage source of comparator
Vref	Reference voltage
Irev	Reverse leakage current
Pin	Input power in dBm

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