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Hybrid Inverter-Based Fully Differential Operational Transconductance Amplifiers

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Abstract: Inverter-based Operational Transconductance Amplifiers (OTAs) are versatile and friendly scalable analog circuit blocks. Especially for the new CMOS technological nodes, several recent applications have been extensively using them, ranging from Analog Front End (AFE) to analog-to-digital converters (ADC). This work tracks down the current advances in inverter-based OTAs design, comparing their basic fully differential structures, such as Nauta (N), Barthelemy (B), Vieru (V) and Mafredini (M) ones, and, in addition, mixing them up to propose new fully differential single-ended and two-stage hybrid versions. The new herein-proposed fully differential hybrid OTAs are the composition of Barthelemy/Nauta (B/N), Barthelemy/Manfredini (B/M), Nauta/Vieru (N/V), and Manfredini/Vieru (M/V) OTAs. All OTAs were designed using the same Global Foundries 180 nm open-source PDK and their performances are compared for post-layout simulations.

Keywords: inverter-based amplifiers; operational transconductance amplifiers; open-source PDK

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1. Introduction

The simple and well-known static inverter is the basis and starting design point of the several common CMOS digital logic gates [1]. Despite its intrinsic simplicity and its wide usage in the digital domain, it is much more versatile than it looks and can be used in many analog applications, ranging from high-speed signal processing [2,3] under typical supply voltages to ultra-low voltage domain as seen within the analog–digital converter designs [4–7], and biomedical instrumentation amplifiers [8]. The performance of such inverter-based dependent systems not only relies on their own topologies but is also dependent on the underlying Operational Transconductance Amplifiers (OTA) schematics [9–16]. If such a system's basic analog blocks can be improved in any aspect, the whole system can benefit from it. Unfortunately, not all the performance characteristics can be improved simultaneously, as there are always trade-offs that must be considered and decided during the OTA design. In addition to that, a fair comparison between inverter-based OTA designs using the same CMOS technology is no longer easily found in the literature.

In this context, for the first time, this work presents a review of the existing basic single-stage inverter-based OTAs found in the current literature and compares their strengths and weaknesses for all circuits designed at the same PDK. The inverter-based topologies used here are the Nauta (N), Barthelemy (B), Vieru (V), and Mafredini (M) OTAs. Their main difference is the common-mode rejection techniques they employ, at which, in the end, there are trade-offs between their power consumption, area usage, complexity, and output voltage excursion. Furthermore, those can be mixed to make hybrid OTA topologies, which are proposed and presented here. The proposed hybrid OTA topologies are Barthelemy/Nauta (B/N), Barthelemy/Manfredini (B/M), Barthelemy/Manfredini (B/M), Manfredini/Vieru

(M/V) OTAs. They are also designed with the same technology and compared with the basic single-stage ones.

The paper is organized as follows. Within Section 2, the paper presents a CMOS inverter cell, its biasing circuit, and its optimal operation point for maximum linearity. Later, in Section 3, the four basic inverter-based OTA topologies [2,3,10,11] are discussed. In Section 4, five combinations of the previous OTA topologies, and how active frequency compensation [17] can be used in the design of two-stage OTAs while improving common-mode rejection are presented. Section 5 shows a fair comparison of each topology, using designs made with the same inverter cells, the same gain-bandwidth performance, and simulated with the same operating conditions. Finally, Section 6 concludes this work.

2. CMOS Inverter

The CMOS inverter is the key building block used to create the OTAs proposed in this work. Consequently, the inverter-based OTAs performance characteristics, such as transconductance, gain-bandwidth, power consumption, common-mode rejection ratio (CMRR), and power-supply rejection ratio (PSRR), depends on the quality of the CMOS inverter design. Its properties, such as large and small-signal parameters, process variability, temperature, and supply voltage dependence, are thoroughly explained in [18,19].

Figure 1a illustrates a custom CMOS inverter circuit diagram, which differs from the conventional CMOS inverter logic gate as it explicitly shows a dedicated driver transistor to control its supply voltage, and its PMOS transistor's bulk terminal availability for body-biasing. Each transistor in this cell is, in fact, a rectangular transistor array [20], made of a m by n matrix of single transistors, as shown in Figure 1b. This inverter cell schematic, in particular, includes a third transistor and has two supplies: a higher supply voltage V_{DD} and a regulated supply voltage V_{REG}. Transistor M_A is made of thick oxide devices, and its function is to control V_{REG} by properly biasing its gate voltage, which is connected to node GP. Transistors M_B and M_C compose the main CMOS inverter structure, and are made of thin oxide devices. Another custom modification is that the PMOS device bulk terminal is available for body-biasing, and it is connected to node BP, instead of V_{REG}. Additionally, an inverter cell, as shown in Figure 1c, is made of multiple cells in parallel with shared power supplies, input and output terminals, so its total small-signal transconductance G_{mX} is a X-folded the single inverter cell transconductance G_{m0}.

A single inverter cell's transconductance changes following Process, Supply Voltage, and Temperature (PVT) variations. For this reason, an OTA made of inverter cells must be biased by an external reference circuit, otherwise, the inverter-based OTA would suffer from large PVT variations jeopardizing the OTA functioning. An OTA's transconductance can be tuned by varying its supply voltage [2] or using body-biasing [19,21–23]. This work proposes a combination of both methods, using two different circuits.

The first circuit, shown in Figure 2, controls the OTA's regulated supply voltage V_{REG}; however, instead of setting V_{REG} proportionally to a reference voltage, it is a function of a reference biasing current I_{BIAS}. This circuit's main goal is to make the replica inverter cell quiescent current I_Q, also known as its short-circuit current, to follow the I_{BIAS}. The circuit mirrors those currents, compares them, and controls the voltage at node GP, closing the negative feedback loop. This circuit considers that there is a supply voltage V_{DD} higher than the desired V_{REG}. Most commercial fabrication processes have thick and thin oxide devices available for different purposes in the same chip, rated for different maximum voltage drops. The proposed circuit has an additional circuit that prevents transistor M_{4C}'s drain-to-source voltage reaching voltages higher than V_{REG}, using the protection think oxide transistor M_{4B}. To avoid connecting its gate terminal directly to V_{REG}, and possibly incurring in antenna design rule violations, it is connected to node HI, from the tie-high circuit.

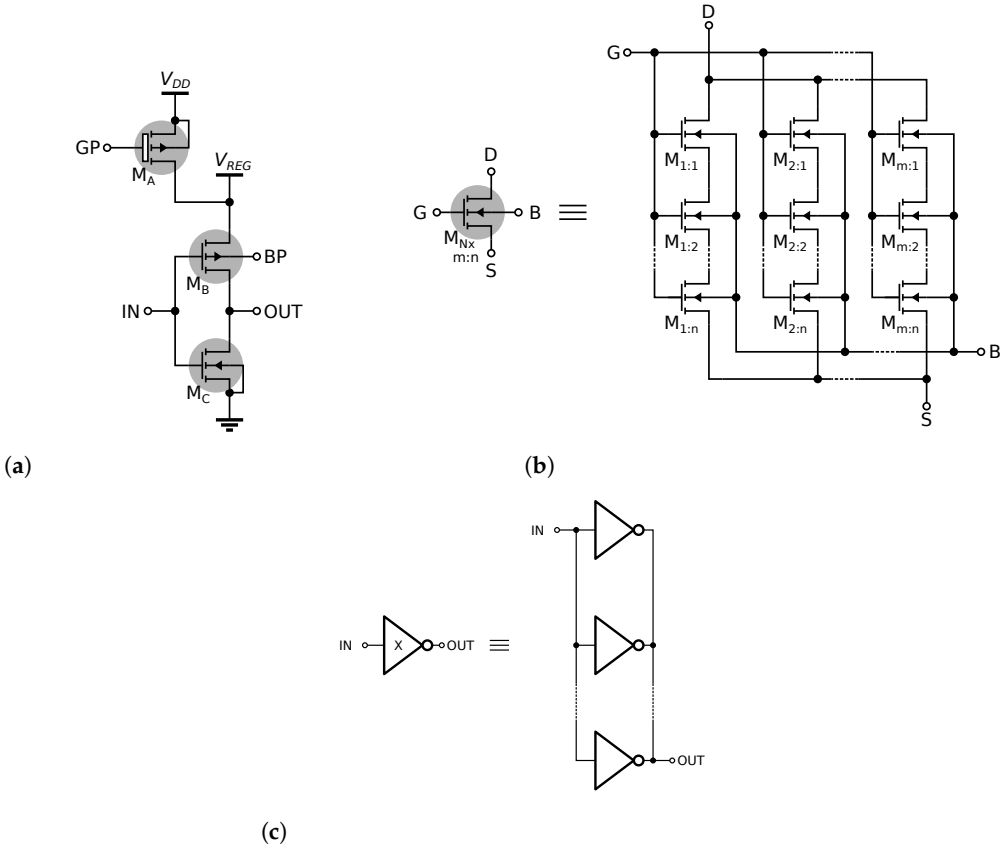


Figure 1. (**a**) Single inverter schematic, (**b**) transistor rectangular array, and (**c**) parallel inverters.

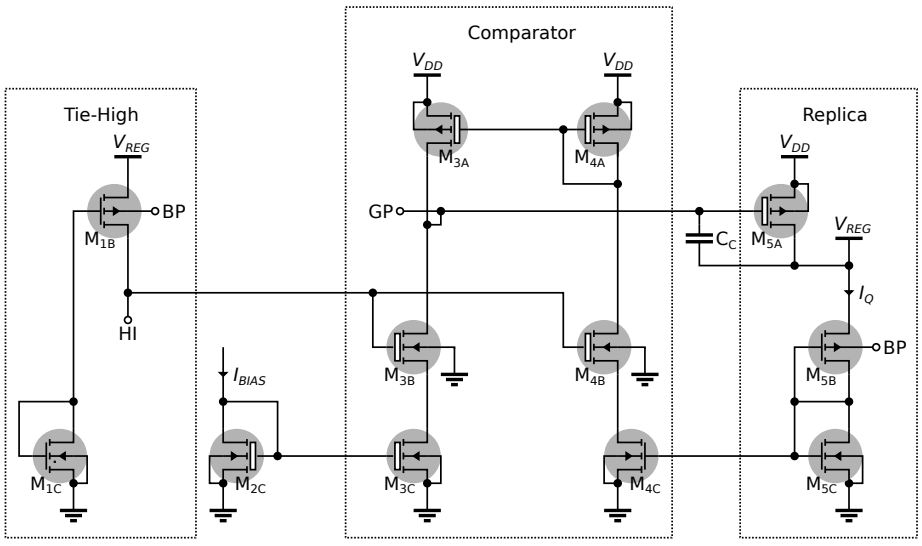


Figure 2. Quiescent current biasing circuit.

The second circuit is the quiescent voltage (also known as inverter trip-point or threshold voltage) biasing circuit, shown in Figure 3. Its final goal is to set a fully differential inverter-based OTA's output common-mode voltage to half supply, regardless of process variations [19]. The REF node voltage is equal to half the regulated supply voltage V_{REF}. Other body-bias circuits use resistor voltage dividers to achieve the same reference voltage [10,21,24]; however, we are using diode-connected PMOS devices. Similar to the previous circuit, to avoid antenna design rule violations, transistor M_{2E} gate terminal is connected to the tie-lo output LO node, instead of being connected directly to the ground.

Another difference from this circuit to the one proposed in [19] is, since it has access to voltages higher than V_{REG}, the PMOS devices can also be reverse-body-biased, which increases the body-biasing range. This happens because the voltage follower, made of the common-drain buffer stage, also works as a voltage level shifter.

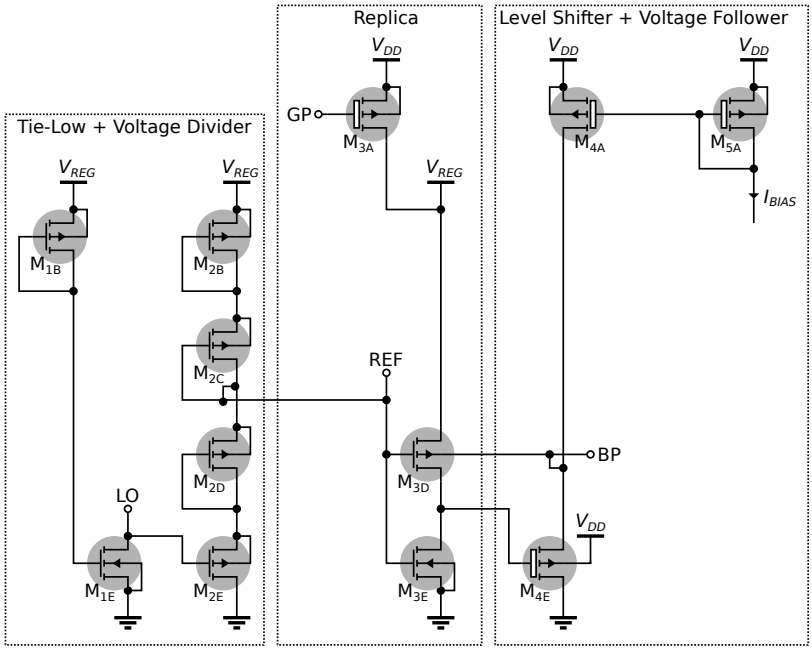
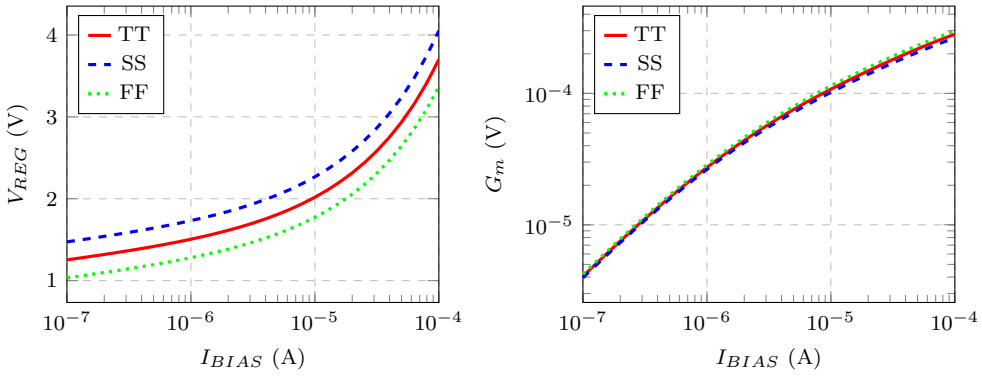


Figure 3. Quiescent voltage biasing circuit.

As an example of the biasing circuit operation, Figure 4a shows the resulting regulated supply voltage V_{REG} as a function of the reference biasing current I_{BIAS} for process corners TT, SS, and FF, for a constant supply voltage V_{DD} at 5 V, and at room temperature. As expected, for the same I_{BIAS}, different corners have different results. Nevertheless, as can be seen in Figure 4b, an inverter cell biased this way, has almost identical transconductance curves as function of I_{BIAS}, independently of the process corner.



(**a**) (**b**)

Figure 4. (**a**) $V_{REG} \times I_{BIAS}$, and (**b**) $G_m \times I_{BIAS}$.

The inverter quiescent voltage is a function of the supply voltage, the transistor model parameters, such as threshold voltage and charge mobility [19], and transistor's dimensions such as width (W) and length (L). For a typical process and operation conditions it should be designed to be close to the half voltage supply but without the expense of the inverter transconductance linearity, so the PMOS and NMOS contributions to the

total transconductance would be as equal and symmetrical as possible. Since the PMOS device transconductance is relatively lower than the NMOS' ones due to the inferior charge mobility of the holes compared to electrons, the PMOS transistor aspect ratio S = W/L must be larger. For this reason, all single inverter cells used in this work have PMOS transistors with aspect ratios about 3.33 times larger than their NMOS counterparts. Additionally, the PMOS devices are basically made of parallel transistor arrays while the NMOS are made of series transistor arrays, so their active areas are also similar. The inverter transistor dimensions is summarized in Table 1.

Table 1. Inverter cell transistor array dimensions.

Name	Type	Array ($m \times n$)	W/L (µm/µm)
M_A	thick P	2:1	1.8 / 0.6
M_B	thin P	2:1	1.5 / 0.6
M_C	thin N	1:2	1.8 / 0.6

Moreover, every CMOS inverter is sized to operate in the optimal operation condition for transconductance linearity [22]. This behavior is depicted in Figure 5a, which shows the inverter cell output current for a varying input voltage around the quiescent voltage, under a constant output voltage. As can be seen, the output current I_{OUT} has a different curvature for different supply voltages V_{REG}, which directly affects the inverter transconductance, as shown in Figure 5b. This effect is easier to observe by normalizing those the same curves as illustrated in Figure 5c,d, respectively.

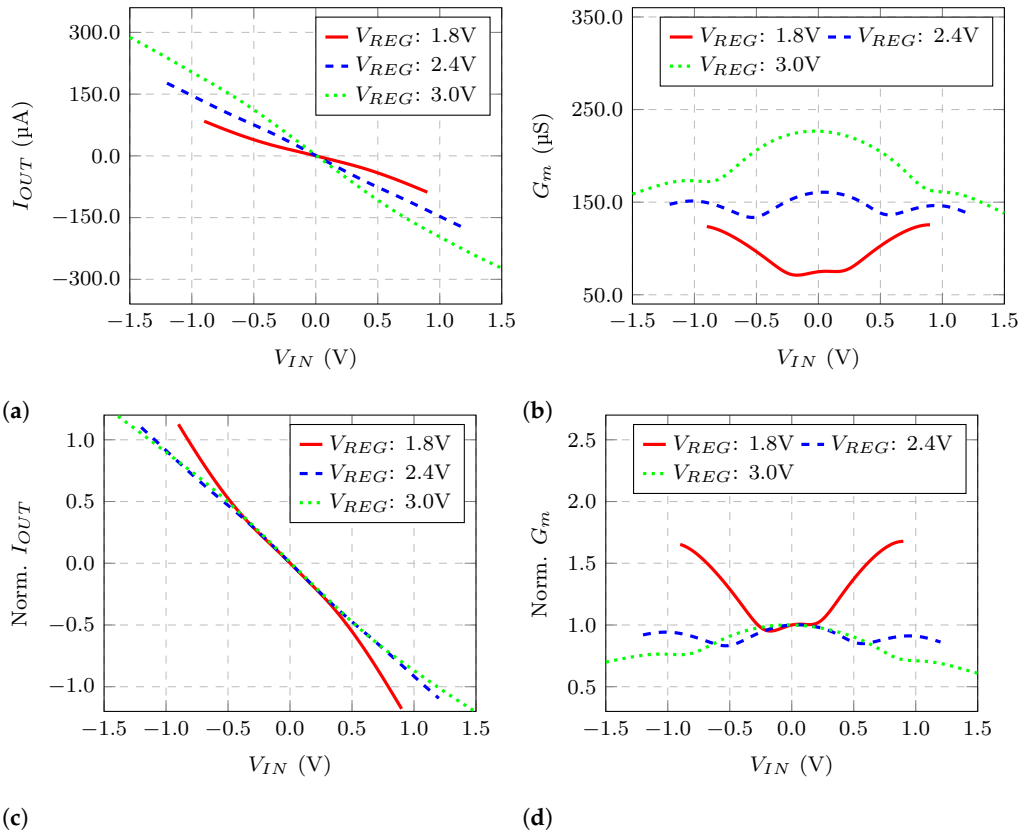


Figure 5. (**a**) Output current × input voltage, (**b**) transconductance × input voltage, (**c**) normalized output current × input voltage, and (**d**) normalized transconductance × input voltage.

3. Basic Inverter-Based OTAs

The first inverter-based OTA was proposed by Nauta in 1989 [2,9]. Figure 6 shows its schematic. It is made of six inverters, has only four nodes, and is completely symmetrical.

It is composed of two parts: the transconductor itself (inverters A) which is responsible for the OTA transconductance, and the common-mode rejection circuit, made of inverters B and C. This topology is essentially an attenuated positive feedback that works differently for differential and common-mode signals. Inverters C are cross-coupled and result in positive feedback for differential signals attenuated by inverters B, which are connected as loads. For common-mode signals, both inverters B and C are seen as loads by inverters A.

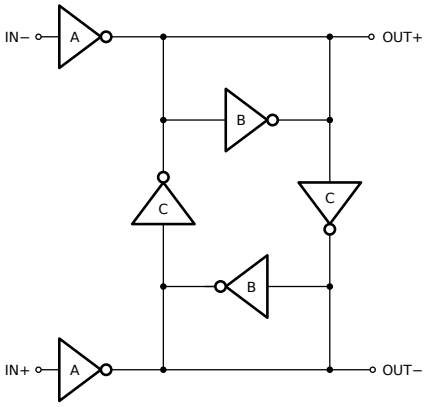


Figure 6. Nauta (N) OTA circuit diagram [2].

The small-signal low-frequency (DC) differential A_{VDF} and common-mode A_{VCM} voltage gains are functions of the inverters transconductances G_{mX} and output conductances G_{oX}

$$A_{VDF} = \frac{G_{mA}}{G_{oA} + G_{oB} + G_{oC} + G_{mB} - G_{mC}} \tag{1}$$

$$A_{VCM} = -\frac{G_{mA}}{G_{oA} + G_{oB} + G_{oC} + G_{mB} + G_{mC}} \tag{2}$$

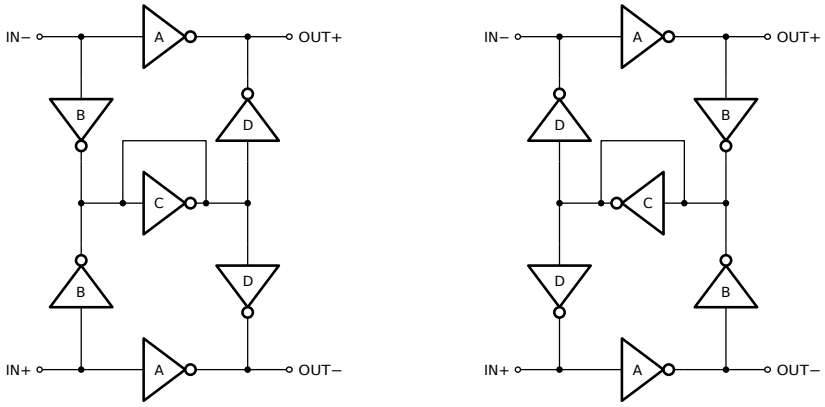
Considering that the equivalent transconductance (output conductance) $G_{mX(oX)}$ of parallel inverter cells is proportional to the transconductance (output conductance) of a single inverter cell $G_{m0(o0)}$ and the inverter cell voltage small-signal voltage gain is equal to A_V, then for the special case where the inverter cell multipliers $A = 2B = 2C$,

$$A_{VDF} = \frac{G_{mA}}{2G_{oA}} = \frac{A_V}{2} \tag{3}$$

$$A_{VCM} = -\frac{G_{mA}}{2G_{oA} + G_{mA}} = -\frac{A_V}{2 + A_V} \approx -1 \tag{4}$$

Ideally, G_{mC} should be designed to be slightly larger than G_{mB}, so that we would have $G_{mC} - G_{mB} = G_{oA} + G_{oB} + G_{oC}$ and infinite differential voltage gain. To achieve this, inverters B and C could be designed with different sizes or biased independently [2,21]. However, as seen in Figure 5b, the inverter transconductance is not linear and voltage gain would be only infinite for a point in the curve. Even if the inverter transconductances were perfectly linear, any variation due to PVT or local mismatch would decrease voltage gain or lead to hysteresis. For this reason, voltage gain improvement by this positive feedback technique is limited by a few dB, even using automatic biasing circuits [24].

As an alternative to the Nauta OTA, Figure 7a shows another inverter-based OTA based on the CM input feedforward rejection technique [3]. This OTA topology main advantage is its output voltage headroom, as the Nauta topology greatly reduces it, even considering that the inverter cell output voltage headroom is almost rail-to-rail.



(**a**) (**b**)

Figure 7. (**a**) Barthelemy (B) OTA diagram [3], and (**b**) Vieru (V) OTA circuit diagram [5].

In this circuit, the common-mode input signal is extracted from the differential signals using inverters B and C. Then, this signal is fed forward to each output with inverted polarity, thus canceling the common-mode component of which is also amplified by inverter A, leaving the remaining input output differential signal. However, this common-mode cancelation is not perfect, as it is limited by the finite inverter voltage gain.

$$A_{VDF} = \frac{G_{mA}}{G_{oA} + G_{oD}} \tag{5}$$

$$A_{VCM} = -\left(G_{mA} - \frac{2G_{mB}G_{mD}}{2G_{oB} + G_{oC} + G_{mC}}\right)\frac{1}{G_{oA} + G_{oD}} \tag{6}$$

Applying the same reasoning was used for the Nauta OTA topology, for the special case, where $(D/A) = (B/2C) = 1$

$$A_{VDF} = \frac{G_{mA}}{2G_{oA}} = \frac{A_V}{2} \tag{7}$$

$$A_{VCM} = -\left(G_{mA} - \frac{G_{mA}G_{mB}}{G_{oB} + G_{mB}}\right)\frac{1}{2G_{oA}} = -\frac{A_V}{2 + 2A_V} \approx -1 \tag{8}$$

In this case, the common-mode voltage gain in the intermediate node is also unity. Other inverter multiplier ratios can be used but this one was selected so that it can have the same differential and common-mode voltage gain as the (N) OTA. Additionally, this OTA could be designed with $A \gg B$ for maximum power efficiency as it does not affect either A_{VDF} and A_{VCM}. However, this could lead to severe voltage offset problems due to transistor local mismatch.

A variant of Barthelemy OTA is the Vieru OTA as depicted in Figure 7b. It is composed of the same number of cells and nodes, but the common-mode signal path direction is reverted so that the CM signal is fed back to the input. This topology is not advantageous alone, once it depends on the OTA input load. However, it can be useful as a cascaded two-stage OTAs [10].

Another approach is to adopt a CM feedback technique which can be used in a standalone single-stage amplifier, as proposed in Mafredini [11] by adding another node so that the output CM signal is fed back to the output nodes without going through the input nodes as done in the Vieru OTA topology. Figure 8 shows the Manfredini OTA. As in the Nauta OTA the output signal is fed back to itself but without positive feedback. As in the Vieru OTA, the output common signal is extracted from the differential output signals by inverters B and C. Inverters D and E invert the common-mode signal polarity, and inverters

F feed the common-mode signal back to the output canceling it. For differential signals, the circuit is ideally transparent. This common-mode technique is limited by the inverter cell low-frequency voltage gain, as shown in the small-signal analysis

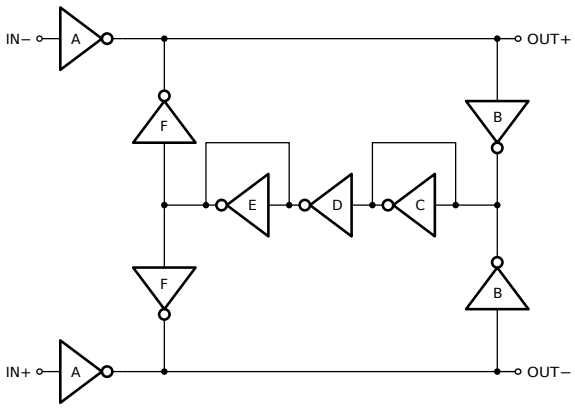


Figure 8. Mafredini (M) OTA circuit diagram [11].

$$A_{VDF} = \frac{G_{mA}}{G_{oA} + G_{oF}} \tag{9}$$

$$A_{VCM} = -\frac{G_{mA}}{G_{oA} + G_{oF} + G_{mF}\left(\frac{2G_{mB}}{2G_{oB} + G_{oC} + G_{mC}}\right)\left(\frac{G_{mD}}{G_{oD} + G_{oE} + G_{mE}}\right)} \tag{10}$$

For the special case where $(F/A) = (B/2C) = (E/D) = 1$,

$$A_{VDF} = \frac{G_{mA}}{2G_{oA}} = \frac{A_V}{2} \tag{11}$$

$$A_{VCM} = -\frac{G_{mA}}{2G_{oA} + G_{mA}\left(\frac{G_{mB}}{2G_{oB} + G_{mB}}\right)\left(\frac{G_{mD}}{2G_{oD} + G_{mD}}\right)} = -\frac{A_V}{2 + A_V\left(\frac{A_V}{2 + A_V}\right)^2} \approx -1 \tag{12}$$

the small-signal differential and common-mode voltage gains are similar to the previous topologies, once the common-mode path voltage gain is unity. Other inverter multipliers could be used to improve either the common-mode rejection or power efficiency, but this would result in the detriment of other OTA performance.

4. Proposed Hybrid Inverter-Based Amplifier Topologies

The previously presented OTA topologies can be merged to create hybrid versions. The OTA shown in Figure 9 combines the common-mode feedforward and attenuated positive feedback techniques from Barthelemy and Nauta OTAs. The Barthelemy/Nauta (B/N) small-signal low-frequency voltage gains are

$$A_{VDF} = \frac{G_{mA}}{G_{oA} + G_{oD} + G_{oE} + G_{oF}} \tag{13}$$

$$A_{VCM} = -\left(G_{mA} - \frac{2G_{mB}G_{mD}}{2G_{oB} + G_{oC} + G_{mC}}\right)\frac{1}{G_{oA} + G_{oD} + G_{oE} + G_{oF}} \tag{14}$$

For the special case, where $(D/A) = (B/2C) = (F/E)$ and $A = 2F$

$$A_{VDF} = \frac{G_{mA}}{3G_{oA}} = \frac{A_V}{3} \tag{15}$$

$$A_{VCM} = -\left(G_{mA} - \frac{G_{mA}G_{mB}}{G_{oB} + G_{mB}}\right)\frac{1}{3G_{oA} + G_{mA}} = -\left(\frac{1}{1 + A_V}\right)\frac{A_V}{3 + A_V} \approx -\frac{1}{A_V} \tag{16}$$

As result, in this proposed B/N OTA, the common-mode voltage signal is further attenuated by a factor proportional to the inverter voltage gain. This is great for applications that need high common-mode rejection such as instrumental and biomedical signal amplifiers. However, B/N OTA suffers from the same drawback seen in the Nauta OTA; the output voltage excursion reduction.

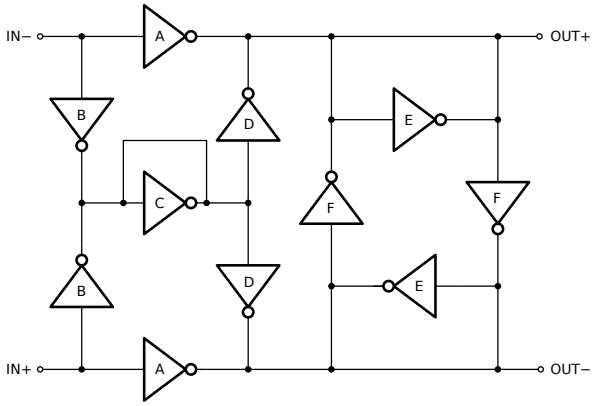


Figure 9. Barthelemy/Nauta (B/N) hybrid OTA circuit diagram.

A solution to keep the high common-mode rejection while having a reasonable output voltage signal headroom is to combine the Barthelemy and Manfredini (B/M) OTA topologies. Figure 10 shows the second hybrid topology, which uses both CM input feedforward and output feedback techniques, by sharing the CM signal path to save area and power. Then, the B/M small-signal low-frequency voltage gains are

$$A_{VDF} = \frac{G_{mA}}{G_{oA} + G_{oD}} \tag{17}$$

$$A_{VCM} = -\frac{\left(G_{mA} - \dfrac{2G_{mB}G_{mD}}{2G_{oB} + G_{oC} + G_{mC}}\right)}{G_{oA} + G_{oD} + G_{mD}\left(\dfrac{2G_{mE}}{2G_{oE} + G_{oF} + G_{mF}}\right)\left(\dfrac{G_{mG}}{G_{oG} + G_{oC} + G_{mC}}\right)} \tag{18}$$

For the special case where $(F/A) = (B/2C) = (E/D) = 1$

$$A_{VDF} = \frac{G_{mA}}{2G_{oA}} = \frac{A_V}{2} \tag{19}$$

$$A_{VCM} = -\frac{G_{mA}\left(\dfrac{G_{mB}}{2G_{oB} + G_{mB}}\right)}{2G_{oA} + G_{mA}\left(\dfrac{G_{mE}}{2G_{oE} + G_{mE}}\right)\left(\dfrac{G_{mB}}{2G_{oB} + G_{mB}}\right)} = -\frac{\left(\dfrac{A_V}{2 + A_V}\right)}{2 + A_V\left(\dfrac{A_V}{2 + A_V}\right)^2} \approx -\frac{1}{A_V} \tag{20}$$

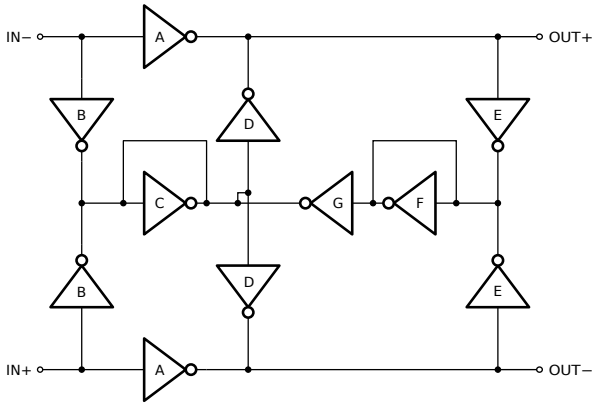


Figure 10. Barthelemy/Manfredini (B/M) hybrid OTA circuit diagram.

As seen in B/N, in B/M OTA the common-mode signal is attenuated by approximately the inverter voltage gain. This topology has the same number of intermediate nodes as the Manfredini OTA; however, it needs extra inverters, increasing this way its power consumption and the silicon area.

The basic and hybrid single-stage inverter-based OTAs seen so far are inherently stable once they do not have intermediate nodes in their differential signal path and there is no voltage gain in their common-mode signal path. Multi-stage amplifiers, on the other hand, need a frequency compensation circuit, if they are used within negative feedback networks. One of the simplest frequency compensation circuits is the Miller compensation capacitor, which implements the pole-splitting technique, which is normally followed by a zero-cancelation technique, mostly implemented with resistors. Another alternative is to use the so-called Nested Transconductance-Capacitance Compensation technique (NGCC) [17], which is an approach that replaces the zero-canceling resistor with an active transconductance, and can be adapted to fully differential two-stage OTAs, as shown in Figure 11.

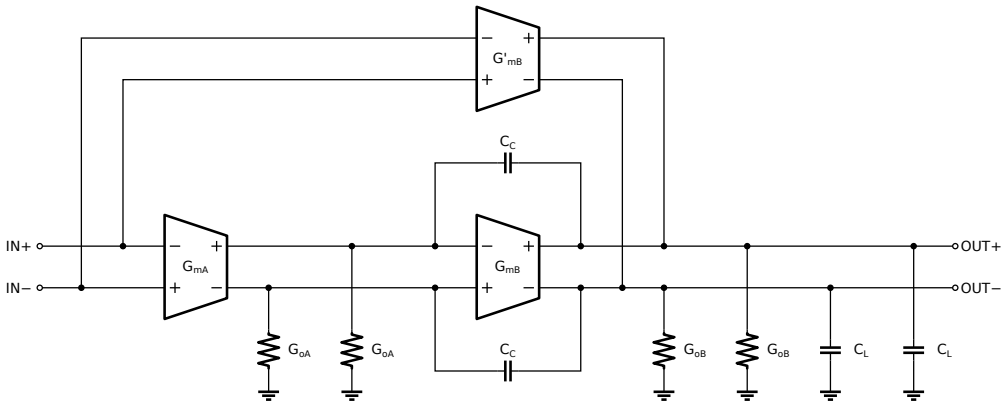


Figure 11. Two-stage amplifier with Gm-C feedforward frequency compensation [17].

Equation (21) shows the open-loop transfer function for the number of stages $n = 2$.

$$H(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} \approx -\frac{g_{mA}}{g_{oA}}\frac{g_{mB}}{g_{oB}}\frac{1}{\left(1+\frac{g_{mA}}{g_{oA}}\frac{g_{mB}}{g_{oB}}\frac{sC_{mA}}{g_{mA}}\right)\left(1+\frac{sC_{OUT}}{g_{mB}}\right)} \tag{21}$$

where g_{mA} and g_{mB} are the transconductance, g_{oA} and g_{oB} are the equivalent conductance of the first and second nodes across the Miller capacitor C_c, respectively.

Figure 12 depicts a two-stage amplifier [6] comprised of two distinct Nauta stages with different strengths, and a Gm-C feedforward compensation path as described by Equation (21) and in the Figure 11. Given that all the design requirements to keep the

circuit stable are considered according to Equation (21), then the Nauta/Nauta (N/N) low-frequency small-signal gains are

$$A_{VDF} = \frac{\left(\frac{G_{mA}}{G_{oA} + G_{oB} + G_{oC} + G_{mB} - G_{mC}}\right) G_{mD} + G_{mG}}{G_{oD} + G_{oE} + G_{oF} + G_{oG} + G_{mE} - G_{mF}} \tag{22}$$

$$A_{VCM} = \frac{\left(\frac{G_{mA}}{G_{oA} + G_{oB} + G_{oC} + G_{mB} + G_{mC}}\right) G_{mD} - G_{mG}}{G_{oD} + G_{oE} + G_{oF} + G_{oG} + G_{mE} + G_{mF}} \tag{23}$$

and, for the special case where $A = 2B = 2C$, $D = 2E = 2F$, and $2A = D = G$

$$A_{VDF} = \left(\frac{G_{mA}}{2G_{oA}} + 1\right)\left(\frac{G_{mA}}{3G_{oA}}\right) \approx \frac{(A_V)^2}{6} \tag{24}$$

$$A_{VCM} = \left(\frac{G_{mA}}{2G_{oA} + G_{mA}} - 1\right)\left(\frac{G_{mA}}{3G_{oA} + G_{mA}}\right) = \left(\frac{2}{2 - A_V}\right)\left(\frac{A_V}{3 + A_V}\right) \approx -\frac{2}{A_V} \tag{25}$$

therefore, the differential voltage gain is proportional to two cascaded amplifiers, and the common-mode voltage gain is further attenuated as an effect of the feedforward path used for frequency compensation. However, the N/N OTA also suffers from the same degraded output voltage excursion of standalone N OTA.

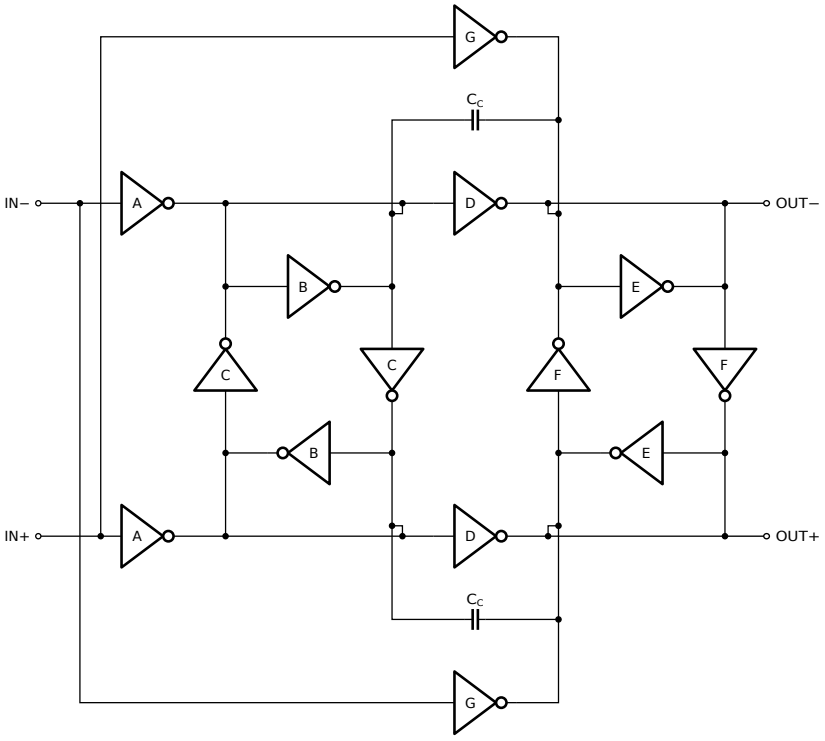


Figure 12. Two-stage Nauta/Nauta (N/N) OTA circuit diagram.

Variants of N/N are also herein proposed considering the current advances in inverter-based OTA designs. Therefore, The N/N second stage can be replaced by the Vieru OTA from Figure 7b, which implements output common-mode feedback to the inner nodes, as shown in Figure 13. Considering the circuit is stable, the Nauta/Vieru (N/V) OTA have

$$A_{VDF} = \frac{\left(\frac{G_{mA}}{G_{oA}+G_{oB}+G_{oC}+G_{mB}-G_{mC}+G_{oG}}\right)G_{mD}+G_{mH}}{G_{oD}+G_{oH}} \tag{26}$$

$$A_{VCM} = \frac{\left(\frac{G_{mA}}{2G_{oA}+G_{mA}}-1\right)\left(\frac{G_{mA}}{G_{oA}}\right)}{\left[1+\left(\frac{G_{mA}}{2G_{oA}+G_{mA}}\right)^2\left(\frac{G_{mA}}{G_{oA}}\right)\right]} \tag{27}$$

as low-frequency gains for the differential and common-mode signals, respectively.

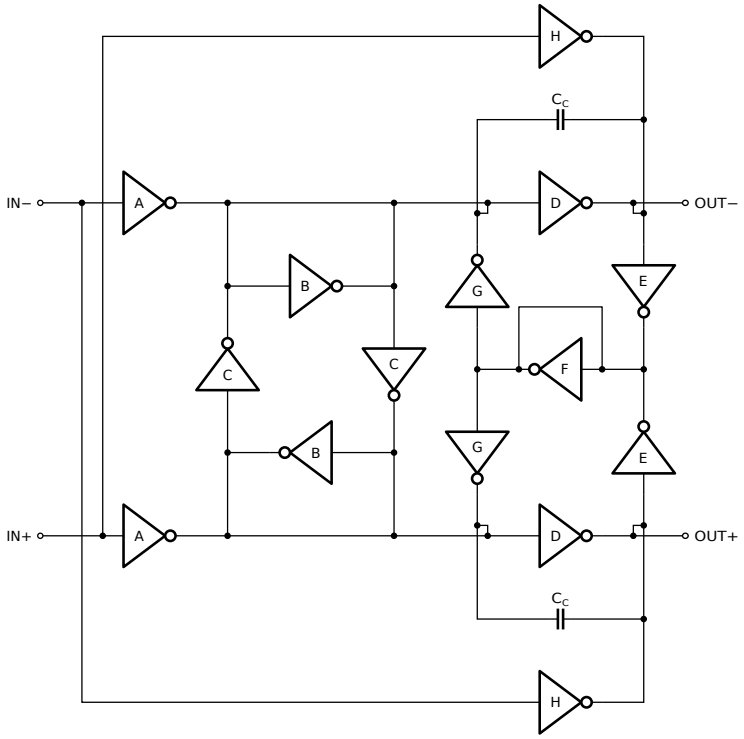


Figure 13. Nauta/Vieru (N/V) hybrid OTA circuit diagram.

For $A = 2B = 2C = G$, $2E = F$, and $2A = D = H$

$$A_{VDF} = \left(\frac{G_{mA}}{3G_{oA}}+1\right)\left(\frac{G_{mA}}{2G_{oA}}\right) \approx \frac{(A_V)^2}{6} \tag{28}$$

$$A_{VCM} = \frac{\left(\frac{A_V}{2+A_V}-1\right)A_V}{\left[1+\left(\frac{A_V}{2+A_V}\right)^2 A_V\right]} \approx -\frac{2}{A_V} \tag{29}$$

Another possibility is to further replace the first stage with a Manfredini stage of the Figure 8, implement self-output common-mode feedback, and share the same path, as shown in Figure 14. Making the same small-signal analysis and applying $A = E$, $2B = C$, $D = 2G = H$ and $2A = F = I$, the Manfredini/Vieru (M/V) hybrid OTA has

$$A_{VDF} = \left(\frac{G_{mA}}{2G_{oA}}+1\right)\left(\frac{G_{mA}}{2G_{oA}}\right) \approx \frac{(A_V)^2}{4} \tag{30}$$

$$A_{VCM} = \frac{\left[\dfrac{A_V}{2 + A_V\left(\dfrac{A_V}{2+A_V}\right)^2}\right] - 1}{1 + \left[\dfrac{A_V}{2 + A_V\left(\dfrac{A_V}{2+A_V}\right)^2}\right]^2 A_V} \approx -\frac{2}{A_V} \tag{31}$$

as low-frequency gains for the differential and common-mode signals, respectively.

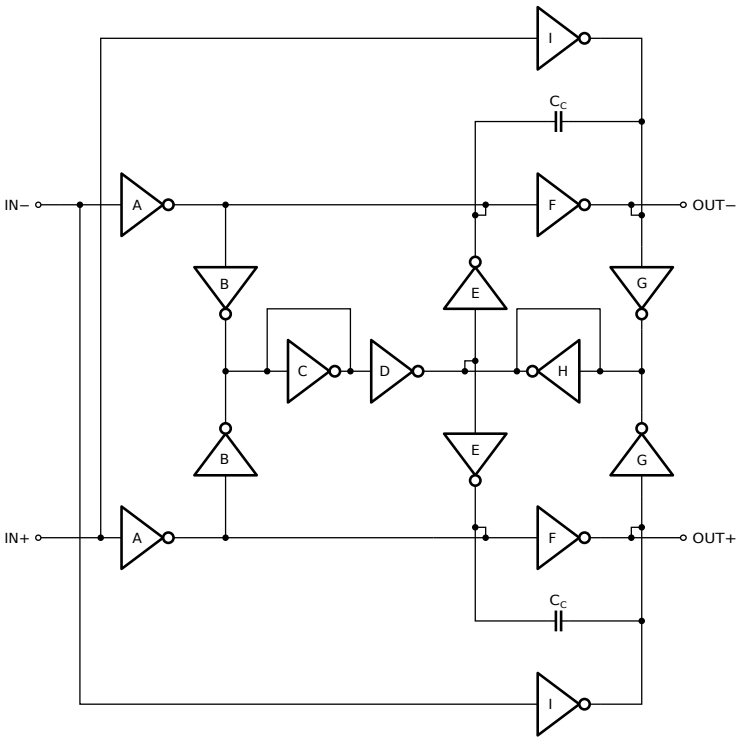


Figure 14. Manfredini/Vieru (M/V) hybrid OTA circuit diagram.

5. Simulation Results

All OTAs have been designed and simulated using Global Foundries 180 nm open-source PDK [25] and open-source tools (ngspice simulator [26] and Magic VLSI layout tool [27]), and their spice netlists and results are available at [28]. All inverter cells are identical, and the number of parallel cells in each OTA individual inverter and total area is defined as in Table 2. The OTA's layouts are shown in Figure 15.

Table 2. OTA inverter cell multipliers.

	A	B	C	D	E	F	G	H	I	Area (µm²)
N	4	2	2							1983.60
B	4	2	4	4						3013.20
M	4	2	4	2	2	4				3682.80
B/N	4	2	4	4	2	2				3906.00
B/M	4	2	4	4	2	4	4			4633.20
N/N	4	2	2	8	4	4	8			12,435.12
N/V	4	2	2	8	2	4	4	8		12,804.48
M/V	4	2	4	4	8	2	4	4	8	14,074.56

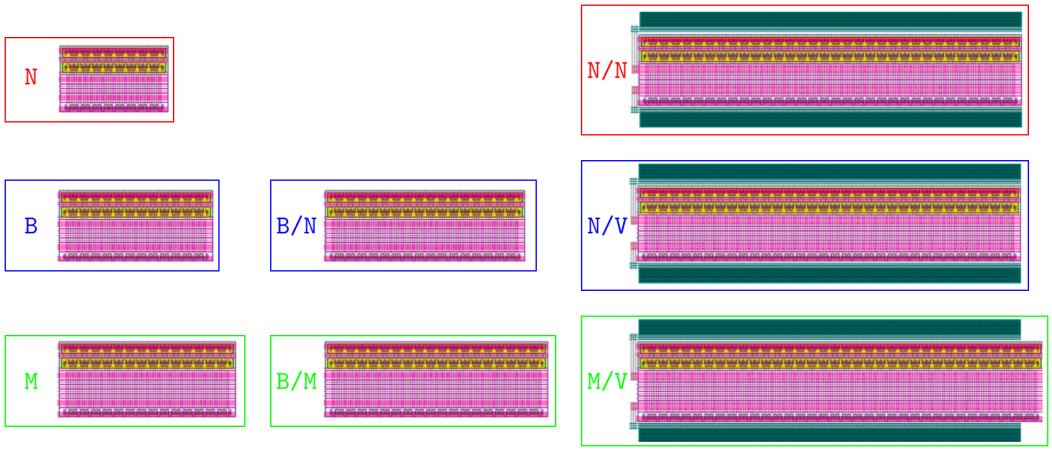


Figure 15. Amplifier layouts.

5.1. Performance under Nominal Conditions

The post-layout simulations have used as parameters typical process corner, 3.0 V as supply voltage at room temperature and a 10 pF as capacitive load (C_L).

As all single-stage OTAs have identical A inverters, they have almost identical differential AC output voltage gain (A_{VDF}), gain-bandwidth-product (GBW) and phase except for the B/N OTA, which has a slightly smaller low-frequency voltage gain, as shown in Figure 16. The main difference is the common-mode voltage gain (A_{VCM}) as the B OTA has a shorter CMR bandwidth and both single-stage hybrid OTAs B/N and B/M OTAs have much lower CM voltage gain.

The small-signal power-supply common-mode voltage gain (A_{VPS}) at the output is negative, which implies that any fluctuation at the voltage supply V_{DD} is attenuated at the output. This is a direct result of the biasing circuit operation, as it works as a low dropout regulator, so the regulated supply voltage V_{REG} is tolerant to V_{DD} variations. Additionally, the hybrid OTA topologies have a slightly higher power-supply rejection than the basic ones.

The DC simulation results, depicted in Figure 17, show the biggest difference between the basic Nauta, the Barthelemy, and Manfredini OTAs. As the N OTA has a lower output voltage swing, consequently, all hybrid OTAs which use this technique suffer from the same penalty. For this reason, the B/M hybrid OTA despite being larger and a bit more complex than the B/N hybrid OTA has a much larger output voltage swing while keeping a similar common-mode rejection.

Both Barthelemy and Manfredini OTAs have similar output voltage excursions however, they do not have rail-to-rail output, as it is limited by the transistor saturation region. This problem is solved using two-stage OTAs, as the first stage still contributes to voltage gain, even if the transistors connected to the output are operating in the low-gain linear region.

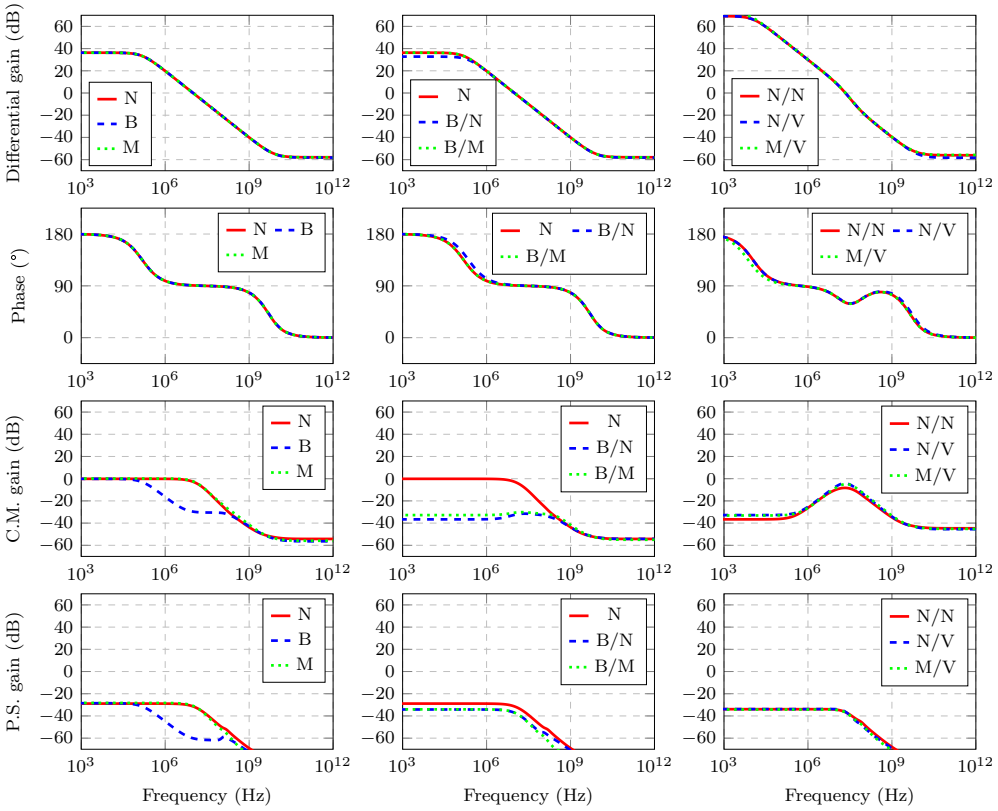


Figure 16. AC simulation results.

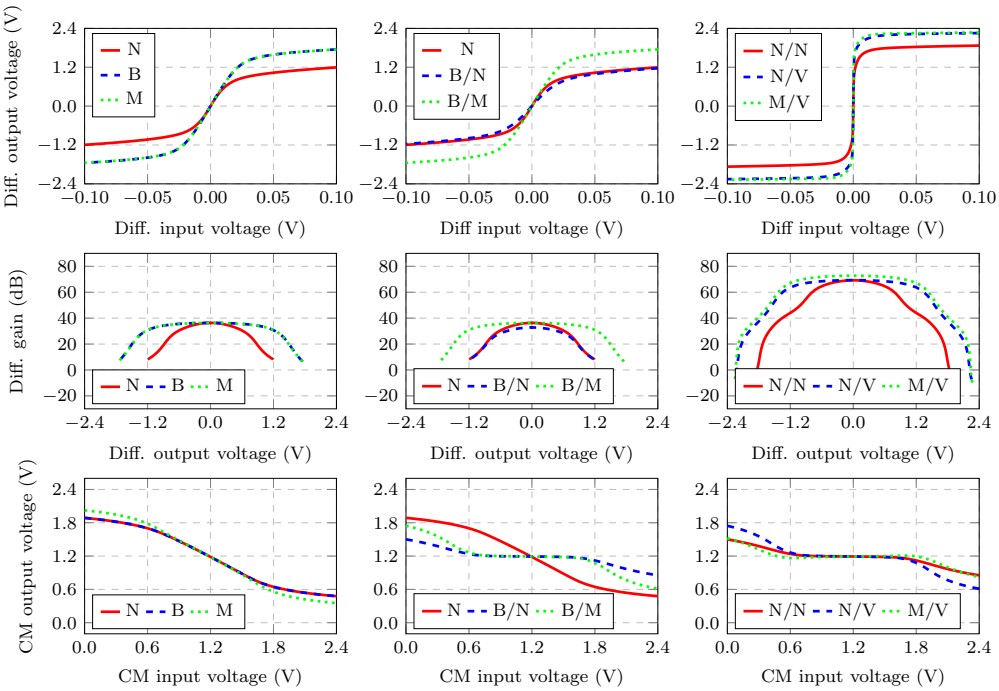


Figure 17. DC simulation results.

The two-stage OTAs have a much larger differential voltage gain and lower phase margin (PM), as expected. The feedforward frequency compensation technique also decreases common-mode voltage gain as a side-effect, so they have common-mode rejection results similar to the single-stage hybrid OTAs. Additionally, as the designs grow more complex

and use more total transistors, not only their area, but their total current consumption (I_{DD}) increases, so their power-efficiency Figure of Merit (FoM) decreases as well.

Figure 18 shows the noise simulation results. All OTAs have similar results, as they have the same number of inverter cells connected to their outputs, which results in the same voltage gain and transconductance. The two-stage OTAs also have similar results, as the first-stage output noise is dominant.

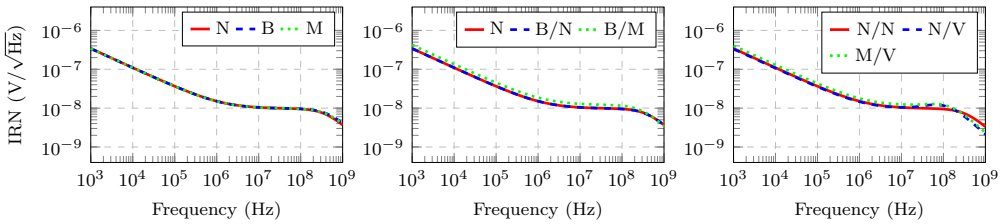


Figure 18. Noise simulation results.

5.2. Process Variations and Monte Carlo Analysis

All OTAs have been simulated under process variations. For PVT corner simulations, the process corners TT, FF, and SS at 27, 70 and 0 °C were chosen and their results are summarized in Table 3. As expected, since it is biased with an ideal current reference, current consumption variation is practically null, but the regulated supply voltage V_{REG} varies accordingly, as a direct result of the biasing circuit operation. Voltage gain and GBW is slightly lower for higher temperatures as the OTA inverter transconductance must be decreasing with temperature for this operation point.

Table 3. OTA PVT simulation results.

		A_{VDF} (dB)	A_{VCM} (dB)	A_{VPS} (dB)	GBW (MHz)	I_{DD} (mA)	P.M. (°)	FoM V^{-1}	Noise uV_{RMS}	V_{REG} (V)
TT	N	36.3	−0.1	−28.9	9.91	0.359	90.1	27.6	54.4	2.39
27 °C	B	36.3	−0.1	−28.5	9.98	0.538	90.1	18.6	54.4	2.39
	M	36.3	0.1	−28.3	9.94	0.628	90.1	15.8	54.4	2.39
	B/N	33.0	−36.6	−34.2	9.87	0.717	91.2	13.8	67.2	2.39
	B/M	36.3	−32.8	−34.1	9.92	0.806	90.1	12.3	54.4	2.39
	N/N	69.2	−36.6	−33.9	21.8	1.434	61.0	15.2	53.0	2.39
	N/V	69.3	−32.8	−33.9	21.9	1.434	61.3	15.3	64.3	2.39
	M/V	72.7	−33.1	−34.2	22.0	1.524	61.1	14.5	52.9	2.39
FF	N	35.0	−0.2	−26.3	9.65	0.363	90.9	26.6	55.3	2.13
70 °C	B	35.0	−0.2	−26.0	9.72	0.544	90.9	17.9	55.3	2.13
	M	35.0	0.2	−25.8	9.67	0.635	90.9	15.2	55.3	2.13
	B/N	31.5	−35.3	−31.7	9.61	0.726	91.4	13.2	68.3	2.13
	B/M	35.0	−31.4	−31.5	9.67	0.816	90.9	11.9	55.3	2.13
	N/N	66.5	−35.3	−31.4	22.4	1.451	58.9	15.5	53.6	2.13
	N/V	66.6	−31.4	−31.3	22.6	1.451	59.3	15.6	64.9	2.13
	M/V	70.0	−31.9	−31.7	22.7	1.542	58.9	14.7	53.5	2.13
SS	N	37.1	−0.1	−31.4	9.93	0.358	90.7	27.8	54.6	2.65
0 °C	B	37.1	−0.1	−31.1	10.0	0.537	90.7	18.6	54.6	2.65
	M	37.1	0.1	−30.9	9.95	0.626	90.7	15.9	54.6	2.65
	B/N	33.6	−37.4	−36.7	9.89	0.715	91.1	13.9	67.3	2.65
	B/M	37.1	−33.6	−36.6	9.95	0.805	90.7	12.4	54.5	2.65
	N/N	70.8	−37.4	−36.5	20.7	1.431	63.0	14.5	53.3	2.65
	N/V	70.8	−33.6	−36.4	20.8	1.431	63.4	14.6	64.6	2.65
	M/V	74.2	−34.0	−36.8	20.9	1.520	63.1	13.8	53.2	2.65

FoM = $100 \times \text{GBW} \times C_L / I_{DD}$.

Monte Carlo simulations have also been run for every OTA, considering a 5 V supply voltage, and room temperature, for local mismatch only (Mis.), global mismatch only (Proc.), and both local and global mismatch enabled (All). A total of 100 runs were simulated for

each case and its result summary is shown in Table 4. As expected, there is an input voltage offset (V_{OS}) resulting only from the local mismatch, and it is negligible for global mismatch, since the OTAs are symmetrical.

The output common-mode V_{OCM} is calculated as the deviation from the expected value, which should be calculated as $V_{OCM} = (V_{OUT+} + V_{OUT-})/2 = V_{REG}/2$. Again, for global mismatch, all OTAs have similar results, as they are made of the same inverter cells and biased with the same circuit. However, for local mismatch, the Barthelemy OTA is an outlier, as its standard deviation is about 3.5 times larger than the others. As an absolute value, 36.5 mV is relatively small, considering a typical V_{REG} at 2.4 V. However, for ultra-low-voltage supplies at the range of a few hundred mV, this variation could be unacceptable.

The differential voltage gain A_{VDF} variation is slightly larger for Nauta and its hybrid OTAs due to local mismatch, as there is positive feedback which can decrease or increase voltage gain. This effect can create outlier results, which can dramatically increase standard deviation, as seen in the Nauta/Nauta OTA.

Table 4. OTA Monte Carlo simulation results.

		A_{VDF} (dB)		V_{OS} (mV)		V_{OCM} (mV)	
		μ	σ	μ	σ	μ	σ
Mis.	N	36.4	1.1	0.1	2.8	3.0	10.8
	B	36.1	0.4	0.1	3.0	1.6	36.5
	M	36.3	0.2	0.5	2.8	3.2	11.9
	B/N	32.8	0.8	0.5	3.7	3.3	11.4
	B/M	36.3	0.2	0.4	2.9	1.7	12.1
	N/N	69.4	1.1	0.3	2.8	2.9	11.1
	N/V	69.2	0.7	0.6	3.7	3.3	11.3
	M/V	72.7	0.4	0.3	3.3	3.3	4.8
Proc.	N	36.3	0.2	0.0	0.0	3.5	1.7
	B	36.3	0.2	0.0	0.0	3.5	1.7
	M	36.3	0.2	0.0	0.0	3.5	1.7
	B/N	32.8	0.2	0.0	0.0	3.5	1.7
	B/M	36.3	0.2	0.0	0.0	3.5	1.7
	N/N	69.1	2.0	0.0	0.0	3.6	1.7
	N/V	69.5	2.2	0.0	0.0	3.6	1.7
	M/V	72.7	1.4	0.0	0.0	3.6	1.7
All	N	36.4	0.9	0.0	3.1	4.2	11.7
	B	35.9	0.6	0.2	3.1	1.4	36.9
	M	36.3	0.3	0.3	3.2	3.2	12.1
	B/N	32.8	0.8	0.2	3.9	3.8	12.5
	B/M	36.3	0.3	0.1	3.0	5.3	11.4
	N/N	72.0	16.1	0.2	3.1	4.9	12.0
	N/V	69.3	1.1	0.2	3.4	5.0	12.4
	M/V	72.6	0.5	0.1	3.1	3.9	5.2

6. Conclusions

Using 180 nm open-source PDK and open-source tools, this paper has described and compared in post-layout simulations, for the first time, the design of eight inverter-based OTAs: Nauta (N), Barthelemy (B), Mafredini (M), Barthelemy /Nauta (B/N), Barthelemy /Manfredini (B/M), Nauta/Nauta (N/N), Nauta/Vieru (N/V), and Manfredini /Vieru (M/V) OTAs. Based on simulation results without doubt the Nauta inverter-based OTA topology is the most power-efficient one, but its drawbacks are lower output swing. The other basic topologies, proposed by Barthelemy and Manfredini solve that by increasing the OTA complexity. Barthelemy and Manfredini OTAs have similar voltage excursions; however, the Barthelemy OTA output common voltage is intolerant to local mismatch, which should be a problem for lower supply voltages. Hybrid topologies merge those

techniques and share paths, to save power and area while retaining the output swing of those alternative basic topologies. Using both Barthelemy and Nauta techniques increases the common-mode rejection; however, it also decreases the output voltage excursion, which is not a problem for the Barthelemy/Manfredini hybrid OTA. Single-stage inverter-based OTAs output voltage excursion does not include the supply voltages, but their multi-stage counterparts have rail-to-rail output voltage excursion. Finally, feedforward active frequency compensation makes two-stage amplifiers stable, and as a bonus, it can also improve common-mode rejection.

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Abbreviations

The following abbreviations are used in this manuscript:

B	Barthelemy OTA
B/N	Barthelemy/Nauta hybrid OTA
B/M	Barthelemy/Manfredini hybrid OTA
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-mode Rejection Ratio
N	Nauta OTA
N/V	Nauta/Vieru hybrid OTA
M	Manfredini OTA
M/V	Manfredini/Vieru hybrid OTA
OTA	Operational Transconductance Amplifier
PSRR	Power-Supply Rejection Ratio
V	Vieru OTA

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