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A CMOS Voltage Reference with Output Voltage Doubling Using Modified 2T Topology

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Abstract: This paper presents an ultra-low power CMOS voltage reference which operates in the subthreshold region. Modified from the conventional 2T circuit, the proposed circuit is capable of generating higher output voltage by using the resistor subdivision. The design comprises a negative-threshold native NMOS transistor as the current generator, a high-threshold PMOS transistor as the active load and an active voltage doubling network to generate the reference voltage. Implemented in TSMC 40 nm CMOS technology, the proposed circuit operates at a minimum supply of 0.65 V and consumes 5.5 nA. Under one sample simulation, the obtained *T.C.* is 16.64 ppm/°C and the nominal V_{ref} is 489.6 mV (75.3% of V_{ddmin}) for the temperature range from −20 °C to 80 °C. For Monte-Carlo simulation of 200 samples at room temperature, the average output voltage is 488 mV and the average *T.C.* is 29.6 ppm/°C whilst with the standard deviation of 13.26 ppm/°C. Finally, at room temperature, the proposed voltage reference has achieved a process sensitivity (σ/μ) of 3.9%, a line sensitivity of 0.51%/V and a power supply rejection of −45.5 dB and −76.3 dB at 100 kHz and 100 MHz. Compared to the representative prior-art works realized in the same technology and a similar supply current, the proposed circuit has offered the best 1-sampe *T.C.*, the best average *T.C.* in multiple samples, the highest output voltage, the maximum output voltage per minimum supply voltage and the lowest process sensitivity in the output, V_{ref}.

Keywords: CMOS voltage reference; ultra-low power; subthreshold; current generator

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1. Introduction

With the rapid development of the Internet of Things (IoT), the Ultra-low power IoT design attracts many research attentions. Many biomedical devices, such as the Wireless Neural Recorder [1], Smart Contact Lens [2] and MEMS Heart Rate Sensor [3] have been designed to consume a few nanowatts of power, which aims to provide a long operation time whilst utilizing limited power sources. The voltage reference is one of the key circuit building blocks in these devices. As a result, there is a growing trend to employ ultra-low power voltage references to support the design of devices.

Conventional bandgap voltage references (BGR) implemented by the bipolar junction transistors (BJT) [4] have been widely explored. This BGR combines the complementary-to-absolute temperature (CTAT) voltage and the proportional-to-absolute temperature (PTAT) voltage to achieve a zero temperature coefficient (zero-*T.C.*) reference voltage. CTAT voltage (V_{be}) is generated by the voltage across the pn junction of BJT and PTAT voltage is derived through the difference of two emitter-base voltages (ΔV_{be}). The BJT voltage references have the key advantages of good precision and low temperature coefficient (*T.C.*). However, the voltage-mode reference voltage cannot be operated lower than 1.25 V due to the usual constraint of 0.7 V on V_{be} value. As such, the supply voltage V_{dd} cannot be made lower than 1 V, thus limiting the ultra-low voltage capability. In order to tackle the problem, the sub-1V BGR was proposed by using current mode topology [5]. A similar approach [6] was reported to reduce the supply voltage through resistor scaling for obtaining lower V_{be} so that it permitted higher headroom for low-voltage operational

amplifier implementation. In general, the use of BJT devices may be difficult to push for very low-power consumption. It is mainly because of the need for optimal bias currents for BJT devices for obtaining good thermal stability since β of BJT is a function of bias current. In another low-supply low-power topology [7], it adopted the supply-doubled circuit using the x2 charge pump and the switched-capacitor network to generate appropriate coefficients for both CTAT and PTAT voltages for better temperature compensation. The price paid for that was at the expense of increasing the circuit complexity. Regarding CMOS implementation, the popular low-power topologies [8–12] involved the principle of I-V conversion to generate a stable voltage reference output. This was pertaining to the application of a particular current source to the active load. The active load was realized in a group of saturation transistors [8,9], a single subthreshold transistor [9] or a group of sub-threshold transistors [11,12]. However, the saturation-based active load designs [8,9] operated beyond 1 V whilst the subthreshold-based active load designs suffered from higher *T.C.* [10], low output reference voltages [11] or higher supply voltage and power consumption [12]. Other common methods [13] for sub-1V voltage reference realization was to replace the BJT devices by the subthreshold MOS transistors in current mode topology. Unfortunately, the employment of an operational amplifier (op-amp) might increase the *T.C.* due to the mismatch in circuit components and the power consumption due to the circuit complexity through additional transistors and biasing network.

The trend towards ultra-low power and ultra-low supply is the recent design agenda, particularly in the area of Internet-of-Things (IoT) applications. This leads to another particular type of voltage references [14–17] where their topological simplicity meets the design objectives. This is usually achieved by realizing the current generator with either one single transistor or one cascode-based transistor for its IV conversion. The pioneer work [14] reported such a voltage reference topology to tackle the stated requirements. It was composed of two transistors, one of which served as the diode-connected active load, whereas another transistor served as the current generator. Due to the subthreshold operation, the circuit could achieve power consumption from the nanowatt down to the picowatt level. To provide another merit, several circuits [15,16] were also proposed to improve the line sensitivity. Since the value of the output voltage was determined by the difference between the threshold voltage of the two transistors, the output voltage was low (174 mV in [14]). To overcome this drawback, the work [14] introduced a stacked structure, whereas the work [17] proposed a scalable output structure by stacking the diode-connected PMOS load. A higher output voltage was attained but at the cost of degrading the *T.C.*, due to the increase in circuit sensitivity through the additional transistors. The motivation of this work is to devise an improved voltage reference topology for use in advanced nano-meter CMOS technology.

The paper is organized as follows. Section 2 reviews the representative prior-art works which include 2T [14], 3T [15], and 4T [16] voltage references in conjunction with other similar topologies [14,17] that offer higher output voltages. Section 3 describes the proposed topology and the circuit analysis. Section 4 presents the simulation results and discussions. This is then followed by a conclusion in Section 5.

2. Review of 2T Voltage Reference and Its Variants

The foundation topology of the 2T ultra-low power voltage reference [14] in Figure 1 was reported to consume only 2.22 pW in an ultra-low supply of 0.5 V. The circuit was made up of two NMOS transistors operating in the sub-threshold region, with M_1 using either a zero V_{th} or negative V_{th} device, whereas M_2 uses a high V_{th} based thick-oxide IO device. In order to obtain the reference voltage, M_2 functioned as an active load in a diode-connected form whereas M_1 served as an ultra-simple current source to inject the current to M_2 for IV conversion. The circuit can be explained intuitively in the following. Although the IV characteristic for the MOS device displays an exponential relationship under the sub-threshold region, the non-linear VI characteristic of M_1 is compensated by the active load in a reversed nonlinear IV characteristic. As a result, a constant output

voltage can be generated from the circuit, regardless of the nonlinear relationship between I and V parameters. As a result of the excellent innovation, the utmost simplicity in voltage reference design can lead to significant performance metrics in terms of ultra-low power consumption, low energy and small area implementation, which are particularly useful for today's IoT integrated circuits and systems.

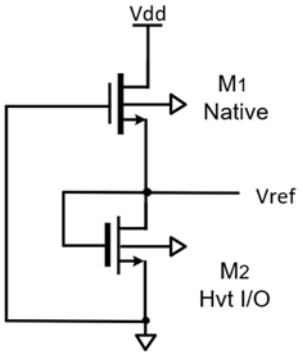

Figure 1. Schematic of Conventional 2T Voltage Reference.

Referring to Figure 1, assume that all transistors work in the subthreshold region with $V_{ds} > 4\ V_T$, and the respective drain-source current for M_1 and M_2 is approximated by

$$I_{D(M1)} = \mu_{n1} C_{ox1} \frac{W_1}{L_1} (m_1 - 1) V_T^2 \exp\left(\frac{-V_{ref} - V_{th1}}{m_1 V_T}\right) \quad (1)$$

$$I_{D(M2)} = \mu_{n2} C_{ox2} \frac{W_2}{L_2} (m_2 - 1) V_T^2 \exp\left(\frac{V_{ref} - V_{th2}}{m_2 V_T}\right) \quad (2)$$

where μ is mobility, C_{ox} is oxide capacitance, m is subthreshold factor ($m = 1 + C_{dep}/C_{ox}$) with C_{dep} denoted as depletion capacitance, V_{th} is threshold voltage, and V_T is thermal voltage ($V_T = \frac{kT}{q}$). Since I_{d1} equals to I_{d2}, the reference voltage [18] is obtained as

$$V_{ref} = \frac{m_1 V_{th2} - m_2 V_{th1}}{m_1 + m_2} + \frac{m_1 m_2}{m_1 + m_2} V_T ln\left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right) \quad (3)$$

When m_1 and m_2 are approximated as 1 [14], (3) can be approximated as follows

$$V_{ref} \approx \frac{m_1 m_2}{m_1 + m_2} \left[(V_{th2} - V_{th1}) + V_T ln\left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right)\right] \quad (4)$$

where m_1 and m_2 represent the subthreshold slope factor of M_1 and M_2, respectively. Since V_{th} has a negative *T.C.*, it can be written as

$$V_{th}(T) = V_{th}(T_0) - \alpha(T - T_0) \quad (5)$$

$V_{th}(T_0)$ is defined as the threshold voltage value at the reference temperature $T_0 = 300$ K, and α is the absolute temperature coefficient of V_{th}. Since V_{th} displays negative *T.C.* while V_T displays positive *T.C.*, by selecting the proper width and length ratio for M_1 and M_2, the temperature coefficient can be cancelled. The optimal transistor size that can be found to achieve zero TC is described as

$$\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} = \frac{\mu_2 C_{ox2} (m_2 - 1)}{\mu_1 C_{ox1} (m_1 - 1)} \exp\left[\frac{q}{k}\left(\frac{\alpha_2}{m_2} - \frac{\alpha_1}{m_1}\right)\right] \quad (6)$$

By substituting (6) in (3), the temperature-compensated V_{ref} is written as

$$V_{ref} = \frac{1}{m_1 + m_2}[(m_1 V_{th2}(T_0) - m_2 V_{th1}(T_0)) + (m_1\alpha_2 - m_2\alpha_1)T_0] \quad (7)$$

As particularly noted, from 49 dies, the best *T.C.* was 16.9 ppm/°C and the average *T.C.* was 62 ppm/°C, for the temperature range between −20 °C to 80 °C. Therefore, it is competitive for this type of voltage reference with respect to the conventional first-order compensated CMOS or BJT voltage references in the context of circuit simplicity and *T.C.* performance metric.

It can be found that the theoretical value of V_{ref} within zero-*T.C.* depends on the difference of V_{th} value (ΔV_{th}) between M_1 and M_2. Therefore, the maximum V_{ref} is limited by the types of devices which are being employed. However, the circuit is difficult to support when a higher output reference voltage is required in the circuit design. In addition, line sensitivity depends on the relative output resistance contributed by the respective device, M_1 and M_2. The native MOS device M_1 usually has poor output resistance when compared with that of IO device M_2. Long channel design should often be utilized to relax the issue.

A self-regulated 3T voltage reference [15], as depicted in Figure 2, was proposed to improve the line sensitivity when the design was targeted in 65 nm CMOS technology. It is mainly because the resistance of the device is lower in the advanced technology node.

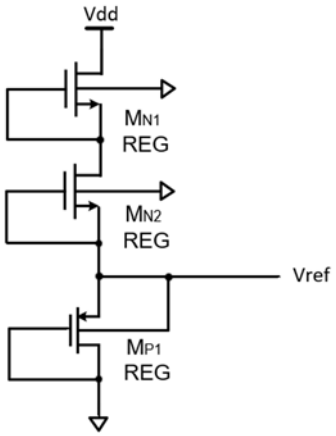

Figure 2. Schematic of the 3T Self-regulation Voltage Reference.

The reported design involved the addition of a self-regulated transistor M_{N1} on top of the current generator NMOS device M_{N2} and the PMOS active load M_{P1}. As such, the equivalent impedance between the output node and the minimum supply voltage was increased while the parasitic capacitor coupling effect between them was reduced. Hence, the line sensitivity of 3T topology was improved by 3.7× when compared with that of the 2T topology in [14]. Despite the 3T topology utilizing high threshold and long channel length devices to attain fW level power consumption, the *T.C.* was degraded to 252.2 ppm/°C. However, the low output voltage had the same design concern as the 2T voltage reference.

Differing from the 3T voltage reference [15], a self-cascode current source and a self-cascode active load were employed to constitute a 4T voltage reference [16] as shown in Figure 3. The obtained *T.C.* was 81.9 ppm/°C from −40 °C to 140 °C, with 256 Monte Carlo samples.

Although the fluctuation of supply voltage was reduced, the 4T voltage reference was not able to produce a higher output voltage. As can be seen, the higher output value is merely achieved by increasing ΔV_{th} between the current source and load transistors. Therefore, it is also often difficult to obtain high ΔV_{th} value.

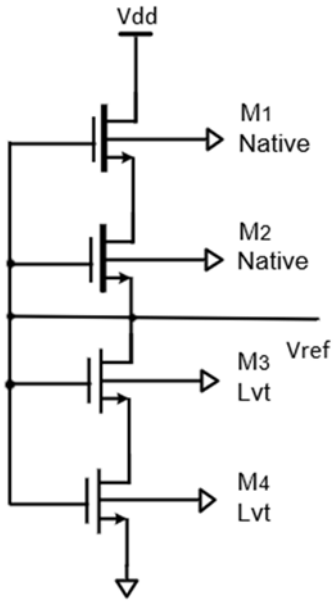

Figure 3. Schematic of the 4T Voltage Reference.

Other approaches based on the 2T based topology were proposed to yield a higher value of V_{ref}. The first design [14], as shown in Figure 4, made use of stacking two 2T voltage references to double the output voltage. It started with the first 2T voltage reference at the bottom level, the output of which was then used to drive the second 2T voltage reference in a cascade arrangement. The resulting output from the stacked topology would give a $\times 2$ output voltage. The penalty paid for that was the degradation of *T.C.* performance due to the increase of circuit sensitivity.

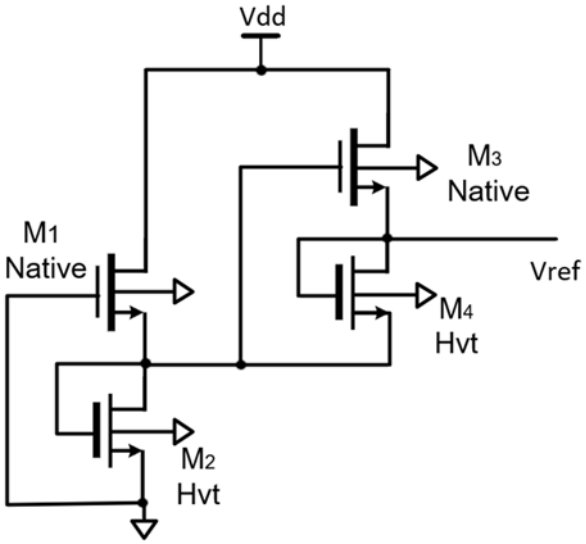

Figure 4. Schematic of Stacked 2T Voltage References to Obtain Higher Output Voltage.

Alternatively, by employing the stacked PMOS transistors in the active load as depicted in Figure 5 [17], it was able to produce the scalable output voltage. Compared with the stacking 2T circuit [14], only one current source was used to pass the current through the series-connected PMOS diodes. As a result, it allowed both the chip area and the power consumption to be saved. Moreover, another key advantage of the topology was that the output voltage was governed by the number of added PMOS devices. There was a trade-off between the power consumption and *T.C.* due to the leakage current flowing through the parasitic diode formed by the n-well and p-substrate of PMOS devices. The higher the output voltage, the larger the tradeoff between circuit sensitivity and *T.C.* performance metric.

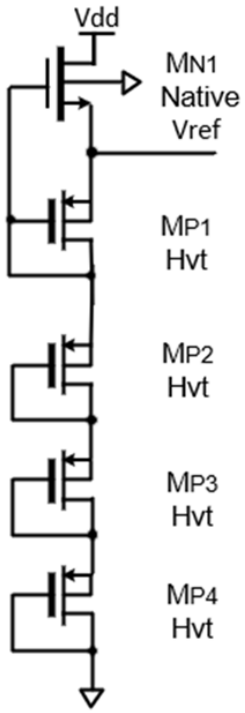

Figure 5. Schematic of Voltage Reference with Scalable Output.

3. Modified 2T Voltage Reference with Output Voltage Doubling

The proposed voltage reference topology is depicted in Figure 6a. It is designed using 40 nm of CMOS process technology. The circuit comprises of a current source using a native NMOS transistor M_1 with negative V_{th} and a diode-connected active load using a PMOS transistor M_2 with high V_{th}, in conjunction with two identical resistors, R_1 and R_2, as a resistive divider network to perform the voltage doubling function at the output of voltage reference. The reason to employ two identical resistors is to obtain the best matching characteristic. In addition, a non-dominant small current is designed to pass through the resistors so as to minimize the variation induced by resistors [19]. This can be achieved by means of a high resistance value. Unfortunately, the drawback of high resistance value is that of large chip size. Thus, the passive resistors, R_1 and R_2, will be replaced by the identical diode-connected PMOS transistors, M_3 and M_4, respectively. This gives the actual circuit as shown in Figure 6b. As particularly noted, the implementation of M_3 and M_4, is based on high-V_{th} PMOS transistors, taking advantage of lower mobility in p-type material. The resistive network permits the realization of a distributed RC filter by adding the capacitors, C_1 and C_2, thus resulting in a sharp roll-off characteristic, which is particularly important for power supply rejection (PSR) at high frequencies.

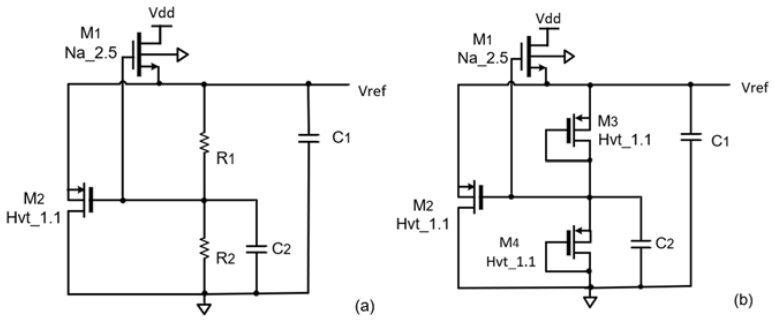

Figure 6. (**a**) Schematic of Modified Voltage Reference with Resistive Divider for Output Voltage Doubling (**b**) Schematic of Modified Voltage Reference with Diode-connected PMOS Active Divider for Output Voltage Doubling.

For a NMOS transistor to operate in the subthreshold region, the drain-source current is expressed as

$$I_{Dn} = \mu C_{ox} \frac{W}{L}(m-1)V_T^2 \exp\left(\frac{V_{gs} - V_{thn}}{mV_T}\right)\left[1 - \exp\left(-\frac{V_{ds}}{V_T}\right)\right] \tag{8}$$

When $V_{ds} > 4\ V_T$, the term $\exp\left(-\frac{V_{ds}}{V_T}\right)$ can be ignored. Hence, the drain-source current can be simplified in the form

$$I_{Dn} = \mu_n C_{ox} \frac{W}{L}(m-1)V_T^2 \exp\left(\frac{V_{gs} - V_{thn}}{mV_T}\right) \tag{9}$$

Similarly, for a sub-threshold biased PMOS transistor, the source-drain current is expressed as

$$I_{Dp} = \mu_p C_{ox} \frac{W}{L}(m-1)V_T^2 \exp\left(\frac{V_{sg} - \left|V_{thp}\right|}{mV_T}\right) \tag{10}$$

Since R_1 and R_2 are identical resistors, V_{ref} equals to 2 V_{sg} of M_2. Then, the corresponding current flowing through the transistor M_1, M_2 is given by

$$I_{Dn(M1)} = \mu_{n1} C_{ox1} \frac{W_1}{L_1}(m_1-1)V_T^2 \exp\left(\frac{-\frac{1}{2}V_{ref} - V_{th1}}{m_1 V_T}\right) \tag{11}$$

$$I_{Dp(M2)} = \mu_{p2} C_{ox2} \frac{W_2}{L_2}(m_2-1)V_T^2 \exp\left(\frac{\frac{1}{2}V_{ref} - |V_{th2}|}{m_2 V_T}\right) \tag{12}$$

where m_1 and m_2 represent the subthreshold factor of M_1 and M_2, respectively. $\frac{W_1}{L_1}$ and $\frac{W_2}{L_2}$ represent the effective aspect ratio of M_1 and M_2, respectively. The current flowing through M_1 is the sum of the current passing through M_2 and the current passing through R_1 and R_2, which is written as

$$I_R = \frac{V_{ref}}{R_1 + R_2} = \frac{V_{ref}}{2R} \tag{13}$$

where R represents the resistance value of R_1 and R_2 under identical design. The current relationship is obtained as

$$I_{Dn(M1)} = I_{Dp(M2)} + I_R \tag{14}$$

Using (11)–(14), the generated reference voltage is expressed as follows

$$Vref = 2\left[\frac{m_1|V_{th2}| - m_2 V_{th1}}{m_1 + m_2} + \frac{m_1 m_2}{m_1 + m_2} V_T ln\left(\frac{I_{s1} W_1 L_2}{I_{s2} W_2 L_1}\right) + \frac{m_1 m_2}{m_1 + m_2} V_T ln\left(1 - \frac{V_{ref}}{2R I_{Dn(M1)}}\right)\right] \tag{15}$$

where $I_s = \mu C_{ox}(m-1){V_T}^2$, which is the characteristic current for MOS transistor operating in subthreshold region. It can be observed that, when R is made as large as possible, the last term tends to be zero. Thus, when using large value resistors, (15) can be simplified as

$$Vref = 2\left[\frac{m_1|V_{th2}| - m_2 V_{th1}}{m_1 + m_2} + \frac{m_1 m_2}{m_1 + m_2} V_T ln\left(\frac{I_{s1} W_1 L_2}{I_{s2} W_2 L_1}\right)\right] \tag{16}$$

As mentioned in Section 2, V_T is a PTAT voltage, while ΔV_{th} is a CTAT voltage [20]. Thus, we have

$$V_{thn}(T) = V_{thn}(T_0) - \alpha_1(T - T_0) \tag{17}$$

$$\left|V_{thp}(T)\right| = \left|V_{thp}(T_0)\right| - \alpha_2(T - T_0) \tag{18}$$

where α_1 and α_2 denote as $\left|\frac{\partial V_{thn}(T)}{\partial T}\right|$ and $\left|\frac{\partial V_{thp}(T)}{\partial T}\right|$, respectively. It is the corresponding absolute value of temperature coefficient of threshold voltage for NMOS and PMOS device.

Thus, the rate of change of reference voltage with temperature can be obtained as

$$\frac{\partial V_{ref}}{\partial T} = 2\left[\frac{m_2\alpha_1 - m_1\alpha_2}{m_1 + m_2} + \frac{m_1 m_2}{m_1 + m_2}\frac{k}{q} ln\left(\frac{I_{s1}W_1L_2}{I_{s2}W_2L_1}\right)\right] \tag{19}$$

To achieve $\frac{\partial Vref}{\partial T} = 0$, the optimal aspect ratio for M_1 and M_2 to realize temperature compensation is given as

$$\frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}} = \frac{\mu_{p2}C_{ox2}(m_2 - 1)}{\mu_{n1}C_{ox1}(m_1 - 1)} \exp\left[\frac{q}{k}\left(\frac{\alpha_2}{m_2} - \frac{\alpha_1}{m_1}\right)\right] \tag{20}$$

Substituting (20) in (16), the temperature-compensated V_{ref} is simplified in the form

$$V_{ref} = \frac{2}{m_1 + m_2}[(m_1|V_{th2}(T_0)| - m_2V_{th1}(T_0)) + (m_1\alpha_2 - m_2\alpha_1)T_0] \tag{21}$$

Compared with (7) in the foundation 2T voltage reference, there is a multiplier of 2 in (21) from the proposed voltage reference. As a result of the sub-division method and identical design for resistors, R_1 and R_2, in Figure 6a, indicates that the output voltage is doubled. In addition, m_1 and m_2 nearly equal to 1, thus it also reveals that the output voltage with temperature compensation is determined by the difference of reference threshold voltage $\Delta V_{th}(T_0)$ and the difference of temperature coefficient of V_{th} between M_1 and M_2 ($\Delta\alpha = \alpha_2 - \alpha_1$). If $\Delta V_{th}(T_0)$ and $\Delta\alpha$ are made as large as possible, the highest output voltage value can be achieved. Here, PMOS with high V_{th} is used for M_2 because of its high absolute value of threshold voltage $|V_{th2}(T_0)|$ in the process technology. In addition, a PMOS transistor also presents a relatively high temperature coefficient of threshold voltage when compared with that of a NMOS transistor. This is because the terms determining α are φ_{ms} (the metal-semiconductor work function potential difference) and φ (the associated band bending), which adds together in the PMOS transistor, instead of compensating each other for the NMOS transistor [21].

Moreover, higher output resistance of the current source benefits PSR. In the design, a large channel length is set for native M_1 (L_1 = 22 µm) whereas a relatively smaller channel length (L_2 = 3 µm) is utilized for high-V_{th} M_2. The choice of M_2's channel length is to avoid the short-channel effect whilst providing good stability for transistor. For sustaining good PSR, the minimum approximated headroom of 200 mV is made for the V_{ds} of top transistor M_1.

Concerning the large value of resistors R_1 and R_2 to achieve better *T.C.*, the passive resistors are replaced by the diode-connected high-V_{th} PMOS transistors, M_3 and M_4. The dc resistance expressions for transistor M_3 and M_4 are obtained as follows:

$$R_{M3} = \frac{V_{ds(M3)}}{I_{Dp(M3)}} = \frac{V_{sd3}}{I_{s3}\frac{W_3}{L_3}\exp\left(\frac{V_{sg3-}|V_{th3}|}{m_3V_T}\right)} \tag{22}$$

$$R_{M4} = \frac{V_{ds(M4)}}{I_{Dp(M4)}} = \frac{V_{sd4}}{I_{s3}\frac{W_4}{L_4}\exp\left(\frac{V_{sg4-}|V_{th4}|}{m_4V_T}\right)} \tag{23}$$

From (22) and (23), the large resistance value is guaranteed by the small aspect ratio for each M_3 and M_4 in conjunction with the higher threshold voltages, V_{th3} and V_{th4} contributed by the high-V_{th} PMOS devices.

The capacitors C_1 and C_2 and the active resistors, realized by M_3 and M_4, serve as a distributed low-pass filter that provides a sharper roll-off characteristic. This significantly filters the high-frequency fluctuation from V_{dd} to the output through the devices. This improves the high-frequency PSR performance of the voltage reference. The sizes of devices in the design are listed in Table 1.

Table 1. Sizes of Devices in the Proposed Design.

Device	Type of Device	Size
M_1	Nch-na 2.5 V	17.3/22 (µm/µm)
M_2	Pch-hvt 1.1 V	9.9/3 (µm/µm)
$M_{3,4}$	Pch-hvt 1.1 V	200/22 (nm/µm)
$C_{1,2}$	MOM	2.5 pF

4. Results and Discussion

The proposed voltage reference is designed and implemented using TSMC 40 nm CMOS process technology. In order to compare different performance metrics of the 2T voltage reference [13] and its variants [14–17], the identical CMOS technology and similar level of current consumption is employed in each design. For filter capacitor used for PSR evaluation, identical capacitor size is adopted. In the comparative design, the supply current in each topology is set at about 5.5 nA, whereas the total capacitor size of each topology is 5 pF.

Refer to the modified topology in Figure 6b and other representative reported designs in Figure 7; all the component sizes and their responding values are listed in the corresponding Tables 1 and 2.

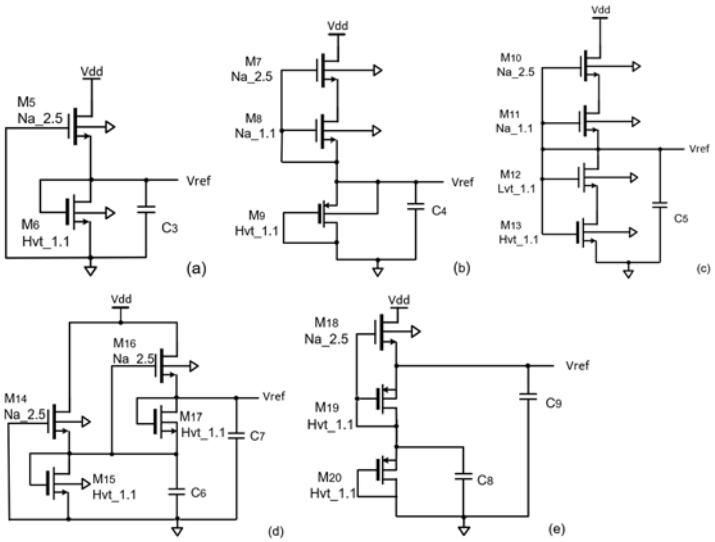

Figure 7. Schematic of Voltage References in 40 nm Process Technology (**a**) 2T Design (**b**) 3T Design (**c**) 4T Design (**d**) Stacked 2T Design (**e**) Scalable Output Design.

Regarding the performance of modified 2T topology, the obtained *T.C.* from one sample simulation is 16.64 ppm/°C for the temperature range from −20 °C to 80 °C shown in Figure 8. This yields 0.815 mV variation at the nominal V_{ref} of 489.63 mV. Consider 200 samples of Monte-Carlo simulation results that comprises within-die (WID) variation and die-to-die (D2D) variation as depicted in Figure 9; the average *T.C.* of the proposed work is 29.6 ppm/°C and the standard deviation of *T.C.* is 13.26 ppm/°C. From the *T.C.* performance metric comparison, although the 2T and its stacked topologies offer lower standard derivation of *T.C.*, with 8.19 ppm/°C and 9.1 ppm/°C, respectively, they display relatively higher values in average *T.C.*, with 42.06 ppm/°C and 49.71 ppm/°C, respectively. For 3T and 4T circuits, the topologies suffer from an even higher average *T.C.*,

with corresponding 71.43 ppm/°C and 91.01 ppm/°C. The same goes for their standard derivation of *T.C.*, with 41.79 ppm/°C and 53.45 ppm/°C, respectively. Finally, the scalable output topology offers 10.27 ppm/°C in the standard derivation of *T.C.* and 40.8 ppm/°C in the average *T.C.*

Table 2. Sizes of devices at different voltage reference designs in Figure 7.

Device	Type of Device	Size (*W*/*L*)	Device	Type of Device	Size (*W*/*L*)
M_5	Nch-na 2.5 V	4.9/22 (μm/μm)	M_{14}	Nch-na 2.5 V	2.05/22 (μm/μm)
M_6	Nch-hvt 1.1 V	3.8/3 (μm/μm)	M_{15}	Nch-hvt 1.1 V	3.4/3 (μm/μm)
M_7	Nch-na 2.5 V	1.95/22 (μm/μm)	M_{16}	Nch-na 2.5 V	2.05/22 (μm/μm)
M_8	Nch-na 1.1 V	1.95/22 (μm/μm)	M_{17}	Nch-hvt 1.1 V	3.4/3 (μm/μm)
M_9	Pch-hvt 1.1 V	5.5/2 (μm/μm)	M_{18}	Nch-na 2.5 V	17/22 (μm/μm)
M_{10}	Nch-na 2.5 V	18/5 (μm/μm)	M_{19}	Pch-hvt 1.1 V	12/3 (μm/μm)
M_{11}	Nch-na 1.1 V	1.66/22 (μm/μm)	M_{20}	Pch-hvt 1.1 V	12/3 (μm/μm)
M_{12}	Nch-lvt 1.1 V	45/10 (μm/μm)	C_3, C_4, C_5	MOM	5 pF
M_{13}	Nch-hvt 1.1 V	17/5 (μm/μm)	C_6, C_7, C_8, C_9	MOM	2.5 pF

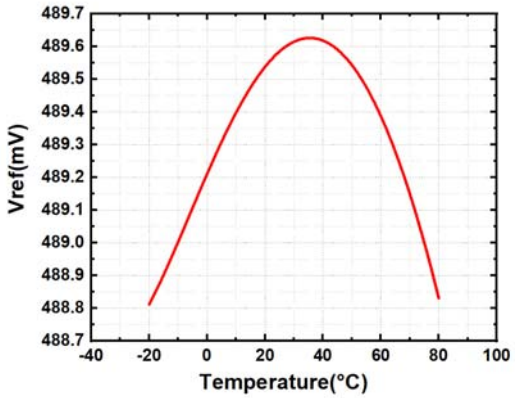

Figure 8. V_{ref} against Temperature for 1 Sample.

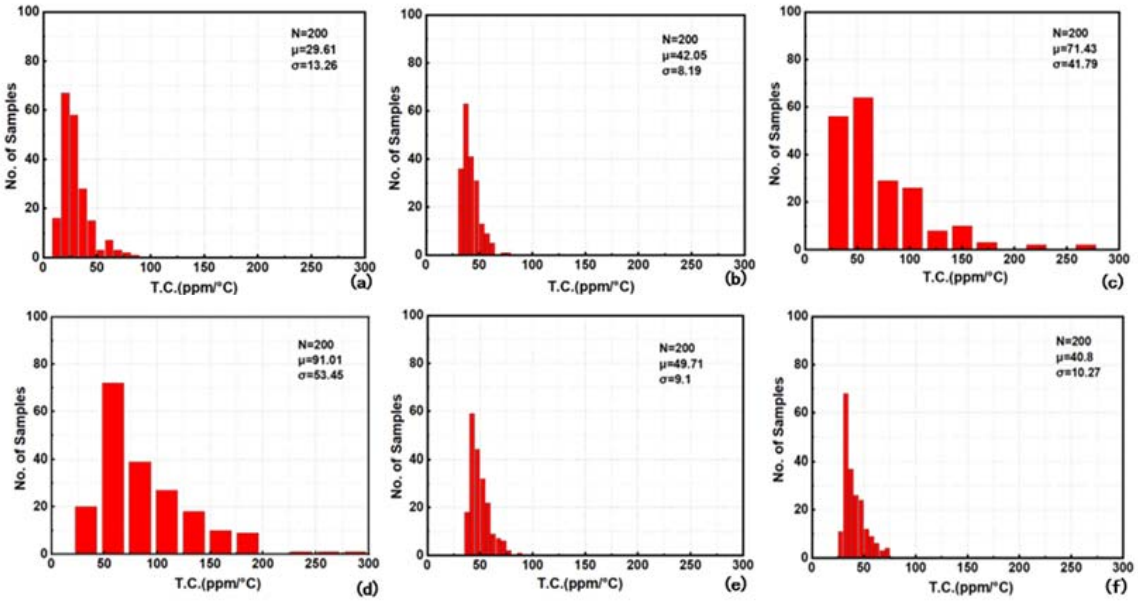

Figure 9. Monte-Carlo Simulation of *T.C.* of V_{ref} (**a**) Modified 2T with Output Voltage Doubling Topology (**b**) 2T Topology (**c**) 3T Topology (**d**) 4T Topology (**e**) Stacked 2T Topology (**f**) Scalable Output Topology.

Through the comparison with those of prior-art topologies, it is suggested that proposed topology displays the best value for one-sample *T.C.* and the average *T.C.* under

Monte-Carlo simulation with multiple samples. The standard derivation of *T.C.* is considered moderate and acceptable.

In order to evaluate the variation of V_{ref} among different topologies, the Monte-Carlo simulations are conducted for 200 samples, which take into account the WID variation and the D2D variation at a temperature of 27 °C, −20 °C and 80 °C in Figures 10–12, respectively. Refer to the simulation results at a nominal temperature of 27 °C in Figure 10; the average V_{ref} of the proposed work is 488 mV. As can be observed, the obtained output voltage is higher than those of 2T, 3T and 4T, stacked 2T and scalable output circuits. The process sensitivity of the proposed work gives σ/μ = 3.9%. It is the lowest value with respect to those having 4.66%, 6.1%, 9.3%, 4.9% and 4.2% for 2T, 3T, 4T, stacked 2T and scalable output circuits, respectively. When operating at corner temperatures of 20 °C and 80 °C in Figures 11 and 12, respectively, it can be observed that all the topologies have no significant change on the performance parameters. This has demonstrated that 2T based voltage references together with the variants are robust in nature. The stems from the topological simplicity in this category of voltage reference.

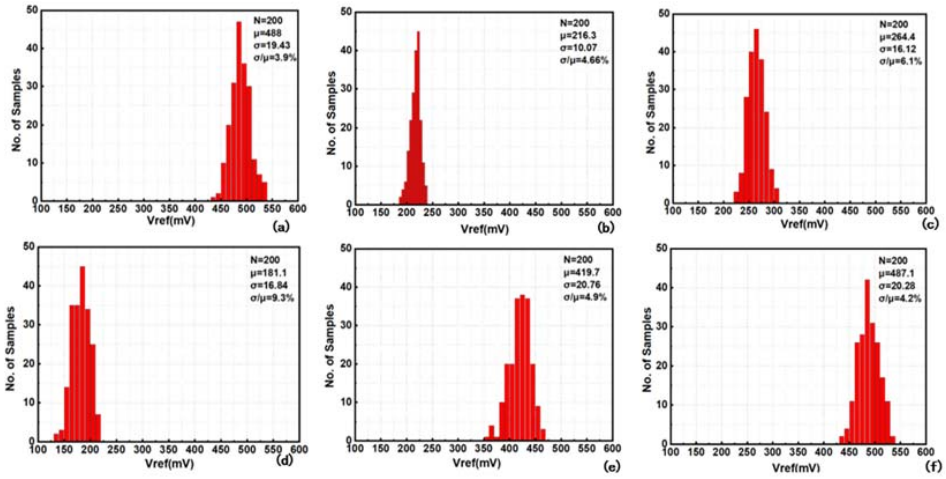

Figure 10. Monte-Carlo Simulation of V_{ref} @27 °C (**a**) Modified 2T with Output Voltage Doubling Topology (**b**) 2T Topology (**c**) 3T Topology (**d**) 4T Topology (**e**) Stacked 2T Topology (**f**) Scalable Output Topology.

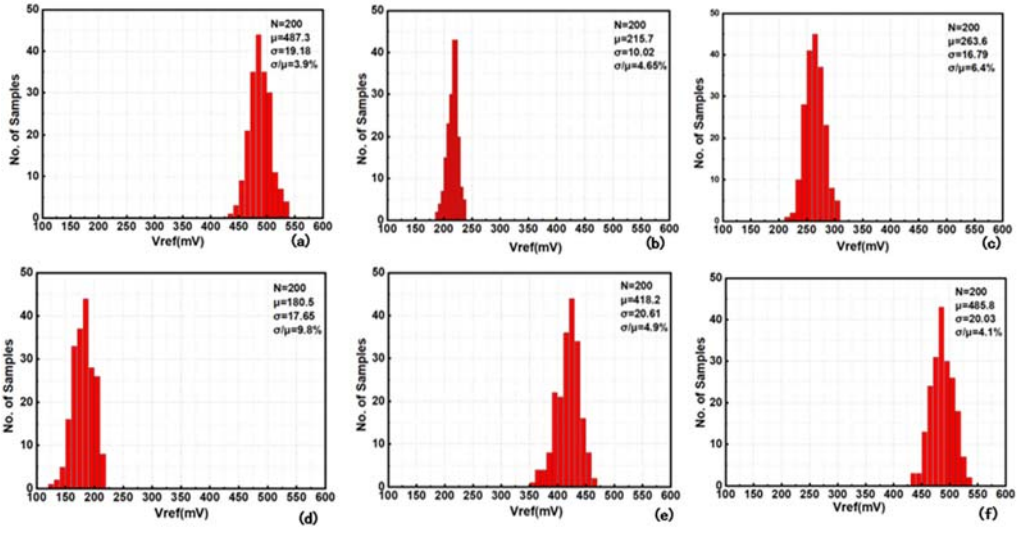

Figure 11. Monte-Carlo Simulation of V_{ref} @−20 °C (**a**) Modified 2T with Output Voltage Doubling Topology (**b**) 2T Topology (**c**) 3T Topology (**d**) 4T Topology (**e**) Stacked 2T Topology (**f**) Scalable Output Topology.

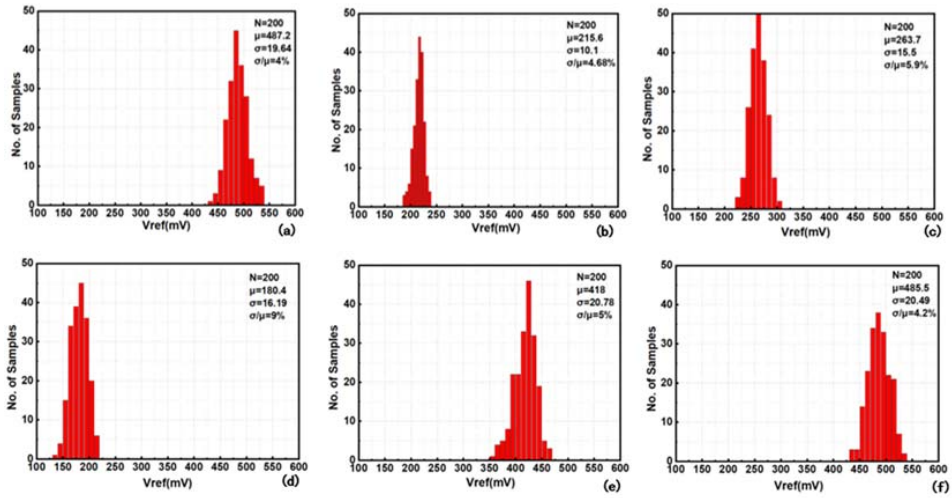

Figure 12. Monte-Carlo Simulation of V_{ref} @80 °C (**a**) Modified 2T with Output Voltage Doubling Topology (**b**) 2T Topology (**c**) 3T Topology (**d**) 4T Topology (**e**) Stacked 2T Topology (**f**) Scalable Output Topology.

Figure 13 presents the PSR plot of the proposed work and its comparison with other topologies. As can be observed, the 3T and 4T circuits exhibit high lower frequency PSR values. This is due to the cascode arrangement for the top transistor. The rest of the other circuits, including the proposed work, offer medium values for low-frequency PSR. This is due to the finite device's output resistance contributed by the 40 nm technology node. In this work, the obtained PSR is −45.5 dB at low frequency (100 kHz) and −76.3 dB at high frequency (100 MHz). The high frequency PSR is comparable with a majority of topologies. This is adequate for many analog circuit applications. Finally, all the simulation results pertaining to temperature of 27 °C, −20 °C and 80 °C are summarized and compared in Tables 3–5, respectively. The 2T circuit displays the lowest operation supply voltage among all the topologies, which is considered the key advantage. Regarding the proposed work, it has the disadvantage of a slight increase in minimum supply voltage, which is similar to the scalable output voltage topology. However, the proposed work offers the best 1-sample *T.C.*, the best average *T.C.* under multiple samples, the highest output voltage as well as the maximum output voltage per minimum supply voltage. Additionally, it also gives low process sensitivity to V_{ref} because it keeps the property of simplicity similar to that of conventional 2T topology. Although the *T.C.* process sensitivity is in moderate value, it is still acceptable because low average *T.C.* is achieved in the proposed topology. The line sensitivity of the current work is reasonable. The slight degradation is due to the voltage headroom consumed by the PMOS diodes for the resistive divider. Nevertheless, the proposed work is a useful voltage reference block which offers balanced and comparable performance metrics.

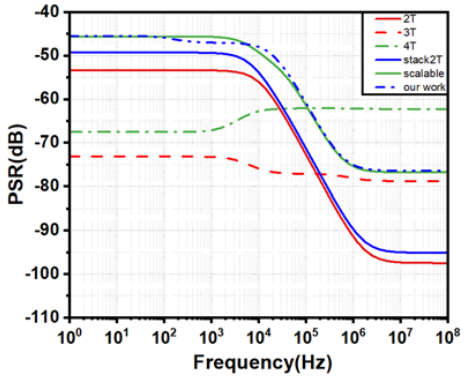

Figure 13. PSR of the Proposed Voltage Reference and its Comparison with Other Designs.

Table 3. Performance Comparison of the Simulation Results at 27 °C.

@27 °C	2T	3T	4T	Stacked 2T Topology	Scalable Output Topology	Modified 2T with Double Output Topology
Minimum V_{dd} (V)	0.4	0.6	0.6	0.6	0.65	0.65
T.C.[1] @1 sample (ppm/°C)	32.22	26.97	40.17	38.54	30.28	16.64
Mean *T.C.* @200samples (ppm/°C)	42.05	71.43	91.01	49.71	40.8	29.6
SD *T.C.* @200samples (ppm/°C)	8.19	41.79	53.45	9.1	10.27	13.26
Average V_{ref} @200samples (mV)	216.3	264.4	181.1	419.7	487.1	488
Maximum V_{ref} @200samples (mV)	238	306.4	215.2	466	534.7	539.3
Process Variation of V_{ref} (%)	4.7%	6.1%	9.3%	4.9%	4.2%	3.9%
LS [2] (%/V)	0.46%/V (0.4–1 V)	0.03%/V (0.6–1.2 V)	0.12%/V (0.6–1.2 V)	0.43%/V (0.6–1.2 V)	0.51%/V (0.65–1.25 V)	0.51%/V (0.65–1.25 V)
PSR (dB) @ 100 kHz	−53.4~	−73.2~	−67.5~	−49.3~	−45.6~	−45.5~
@ 100 MHz	−97.5	−78.8	−62.3	−95.1	−76.7	−76.3
Power Consumption (nW)	2.228	3.27	3.32	3.31	3.575	3.614
Output Voltage/V_{ddmin} @1 sample (%)	54%	44.1%	30.2%	70%	75%	75.3%

[1] $T.C. = [\Delta V_{ref}/(\Delta T \times V_{ref\_normal})] \times 10^6$ ppm/°C. [2] $LS = \Delta V_{ref}/(V_{ref\_average} \times \Delta V_{dd})$%/V.

Table 4. Performance Comparison of the Simulation Results at −20 °C.

@−20 °C	2T	3T	4T	Stacked 2T Topology	Scalable Output Topology	Modified 2T with Double Output Topology
Minimum V_{dd} (V)	0.4	0.6	0.6	0.6	0.65	0.65
T.C. @1 sample (ppm/°C)	32.22	26.97	40.17	38.54	30.28	16.64
Mean *T.C.* @200samples (ppm/°C)	42.05	71.43	91.01	49.71	40.8	29.6
SD *T.C.* @200samples (ppm/°C)	8.19	41.79	53.45	9.1	10.27	13.26
Average V_{ref} @200samples (mV)	215.7	263.6	180.5	418.2	485.8	487.3
Maximum V_{ref} @200samples (mV)	237.2	307	216.5	464.5	533.2	537.2
Process Variation of V_{ref} (%)	4.7%	6.4%	9.8%	4.9%	4.1%	3.9%
LS (%/V)	0.5%/V (0.4–1 V)	0.02%/V (0.6–1.2 V)	0.1%/V (0.6–1.2 V)	0.39%/V (0.6–1.2 V)	0.48%/V (0.65–1.25 V)	0.44%/V (0.65–1.25 V)
PSR (dB) @ 100 kHz	−55.0~	−76.3~	−70.5~	−51.0~	−47.5~	−47.5~
@ 100 MHz	−103.0	−79.8	−62.3	−99.9	−80.1	−79.7
Power Consumption (nW)	0.356	0.43	0.44	0.513	0.44	0.44
Output Voltage/V_{ddmin} @1 sample (%)	54%	44%	30%	69.4%	74.8%	75.2%

Table 5. Performance Comparison of the Simulation Results at 80 °C.

@80 °C	2T	3T	4T	Stacked 2T Topology	Scalable Output Topology	Modified 2T with Double Output Topology
Minimum V_{dd} (V)	0.4	0.6	0.6	0.6	0.65	0.65
T.C. @1 sample (ppm/°C)	32.22	26.97	40.17	38.54	30.28	16.64
Mean *T.C.* @200samples (ppm/°C)	42.05	71.43	91.01	49.71	40.8	29.6
SD *T.C.* @200samples (ppm/°C)	8.19	41.79	53.45	9.1	10.27	13.26
Average V_{ref} @200samples (mV)	215.6	263.7	180.4	418	485.5	487.2
Maximum V_{ref} @200samples (mV)	237.4	305.1	212.8	463.8	533.2	539.4
Process Variation of V_{ref} (%)	4.7%	5.9%	9%	5%	4.2%	4%
LS (%/V)	0.57%/V (0.4–1 V)	0.04%/V (0.6–1.2 V)	0.14%/V (0.6–1.2 V)	0.48%/V (0.6–1.2 V)	0.55%/V (0.65–1.25 V)	0.54%/V (0.65–1.25 V)
PSR (dB) @ 100 kHz	−50.9~	−68~	−63.5~	−46.7~	−43.3~	−43~
@ 100 MHz	−91.5	−77	−62.2	−89.4	−73.3	−73
Power Consumption (nW)	9.26	16.08	16.12	15.29	19.11	18.79
Output Voltage/V_{ddmin} @1 sample (%)	54%	44%	30%	69.4%	74.8%	75.2%

5. Conclusions

An improved voltage reference topology which is modified on the basis of the conventional 2T circuit is proposed in this work. Under the design at identical 40 nm CMOS technology and similar level of supply current consumption, the comparative simulation results have shown that the proposed circuit exhibits the best 1-sample *T.C.* and 200-sample average *T.C.* and the lowest process sensitivity with respect to that of the representative topologies such as 2T, 3T, 4T, stacked-2T and scalable output topologies. Additionally, the generated reference output voltage is also higher than 2T, 3T, 4T, stacked-2T and scalable output circuits, yielding maximum output voltage per minimum supply voltage. Finally, the proposed circuit provides balanced and comparable performance metrics in terms of line sensitivity and PSR. The voltage reference is very useful for the ultra-low power IoT applications.

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