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Signal Amplification by Means of a Dickson Charge Pump: Analysis and Experimental Validation

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Abstract: Recently, with the aim of extending the use of the CP in all those applications where a time-variant signal must be amplified with its DC component above the positive power supply rail, the signal amplification feature of a conventional Dickson charge pump (CP) has been investigated, introducing a small-signal model for each particular condition in which a CP can work. In this paper this idea is further investigated, especially under the slow switching limit (SSL) condition, and experimental validation has been carried out using a 65 nm CMOS technology for four different voltage gain values. Starting from an equivalent model of the CP, the main small- and large-signal parameters are analytically derived and discussed in depth. As a proof of concept, experimental measurements on four CPs with different numbers of stages confirm the validity of this unconventional application and the effectiveness of the CP when used as an amplifier.

Keywords: amplifier; DC–DC converters; Dickson charge pump; switched capacitor circuits



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1. Introduction

Since the first monolithic implementation [1], charge pumps (CPs) have been employed for on-chip generation of voltages that stay within the supply rails, behaving as a buck converter, or can reach a level off the supply rails, acting like a booster converter or a negative voltage generator [2–4]. The first integrated CP, the Dickson one [1], targeted the generation of the high voltages necessary to write or erase data, typically 30–40 V, in the nonvolatile memory circuits. Successively, other topologies, such as the Fibonacci, the serial-to-parallel and the exponential [5–10], as well as different design optimization strategies and ameliorative solutions of the Dickson CP have been introduced in the literature to cope with the relentless evolution of the applications.

In particular, detailed behavioral models of Dickson CP with an arbitrary number of stages were introduced in [11,12] and recently revised in [13] by using an all-resistor equivalent model in order to enrich the know-how about these blocks. Design strategies as a function of the output capacitive load were proposed in [14–16] with the goal to speed-up the CP and decrease output voltage ripple in low-output current applications. In [17], the suggested design strategy aimed to decrease switching power losses and increase the power conversion efficiency, and a topology based on this strategy was introduced in [18] targeting solid-state memories.

More recently, CP solutions for different types of input sources have been studied and presented. For example, in [19], a charge pump system for a flexible thermoelectric generator (TEG) with high-output impedance was described. In this case, despite the high-output impedance of the used TEG, the system controls the input voltage to keep it higher than the minimum operating voltage by modulating the input impedance of the charge pump using two-phase operation with low- and high-input impedance modes.

Dickson-based CP topologies for energy harvesting, able to be coupled with very-low voltage generators, such as TEGs, are also now an established hot topic. See, for

example, [20,21], where the topologies presented enable low-voltage operation while maintaining good output current drivability.

Compared to other topologies, the Dickson CP is the least sensitive to parasitic effects and shows the smallest total capacitor area and the highest power efficiency. Therefore, the Dickson CP is the best option for integration and has become the widest adopted and studied topology. Indeed, nowadays CPs are generally used in power management units (PMUs) for an extended variety of ICs, such as the energy-autonomous nodes for the Internet of Things (IoT) and the Internet of Medical Things (IoMT), or the powered platform for the lab-on-a-chip paradigm [6,10,22,23].

Despite the huge recent growth of the number of works dealing with CPs [10], only very few of them exploit these circuits in atypical applications. Among these, in [24,25] a time-mode flash ADC exploits CPs as a part of the variable-slope voltage-to-time converter, enabling fast conversion thanks to the inherent voltage boosting operation of the CP. Another application involves CPs to re-distribute the charge inside strings of solar cells to reduce mismatches and shading effects [26,27]. Moreover, NMOS LDOs can take advantage of CP circuits to achieve low line and load sensitivities while keeping good performance in terms of drop-out voltage [28].

With the aim of extending the use of the CP in all those applications where a time-variant signal must be amplified with its DC component above the positive power supply rail, recently the authors presented the original idea to use the CP as a signal amplifier; as a preliminary proof of concept, the idea was tested for only one voltage gain value, about equal to five (i.e., only four stages) and by using an almost old 130 nm CMOS technology [29].

In this paper the novel and unconventional idea to use a CP as a signal amplifier is expanded in terms of further investigation under the slow switching limit (SSL) condition. Moreover, a wider experimental validation is carried out by using a 65 nm CMOS technology (a more scaled technology than the one in [29]) since CPs for four different voltage gains are designed and tested. In particular, four Dickson CPs, which differ for the number of stages, are designed with a 65 nm CMOS technology and experimentally tested. The behavior of the CP as an amplifier is analyzed using an equivalent model through which equations for the main design specifications are carried out and the analytical description and the developed model find a high level of agreement with the experimental results.

The paper is organized as follows. In Section 2, after some general considerations, the DC behavior of CP is exploited to introduce the small-signal equivalent model under the SSL condition. In particular, each parameter is derived and used to give the required information on both the small- and the large-signal CP performances. In Section 3, the transistor-level implementation of a proof-of-concept is analyzed, and the experimental setup together with the obtained results are reported and extensively discussed. Finally, in Section 4 concluding remarks are given.

2. The Equivalent Model of the CP

2.1. General Considerations

Let us consider the simplified schematic of a Dickson CP as shown in Figure 1. Each switch allows the one-directional transfer of the charge from the input to the output, and it can be implemented using different circuit topologies, as diodes, diode-connected transistors, or active switches involving more than one transistor, such as the cross-coupled topology [10]. Each stage of the CP is made up by a switch and a pumping capacitor, C , whose value is assumed to be constant. Finally, the output block comprises a capacitor, C_L , which also models the input capacitance of the circuits driven by the CP, and a bias current generator, I_{BIAS} , which sets the quiescent point of the CP with the DC input voltage.

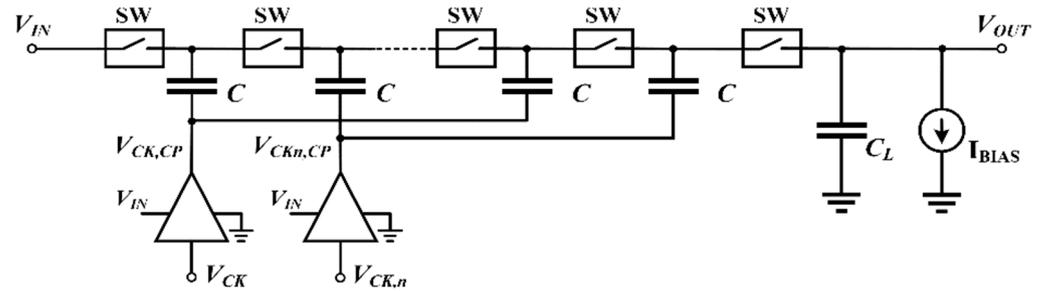


Figure 1. Simplified schematic of a Dickson charge pump.

It is worth noting that in Figure 1, unlike the conventional CP scheme, the input voltage, V_{IN} , is connected also to the buffers driving the pumping capacitors. Adopting this solution, the digital buffers behaves as a two-input MUX and the output signals, $V_{CK,CP}(t)$ and $V_{CKn,CP}(t)$, are then given by

$$V_{CK,CP}(t) = V_{IN}(t) \cdot \Pi\left(\frac{t}{T_s}\right) \tag{1}$$

$$V_{CKn,CP}(t) = V_{IN}(t) \cdot \Pi\left(\frac{t}{T_s} + \frac{1}{2}\right) \tag{2}$$

where the canonical function $\Pi(t/T_s)$ represents a square wave with a period equal to T_s and high and low level equal to 1 and 0, respectively.

Note that the minimum and maximum $V_{IN,DC}$ values depends on the adopted technology. Indeed, they are fixed by the breakdown voltage of both the capacitors and the transistors, which limits the maximum value, and the device’s threshold voltage, which determines the input minimum value.

Similarly to the study of a traditional amplifier, the input signal can be split into the DC and AC components, $V_{IN,DC}$ and $v_{in,ac}(t)$, respectively, whose relationship satisfies the small signal condition (i.e., $v_{in,ac} \ll V_{IN,DC}$).

2.2. DC Behavior

As shown in [5], considering the DC component of the input signal only, the CP in Figure 1 can be modeled using the equivalent circuit shown in Figure 2, whose output voltage DC component is $V_{OUT,DC}$. The input current source, $I_{IN,SW}$, models the switching losses due to the stray capacitance of the stage capacitors, and is expressed by

$$I_{IN,SW} = 0.5N(C_B + C_T)f_s V_{IN} \tag{3}$$

where C_B and C_T are the bottom and top parasitic capacitance of each pumping capacitor, respectively.

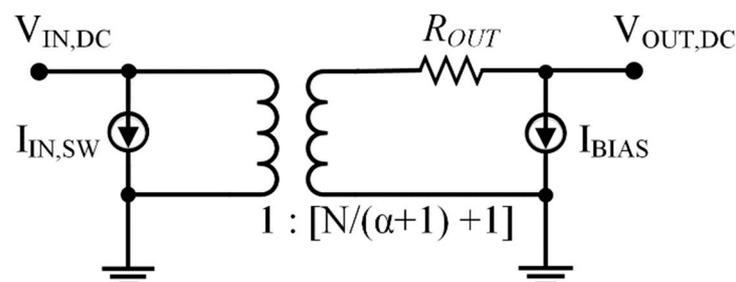


Figure 2. Equivalent static model of the CP.

When the clock period is high enough to allow the complete charge transfer from one stage to the following one, the CP works in the slow switching limit (SSL) [5]. In this condition, the output resistance can be expressed by

$$R_{OUT} = \frac{N}{(1 + \alpha)Cf_s} \tag{4}$$

where N is the number of stages and the factor α is the ratio between the top parasitic capacitance and the nominal value of the stage capacitance.

The ideal transformer in Figure 2 models the voltage gain, which is the main outcome of the charge pumping mechanism. Therefore, by analyzing the circuit in Figure 2, the $V_{OUT,DC}$ is analytically given by

$$V_{OUT,DC} = \left(\frac{N}{1 + \alpha} + 1 \right) V_{IN,DC} - R_{OUT}I_{BIAS} \tag{5}$$

2.3. AC Behavior in SSL

Without loss of consistence, in the analysis to come we neglect the on-resistance of the PMOS (i.e., the pull up network) of the buffers. Indeed, in practical cases such resistance can be made negligible by sizing the transistors of the buffers opportunely large. (This design strategy is conventionally adopted for CP-based on-chip voltage generation. However, for the MOSFETs of the buffers involved in the path of all CP currents, their on-resistances increase the total equivalent resistance seen by the pumping capacitors. Thus, the width of the SSL domain is reduced and, equivalently, the CP is pushed to go to and enter into the FSL domain. However, in such a case, the model to be used is another one (see ref. [29]).) Moreover, assuming the adoption of non-overlapping clock signals, we also neglect the short circuit currents of the buffers. In addition, we assume that the reverse current of the switches is negligible. Finally, we suppose that the output capacitive load, C_L , is small enough in comparison to the CP pumping capacitance that its effect can be initially neglected.

Under the SSL condition, the Dickson CP in Figure 1 can be modeled through the small-signal equivalent circuit shown in Figure 3.

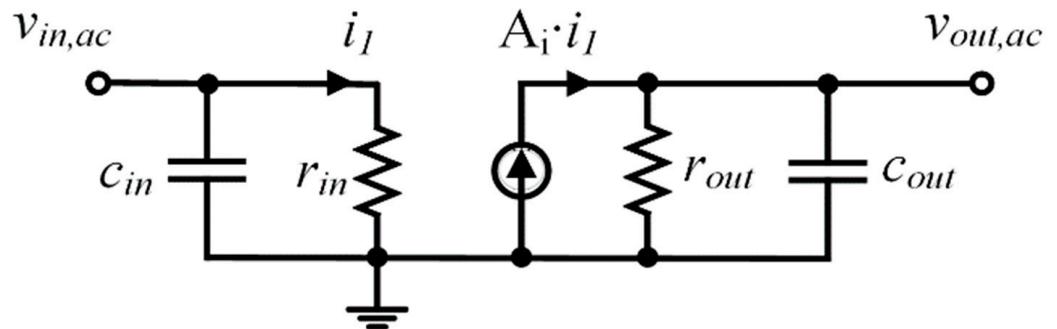


Figure 3. Small signal equivalent model of the CP working in SSL.

Parameters c_{in} and r_{in} model the input impedance of the CP. In particular, from Figure 3, the capacitance c_{in} corresponds to the total capacitive load of the buffers (i.e., the total parasitic bottom plate capacitance); thus,

$$c_{in} = NC_B \tag{6}$$

Considering that in the SSL the CP can be supposed to work like a switched-capacitor (SC) circuit, and remembering that the SC small-signal resistance is proportional to T_S/C [5], for a series of N stages we can write

$$r_{out} = \frac{N}{(1 + \alpha)Cf_S} \quad (7)$$

Neglecting losses, from Figure 2 the input power is equal to the output power; thus, we can write

$$r_{in} = r_{out} \left(\frac{i_{out}}{i_{in}} \right)^2 = \frac{N}{\left[\frac{N}{1+\alpha} + 1 \right]^2} \frac{1}{(1 + \alpha)Cf_S} \quad (8)$$

To analyze how the CP transports the total input current through the different stages up to the output node, let us consider a Gaussian curve around the CP. Applying Kirchhoff's current law in steady-state, the total current flowing into the CP is equal to $(N/(1 + \alpha) + 1)$ -times the one that flows out during each clock period. Consequently, the current gain, A_i , of the current-controlled current source generator is equal to $1/(N/(1 + \alpha) + 1)$.

Finally, the CP small signal output capacitance is expressed by

$$c_{out} = \frac{A(N)}{N}(1 + \alpha)C \quad (9)$$

whose values coincides with the switching impedance of the pumping capacitors and, thus, to the CP self-capacitance [12]. The function $A(N)$ was introduced in [12] and its value is reported here as

$$A(N) = \frac{N(4N^2 + 3N + 2)}{12(N + 1)}, \text{ for even } N \quad (10)$$

$$A(N) = \frac{4N^2 - N - 3}{12}, \text{ for odd } N \quad (11)$$

The output impedance introduces an intrinsic pole which defines the bandwidth of the CP. Hence, the CP transfer function can be expressed as

$$H_{CP}(s) = \frac{\frac{N}{1+\alpha} + 1}{1 + \frac{s}{\omega_{pi}}} \quad (12)$$

where the intrinsic pole frequency, ω_{pi} , is given by

$$\omega_{pi} = \frac{1}{A(N)}f_S \quad (13)$$

The intrinsic pole in (13) depends on the clock frequency, f_S , and approaches the value $3f_S/N^2$ for $N > 4$. Considering the CP capacitive extrinsic load, C_L , the resulting pole frequency is given by

$$\omega_P = \frac{1}{r_{out}(C_L + c_{out})} \approx \frac{C}{NC_L}f_S \quad (14)$$

where the rightmost approximation holds when C_L is greater than the CP self-capacitance expressed in (9). From (14), ω_P is inversely proportional to the number of stages, N , whereas the intrinsic pole, ω_{pi} , is inversely proportional to N^2 .

2.4. Small- and Large-Signal Analysis

A simplified expression of the intrinsic gain-bandwidth product (GBW) can be defined for a CP considering the ideal gain, $N/(1 + \alpha) + 1$, and the bandwidth fixed by the pole frequency derived in the previous section, thus yielding

$$GBW = \frac{\frac{N}{1+\alpha} + 1}{2\pi r_{out}(C_L + c_{out})} \tag{15}$$

A key amplifier parameter for large-signal behavior is the slew rate (SR). In a CP used as a single-stage amplifier, the SR is limited by the maximum charging/discharging current provided by the charge transfer mechanism. Thus, considering that the charge level of the output capacitor can be changed by the input current and the bias current only, the SR can be expressed as

$$SR \approx \min \left[\frac{I_{BIAS}}{C_L + c_{out}}, \frac{v_{out,ac}}{r_{out}(C_L + c_{out})} \right] \tag{16}$$

Note that since $I_{BIAS}/(C_L + c_{out})$ or $v_{out,ac}/r_{out}(C_L + c_{out})$ is proportional to the gain-bandwidth product, an increase of the GBW generates a proportional increase of the SR .

3. Experimental Validation

To verify the behavior of the unconventional use of the CP as a signal amplifier and validate the analytical model derived, four CPs with different numbers of stages (namely $N = 2, 4, 6$ and 8 with nominal gain equal to $3\times, 5\times, 7\times$ and $9\times$, respectively) were implemented using the 65 nm triple-well CMOS technology provided by STMicroelectronics. Figure 4a shows the schematic of the adopted switch which is referred to as dual-branch cross-coupled topology (also named “latched”) [30–32]. The bottom of Figure 4a shows the layout of the CPs superimposed over the chip microphotograph. The occupied area is $56 \times 101 \mu\text{m}^2, 56 \times 220 \mu\text{m}^2, 56 \times 330 \mu\text{m}^2$ and $56 \times 440 \mu\text{m}^2$ for the 2-, 4-, 6- and 8-stage CP, respectively.

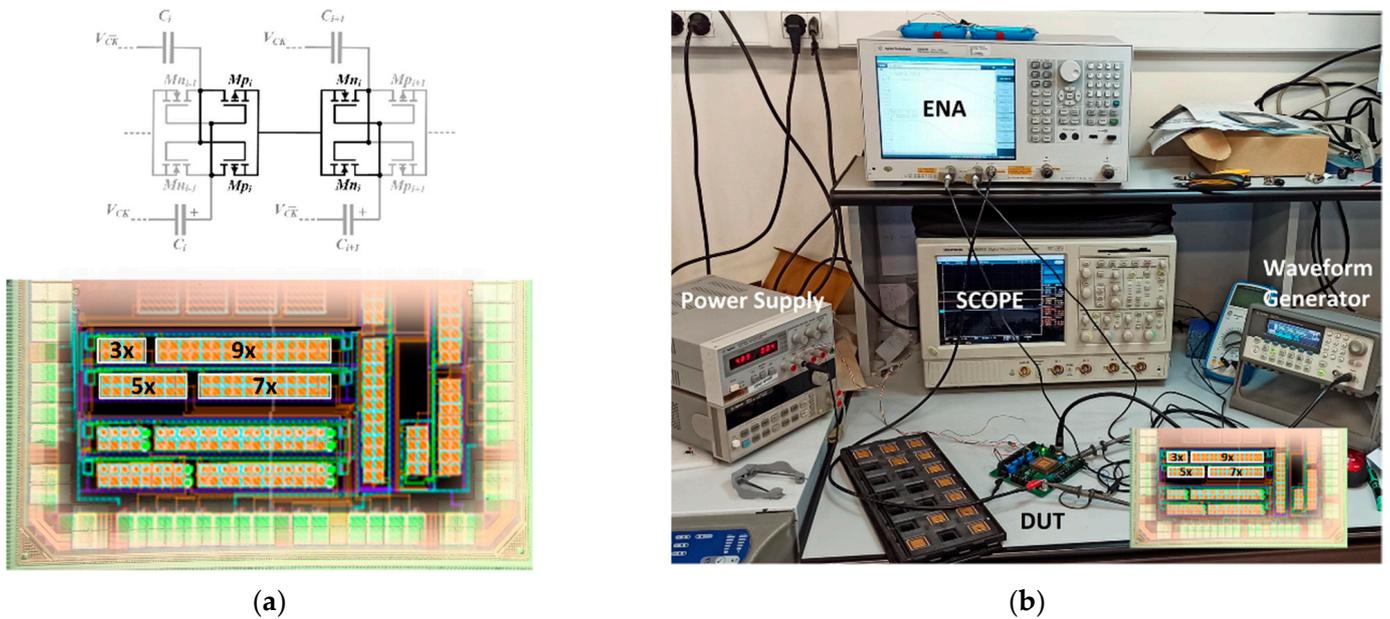


Figure 4. (a) Simplified circuit diagram of a stage of the CP (top) and layouts of the CPs superimposed on the chip photo (bottom); (b) experimental setup.

Design constraints have been set as $f = 1 \text{ MHz}$, $I_{BIAS} = 0.1 \mu\text{A}$ and $V_{IN,DC} = 300 \text{ mV}$. The value of the pumping capacitances is $C = 10 \text{ pF}$ and they are implemented with MIM technology, which provides high specific capacity and low top stray capacitance ($\alpha = 0.04$).

The NMOS and PMOS transistors all have a $0.1 \mu\text{m}$ channel length and an aspect ratio equal to 100. The clock buffers are opportunely sized to not affect the CP responses. In particular, they are implemented by using conventional CMOS inverters whose aspect ratios of PMOS and NMOS transistors are 100 and 200, respectively, with a channel length equal to 60 nm . Finally, an external capacitance equal to 50 pF is connected at the output of each CP (comprising the capacitive contributions of the oscilloscope probe, package and PCB connections, with an externally added capacitor to reach the accurate value).

Figure 4b shows the experimental setup involving an oscilloscope, a power supply for input voltage supplement, a waveform generator and a network analyzer (ENA) to allow transient and AC measurements. The PCB prototype hosts the test chip (DUT). All the circuits have been characterized for small- and large-signal response over 10 samples.

Figure 5 shows the transient output of the CPs in the SSL for a 500 Hz , 50 mV input square wave. The voltage gain is equal to 2.9, 4.7, 6.4 and 7.96 for the 2-, 4-, 6- and 8-stage CP, respectively.

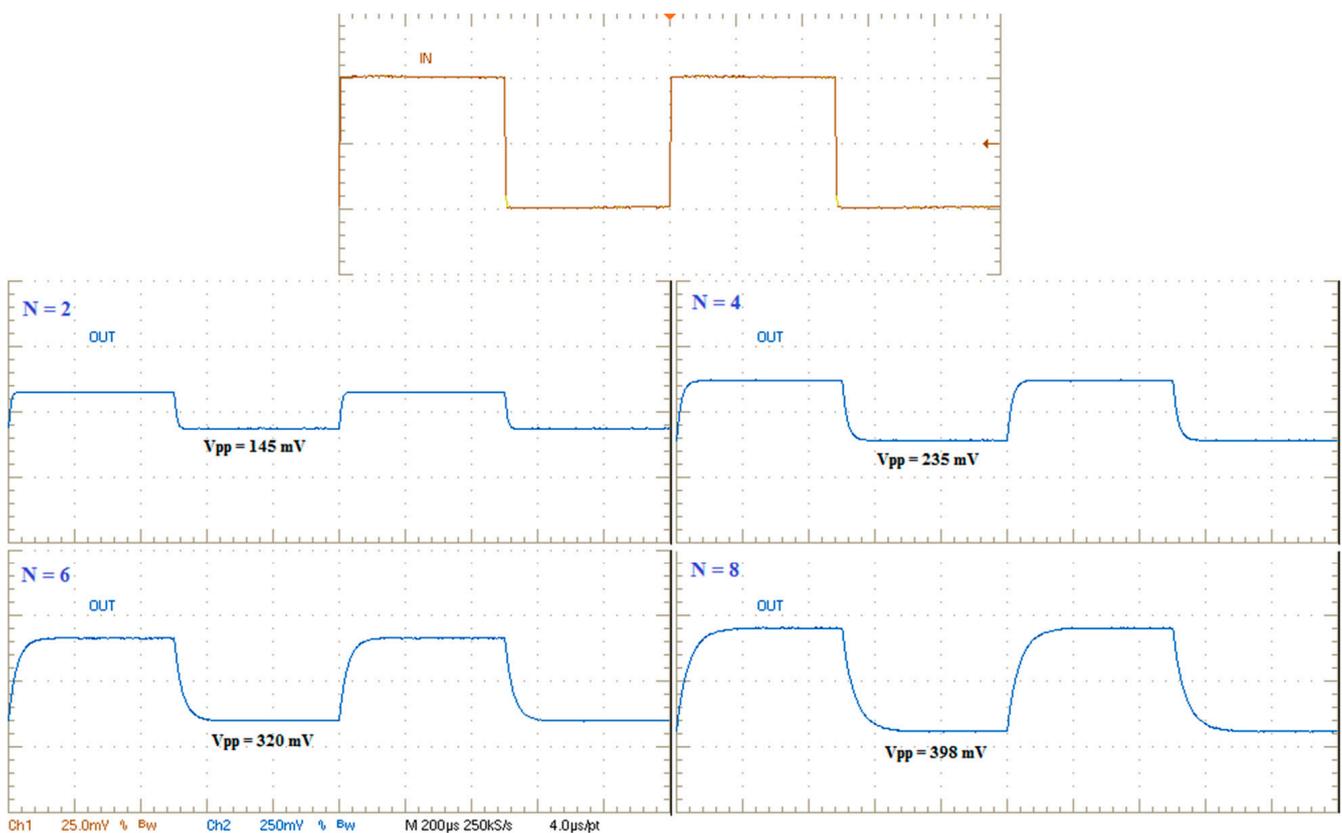
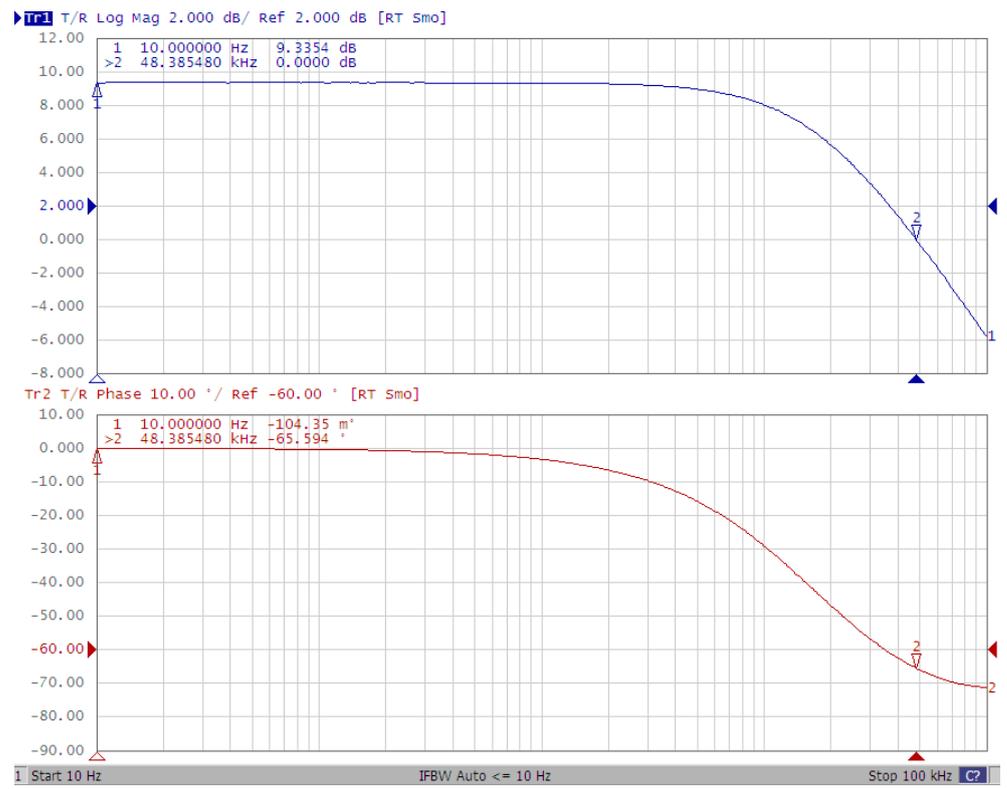


Figure 5. Measured transient responses to a $50 \text{ mV}_{\text{pp}}$ square-wave input signal.

The value of the gain is confirmed in Figure 6, which reports the measured frequency response of the same samples. From this figure it is apparent that the CPs behave like a single-pole system with a GBW equal to 48.38 kHz , 36.32 kHz , 31.81 kHz and 30.27 kHz for the 2-, 4-, 6- and 8-stage CP, respectively.

Table 1 summarizes the transient and frequency response measurement results over 10 samples. As can be verified, the results agree with the analytical prediction with an accuracy error always lower than 14%. The results found are in agreement and further confirm the preliminary experimental results reported in [29], but obtained with an older CMOS technology and for only the case of a voltage gain equal to about 4. In other words, with much more confidence and generality we can confirm the validity of the use of a Dickson CP as signal amplifier and the accuracy of the model derived.

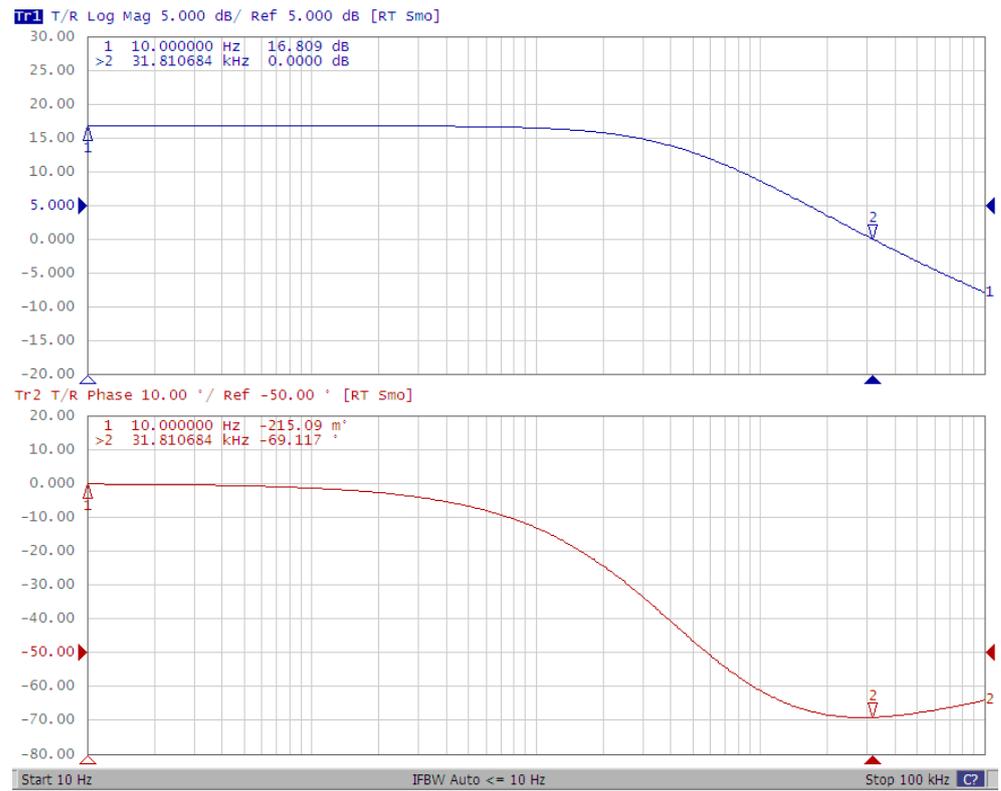


(a)

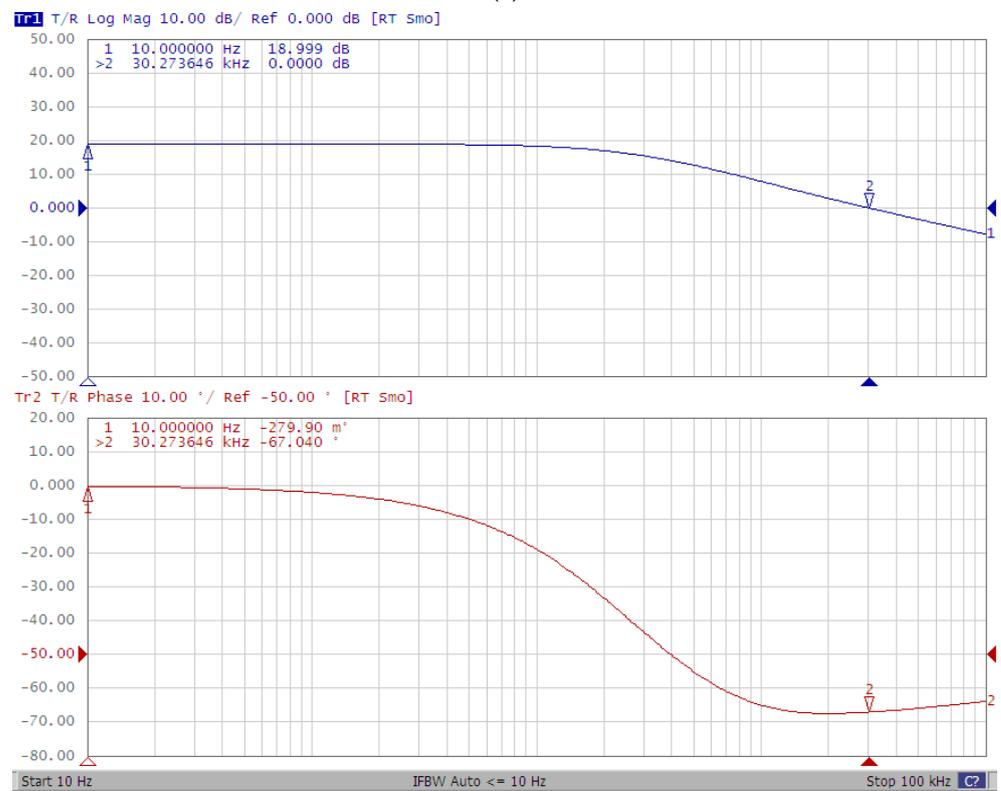


(b)

Figure 6. Cont.



(c)



(d)

Figure 6. Measured frequency response of the CP for $N =$ (a) 2; (b) 4; (c) 6; and (d) 8.

Table 1. Measured charge pumps parameters over 10 samples @ $C_L = 50$ pF.

Parameter	2-Stage CP			4-Stage CP			6-Stage CP			8-Stage CP		
	μ/σ	Model	$\varepsilon_{P2M\%}$									
UGF (kHz)	41.3/1.3	43.5	−5.3	33.6/1.2	34	−1.1	30.3/0.9	29.9	1.5	28.8/0.5	27.2	5.6
DC gain (dB)	9.28/0.07	9.32	−0.4	13.71/0.13	13.71	0.02	16.63/0.14	16.61	0.1	18.81/0.14	18.78	0.2
Settling time ^a (ms)	0.34/0.02	0.31	9.1	0.68/0.03	0.66	3.5	1.14/0.06	1.04	8.5	1.56/0.08	1.47	5.8
SR ^a (V/ms)	15.75/0.19	13.67	13.2	11.26/0.15	10.67	5.2	10.35/0.08	9.38	9.4	9.12/0.11	8.55	6.3

^a Average between positive and negative values; “ $\varepsilon_{P2M\%}$ ”—predicted to average measure relative error (accuracy).

4. Conclusions

This work discusses the use of the Dickson CP as a signal amplifier and explores its time and frequency domain characteristics. The analytical equations and the main design metrics commonly used to evaluate the performance of a conventional amplifier are derived using a simple while accurate equivalent model of the CP working in the slow switching limit. The results obtained through measurements on four CPs, implemented in a 65 nm CMOS technology, confirm the validity of the proposed idea. It is worth noting, however, that the CP cannot be considered as a substitute of conventional amplifiers, but it can be profitably exploited in all those applications where a signal superimposed to a DC component higher than the power supply voltage is required, such as drivers for piezoelectric devices for ultrasound imaging, NMOS LDOs or implanted biomedical devices powered and communicating using single solar cells. Finally, it is worth noting that the proposed model can be extended to other CP topologies which may show an inherent higher GBW but at the cost of lower efficiency and area occupation.

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