

Article

Nanoimprint on Silicon for Opto-Electronic Applications

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Abstract

For the development of a novel optical sensor technology, diffraction grating microstructures were manufactured on a silicon surface. The principle of operation of the sensor technology is based on rotatory encoder technology, developed at Hahn-Schickard. It is based on a convolution of a Gaussian laser beam at a diffraction grating, generating sine and cosine signals resulting from the movement of the diffraction grating. Applying this approach to silicon is new and places technological challenges, which are overcome using a proprietary nanoimprint lithography (NIL) process. The process development, which was done on bulk silicon, is discussed, and its capability of producing operational optical grating microstructures is verified by moving the bulk silicon chips with the grating over an opto-electronic module using a piezo stage in an automated control and data acquisition setup. The noise measured in a 16-bit setup was below 2.8 nm RMS, and the linearity error was 100 nm RMS. Compared to the traveled distance (320 μm), this is less than 350 ppm. Furthermore, the chips with the grating were refined to a MEMS-accelerometer chip by introducing etched spring structures. This setup then was verified using different miniaturized interpolator boards.

Keywords: nanoimprint; lithography; NIL; accelerometer; drift; grating; sensor; optic; interpolator

1. Introduction

The presented optical sensor technology with high signal interpolation capability for an accelerometer is motivated by current limitations of micro-electro-mechanical systems (MEMS) accelerometers. Existing optical technologies generally rely on spectral readout technologies [1–3], which are complex and often associated with high costs of the readout device, or use gratings but are not well interpolatable [4]. Piezoelectric sensors are also common but often use poisonous, expensive materials [5–8] and are only feasible for highly dynamic (10 Hz up to several 10 kHz bandwidth) applications, not for quasi-static signals. The most common approaches in mid- and low-cost static and moderately dynamic (0 Hz up to a few 100 Hz) applications are therefore capacitive or piezoresistive principles for the detection of the inertial mass deflection. This eventually results in a multi-material assembly of the silicon element, resulting in strain due to different coefficients of thermal expansion (C.T.E.), but also strain due to the fabrication processes involved, such as physical vapor deposition (PVD). The introduced strain relaxes over time, resulting in a long-term drift of the sensor element [9,10]. Due to this drift, calibration of the sensor on a regular basis is required for precision measurements.



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To overcome this issue, the proposition of this work is to create an inertial mass in pure silicon, to operate it within the range of its almost perfect elastic properties and, if possible, to reduce the number of different materials and processes involved in order to minimize induced strain. For detecting the deflection of the inertial mass, a technology from an optical encoder was used. This, however, requires the fabrication of optical grating microstructures on a silicon surface. In the final sensor, the grating structures are located directly on the inertial mass and are scanned by a laser with a Gaussian beam profile, generating differential sine and cosine intensity patterns as well as a differential index signal on photodiodes when the inertial mass is deflected. These signals are then processed using an arctan interpolation to achieve motion information with nanometer resolution.

1.1. Principle of Operation of the Accelerometer

The principle of operation, shown in Figure 1, is known from rotary encoders [11,12]. An encoder disk with a diffraction grating on it is scanned with a laser. In the region of the grating the laser is diffracted and deflected towards the photodiodes. In this way, four sine and cosine signals are generated during rotation of the encoder disk, as shown in the upper diagram of Figure 1. After differentiation of PD A and PD A' or, respectively, PD B and PD B' sine and cosine is obtained like shown in the lower diagram.

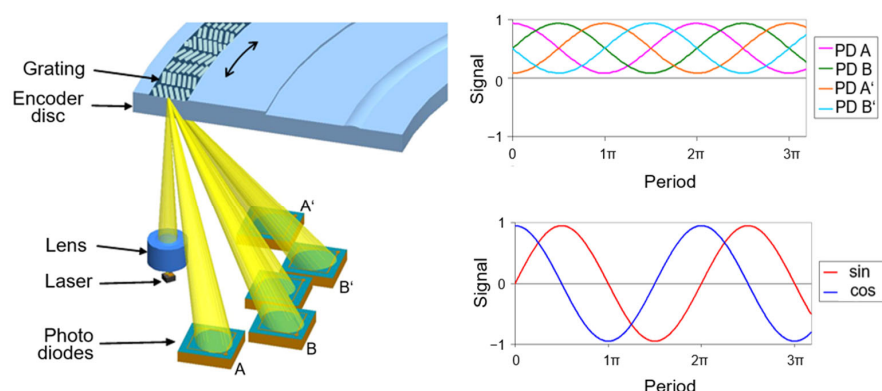


Figure 1. Basic principle of operation of the optical sensor.

The idea is to use this principle of operation and apply it to an optical accelerometer. Figure 2 shows the schematic layout of the accelerometer. An inertial mass is suspended from four springs. On the surface of the inertial mass there is an optical grating. During acceleration, the inertial mass is deflected, and this deflection can be measured using the optical arrangement, as described in the previous section. The unit, comprising the inertial mass, the grating and the springs, is designed as a silicon MEMS element. The fabrication of this MEMS element and the initial commissioning of the accelerometer sensor are described in this work.

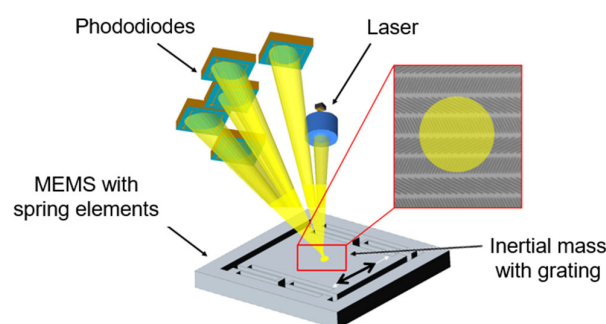


Figure 2. Basic principle of operation of the optical sensor.

Therefore, the grating has to be applied on the inertial mass. The challenges arise from the high precision required for grating fabrication technology and the target of low costs, while simultaneously offering the prospect of benefits such as a substantial reduction in sensor drift and temperature effects without excessive expense. These challenges can be overcome using a NIL process on silicon, which is ideally suited to reduce costs while maintaining the ultra-high precision of the optical grating.

The expected technical specifications are compared with some typical sensors available on the market in Table 1. It shows that the spread in the core parameters of acceleration or vibration sensors on the market is quite large. No sensor addresses the whole market; on the contrary, accelerometers are often tailored to a specific demand or market share. The presented technology is no exception and allows addressing various markets depending on design decisions, and it is expected that its performance is competitive in any market, but the low drift is not always required. Therefore, we decided on a variant where low drift is of interest.

Table 1. Comparison of three possible variants with typical market samples.

Manufacturer	Model	Application	Principle	Meas. Range (g)	Sensitivity	Bandwidth (Hz)	Noise Density ($\mu\text{g}/\sqrt{\text{Hz}}$)	Noise @ Bandwidth (mg RMS)
Measurement Range < 2 g								
2 g Variant		Seismic high Res.	Optical MEMS	2	530,000/g (19-bit/g)	50	0.2 *	0.001 (50 Hz) *
MEMSIC	MXC6232xE/F	Low Cost	Thermal	1.5	512/g (0.5 mg)	1	500	0.5 (1 Hz)
Colibrys	MS1010	Tactical Grade	Capacitive MEMS	2	0.27 V/g	200	30	0.3 (100 Hz)
Sercel	DSU-428	Marine Geophone	Capacitive MEMS	0.5	n/a	800	0.04 (10–200 Hz)	<0.0006 (10–200 Hz)
Measurement Range 2–16 g								
15 g Variant		Industrial Low g	Optical MEMS	15	84,000/g (16-bit/g)	100	0.9 *	0.009 (100 Hz) *
Analog Devices	ADXL363	Low Cost	Capacitive MEMS	$\pm(2/4/8)$	1024/g (2 g)	200	550	Normal Mode 7.7 (200 Hz)
Murata-VTI	SCA3300-D01	Industrial	Capacitive MEMS	$\pm(1.5/3/6)$	2700/g (3 g)	70	37	0.44 (70 Hz)
innalabs	AI-Q-2071	Navigation Grade	Quartz Flexure	15	1.2 to 1.46 mA/g	>300	<2.2 (0–10 Hz) <3.13 (10–500 Hz)	<0.007 (0–10 Hz) <0.07 (10–500 Hz)
Measurement Range > 16 g								
Mid g Variant		Industrial Mid g	Optical MEMS	>100	512/g (9-bit/g)	>5000	28 *	1.9 (5 kHz) *
Bay Sensortec	BST 13C	Crash-Test (Automotive)	Piezoresistive MEMS	500	0.035 mV/V/g	>1000	n/a	n/a
Micronor	MR664	Industrial	Fiber-Optical	40	100 mV/g	1000	<100	<3.2 (1 kHz)
Jewell Instruments	QFA-180	Industrial	Quartz Flexure	30	1.1 to 1.4 mA/g	>300	30	3 (0–10 kHz)

The lines highlighted in green were selected in this project. * according to thermo-mechanical noise of MEMS.

1.2. Nanoimprint Lithography

The demand for miniaturized semiconductor components is constantly rising, are nanoscale structure requirements for new functionalities across all industries [13–16]. These are generally produced by using cost-intensive sequential exposure methods such as electron beam (e-beam) lithography or advanced UV lithography. In comparison, NIL offers a cost-effective alternative to reproduce a certain nanostructure many times, based on high-resolution masters. Therefore, it is not surprising that the market for NIL systems is forecasted to reach USD 54.52 million by 2027 [17]. NIL is used to replicate the surface structure by putting a stamp (master) into a resist. The structure that has emerged from this procedure can be used as a functional unit or etching mask. For the NIL method, two fundamentally different basic process types can be distinguished: UV and thermal NIL [13,18]. UV- NIL has a significant advantage due to short process time and is done at room temperature [13,19]. In this way, large nanostructure areas can be created at wafer level [14,20]. The big disadvantage of the widely used process is the need for a

transparent stamp with high transparency, which is usually produced from quartz by using e-beams [13,21,22]. Therefore, the acquisition of the stamp and the resist processing system are associated with a high investment cost.

NIL processing can be realized by two methods, namely, step-and-repeat or single-step processes [23,24]. The step and repeat approach simplifies the mastering process because the stamp covers one chip or a few chips at once, which lowers the mastering costs. However, it takes more time to stamp the full wafer, and a very precise alignment between the different steps is required. In comparison, the single-step process is fast but needs a stamp with full wafer size. In this case, the mastering is more expensive, and a very advanced NIL process is needed in order to reach a homogeneous replication over the full wafer.

In this paper, we present a low-cost solution for the production of the stamp as well as the transfer of the NIL on silicon substrates. Furthermore, common laboratory equipment along with resistors for commercial use are applied to our experiments. Finally, the ability of the process to produce functional optical grating microstructures is demonstrated through a measurement procedure using process samples, a readout setup including a laser and photodiodes, and a piezo stage for well-defined relative movement of the grating microstructures.

1.3. Microstructure Process Development

The process development of the microstructure on bulk silicon is divided into four steps and is shown schematically in Figure 3.

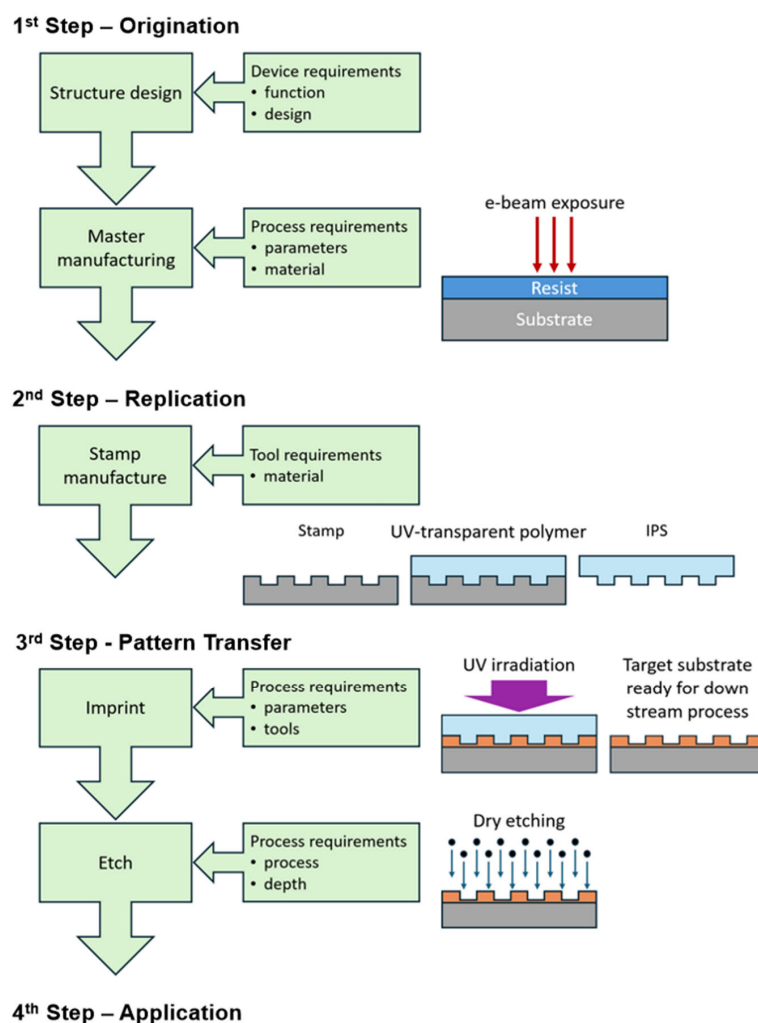


Figure 3. Process development of microstructure.

The first step, called ‘Origination’, includes the nanostructure design and the master-ing process. As explained, it is required that the microstructure contain a special grating structure with 4 different zones with submicrometer sizes. Each zone has a specific grating orientation, while the grating constant is the same, in particular, 1.6 μm , due to the wavelength of the laser (850 nm). The 4 zones are repeated every 40 μm . The optimum diffraction efficiency is typically achieved at $\lambda/4$, which corresponds to roughly 212 nm. The first manufacturing step is made by suitable lithography (laser or e-beam; Figure 2). Typically, for structure sizes down to about 500 nm, laser beam recording is preferred due to lower costs; however, for real nanostructures below 500 nm, either a high NA laser or even electron beam recording is required.

The second step, called ‘Replication’, describes the manufacturing of an Intermediate Polymer Stamp (IPS[®]), a wording that is protected under trademark and patent law by the Swedish nanotechnology company Obducat AB (Lund, Sweden). First, a curable polymer material (such as PDMS, UV-curable resins, or OrmoStamp) is dispensed over the master. The polymer is cured using heat or UV light and then gently peeled away from the master. This flexible or intermediate polymer stamp now contains the exact inverse (negative) features of the master.

The third step, called ‘Pattern Transfer’, is related to the process that transfers the micro/nano structure from the polymer stamp to the final target, for example, a silicon wafer. First, the stamp is touched down on the NIL resist. Then, UV light or thermal treatment is used to cure the resist, and the stamp is removed, and the process can be repeated on the same wafer or, for a full wafer stamp, on a freshly coated wafer. Finally, a dry etching process is needed to transfer the structure into the target wafer. Further optimization of the transfer process is possible by simultaneous thermal and UV treatment [25,26].

The last step is the final ‘Application’ of the micro/nano structure.

2. Materials and Methods

2.1. Materials

OrmoStamp[®] from micro resist technology (Berlin, Germany) was used to manufacture the nanostamp. The material properties after curing are similar to glass, and therefore it is a cost-efficient alternative solution to quartz-based stamps. The UV photoresist mr-NIL200 (micro resist technology) was used for pattern transfer, as well as a non-stick coating (1H, 1H, 2H, 2H-perfluorooctyltrichlorosilanes) for easier separation of the stamp and the photoresist after curing.

2.2. Manufacturing of the Microstructure

The manufacturing of the microstructures is described in the following sections.

2.2.1. Step “Origination”

The nanostructured surface, which serves as the basis for the acceleration sensor, has a size of $3 \times 3 \text{ mm}^2$, a period length of 40 μm , a grating constant of 1.6 μm and a grating height of 212 nm, as shown in Figure 4. Panel (a) shows the entire wafer and panel (b) shows the magnified grating using an electron beam microscope.

To produce the micro-optical elements, a silicon wafer was coated with an 800 nm thick resist layer (AZ-MIR701), including Ti Prime as an adhesion promoter, and exposed using laser lithography by an external partner. The laser intensity plays a crucial role in the formation of the structure. The difficulty here was to expose the full depth of the resist with the focused laser beam. In the case that the resist was not completely exposed, after development, residues of the resist are visible between the grating walls.

A series of tests was performed to determine the correct exposure parameters. In the first series of tests, the structure was exposed to an intensity between 60, 70 and 80 mJ/cm². As can be seen in Figure 5, there remained residues from resist between the trenches of the structure. Therefore, the intensity was further increased.

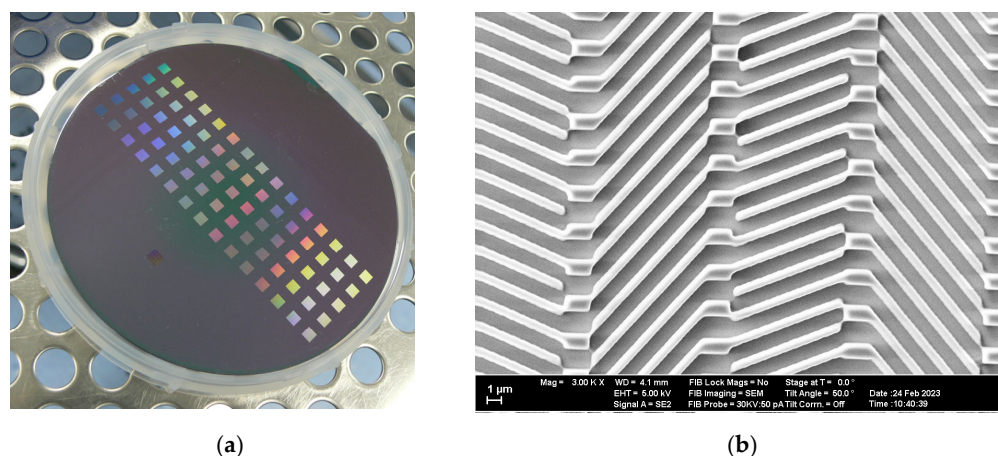


Figure 4. Wafer and grating with different magnifications: (a) wafer with grating; (b) grating magnified by an electron beam microscope.

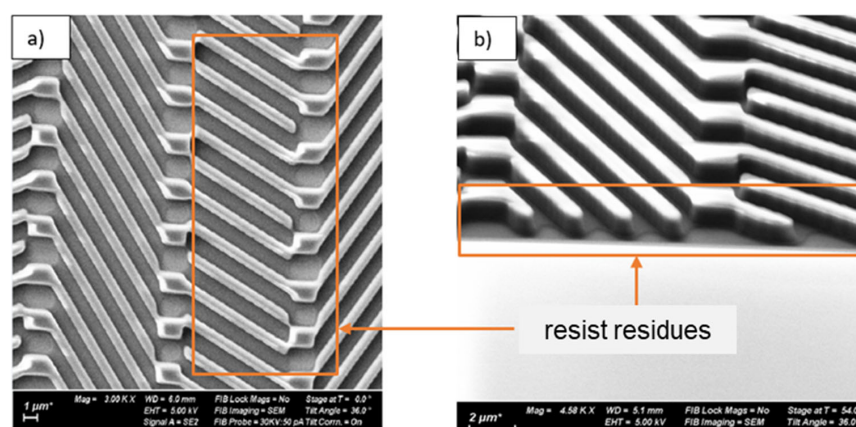


Figure 5. Influence of exposure intensity at 80 mJ/cm²; (a) top view of the structure at 80 mJ/cm²; (b) front view of the structure at 80 mJ/cm².

A complete exposure was achieved at 90, 100 and 110 mJ/cm² at which no more residues from resist could be found (Figure 6). It was also observed that the geometry of the structure changed with increasing intensity. The walls became thinner with increasing exposure intensity. This change in exposure width and depth with increasing dose is well known from optical lithography, as shown, for example, in reference [18].

In order to replicate a stamp from a given structure, the pattern was exposed at 90 mJ/cm² and etched into the wafer using the reactive ion-beam etching (RIE) process. Figure 7 shows the result of the etched microstructure. In method (a) a bare silicon wafer was used, which had a grating height of approx. 140 nm after the etching process. Obviously, this is quite far away from the target of about 212 nm. Here, it has to be taken into consideration that in many cases the resist has a higher etching rate than silicon. As a consequence, a rough surface can be seen between the trenches of the structure. In method (b), a 211.5 nm thick oxide layer was applied on the bare silicon wafer before lithography, which served as an etching stopper to secure the required etching depth. After etching, a grating height of approx. 233 nm was achieved. In comparison to method (a), a smooth surface by applying an oxide layer was achieved between the trenches after etching of resist and can be seen on top of the

embossed structure. Nevertheless, the function for the application is given, as the process does not generate an image but four separate signals for the arctan interpolation.

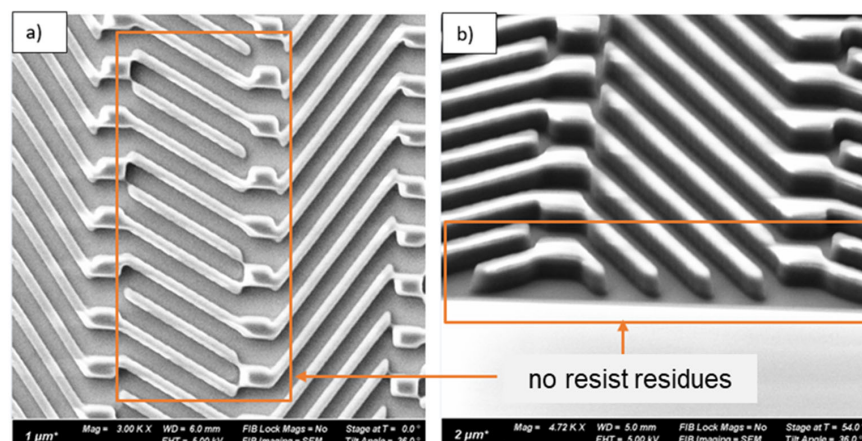


Figure 6. Influence of exposure intensity at $100 \text{ mJ}/\text{cm}^2$; (a) top view of the structure at $100 \text{ mJ}/\text{cm}^2$; (b) front view of the structure at $100 \text{ mJ}/\text{cm}^2$.

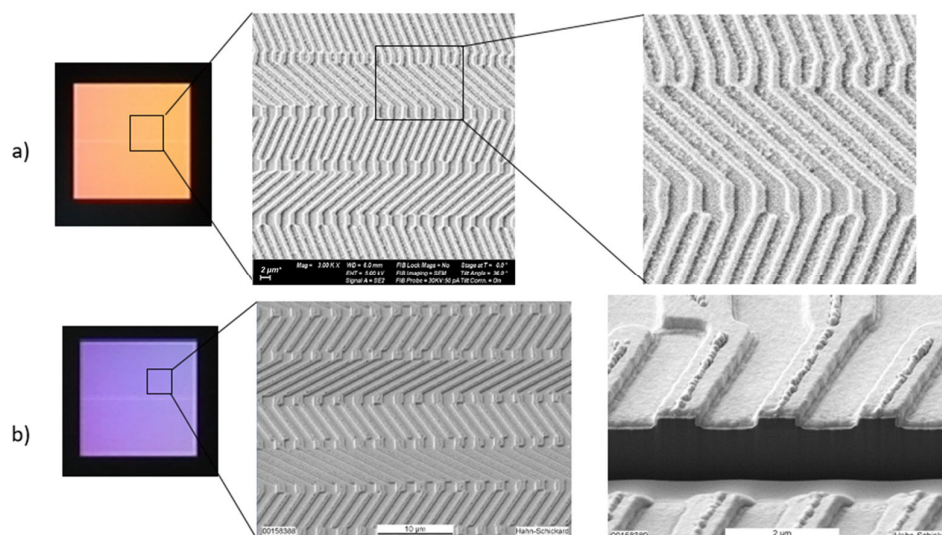


Figure 7. Etched microstructure: (a) on bare silicon wafer; (b) a deposited 211.5 nm thick oxide layer on bare silicon wafer in comparison.

2.2.2. Step “Replication”

The structured silicon wafer (method (b)) was used as a master for stamp production. Therefore, materials from the company micro resist technology were used. On the one hand, OrmoStamp, which has glass-like material properties after curing as explained before, was used. On the other hand, the UV photoresist mr-NIL200, which serves as an etching mask for the structure transfer and does not require an adhesion promoter, was applied. For easy separation between the photoresist and the stamp, the stamp was coated with a non-stick layer before the process. Initial tests of nanostructure production were carried out manually with the aid of a microscope and UV light source. In further procedures, a Fineplacer from Finetech ($5 \mu\text{m}$ placement accuracy) was used with an additional UV light source for the NIL process. This is particularly suitable for a parallel plate process (pressing the components between the plates). When attached to the placement head, the stamp can be used to structure the entire surface by simply moving it (step and repeat). The process development of the stamp is shown schematically in Figure 8. First of all, the structured

substrate surface is applied with a non-stick coating. After drying, 0.01 g of OrmoStamp is applied to the center of the $3 \times 3 \text{ mm}^2$ surface. A Pyrex substrate ($5 \times 5 \text{ mm}^2$) is placed on the top and pressed down lightly to avoid air pockets. After waiting for a few minutes until the liquid had spread, the varnish was cured under UV for 20 s (395 nm LED) at a distance of approx. 2 cm from the LED. The two parts are then separated from each other. Instead of a Pyrex substrate, it is also possible to use any other transparent substrates. It is also possible to create a substrate from OrmoStamp.

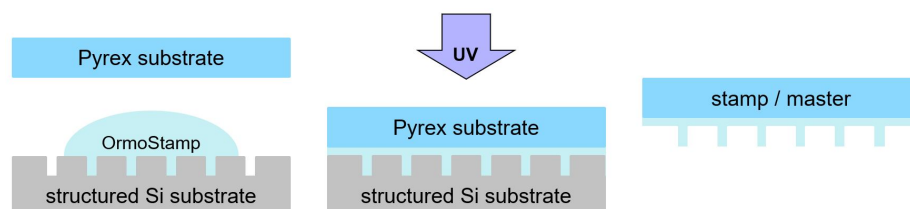


Figure 8. Stamp production process.

Figure 9 shows the finished single stamp (master) with which the structure can be replicated.

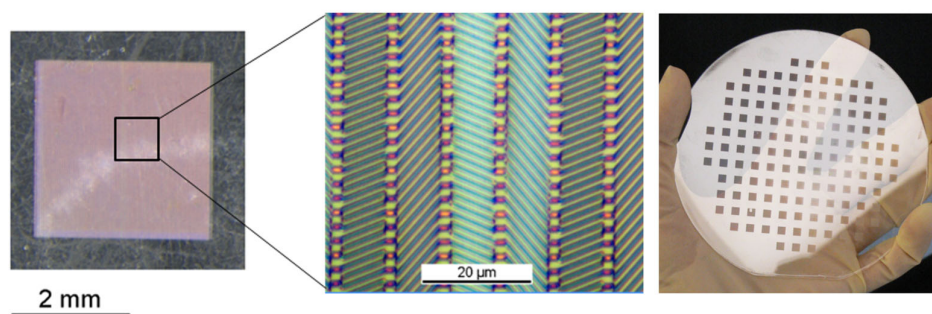


Figure 9. Finished stamp on the left side; zoomed in the middle; finished wafer stamp on the right.

It was also possible to create a stamp for the whole wafer, shown also in Figure 9. The advantage is that multiple structures can be produced at the same time. Furthermore, the process is time-saving and results in higher yield, which leads to cost reduction in processing.

2.2.3. Step “Pattern Transfer”

The structure can be reproduced on the target wafer with the manufactured stamp. The structure transfer works in the same way as the production of the stamp and is shown in Figure 10. The cleaned $5 \times 5 \text{ mm}^2$ silicon substrate is coated with 0.01 g of photoresist (mr-NIL200) and pre-baked at 60°C for 3 min (hotplate). The master was placed on top, pressed down with 10 N and cured for 20 s using a UV lamp.

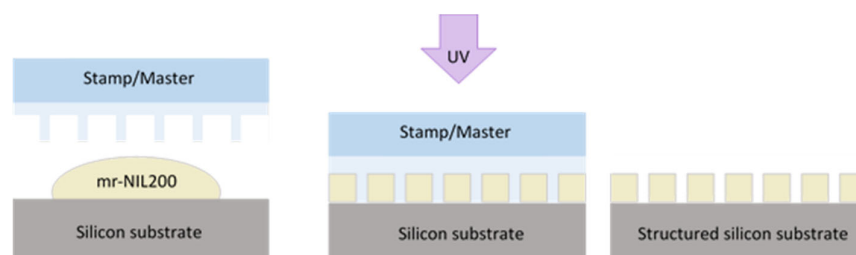


Figure 10. Process of pattern transfer.

Further, the structure was applied on a silicon wafer using a lithography process and dry etching according to the pattern transfer described above. For first functional testing, the wafer was then sputtered with gold to increase the reflectivity of the structure. However, for future applications, the silicon wafer with grating structure should not be coated, as the intention was to use pure silicon.

After optimization of the particular NIL process on dummy wafers, the grating structure was used to create a single-axis acceleration sensor using a spring-loaded inertial mass. During construction, attention was paid in particular to large deflection, linearity and practicability. Figure 11a shows two versions of the spring-loaded inertial mass with the same deflection (20 g) and different lengths of the springs, as can be seen on the right side in the figure. The springs of the upper variant are 2.5 mm long and have a cross-section of $15\ \mu\text{m} \times 300\ \mu\text{m}$. The springs of the second variant have a length of 3.7 mm instead. The first variant is designed for the high single-digit g-range, and the second variant for the low single-digit g-range.

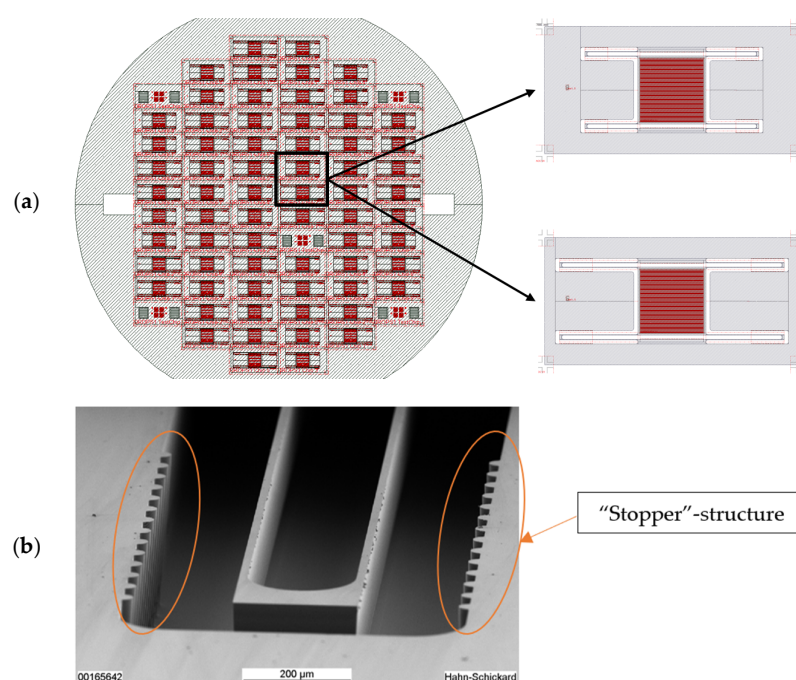


Figure 11. (a) Layout of the spring-mass system with two versions; (b) stopper structure prevents the system from sticking together.

In addition, a “stopper” structure (panel (b)) has been added to the construction to prevent the system from sticking together in case of a large shock.

It should be noted, that the manufacturing of the sensor device requires two lithography and etching steps. The first step is needed to create the precise grating structure, as explained above, whereas the second step is needed to create the MEMS structure.

Before applying resist on the wafer, gold coating had to be removed from the unstructured areas. This step is crucial for dicing chips with a Stealth Dicer. A common wafer saw would flush the particles over the surface, which could stick to the diffractive patterns and could not be removed by cleaning. A Stealth Dicer, however, uses a laser to create local microcracks in the silicon wafer. The laser treatment creates a targeted modification of the silicon crystal along desired, straight fracture lines so that the wafer breaks into exact rectangles through lateral expansion. No particles are produced, and the diffractive structures remain largely particle-free. Figure 12 shows the finished silicon chip as well as some common defects that occurred after etching.

In particular, the chips on the edge of the wafer (panel (a)) were not completely etched through. Other chips, however, were destroyed by the etching process so that the springs were not present (panel (b)) or were broken during the dicing process (panel (c)). Nevertheless, some chips met the requirements and were used for measurements (panel (d)). It is expected that the overall yield can be increased through further optimization of the design and process. The yield data are not very meaningful, as the project was merely a feasibility study involving small quantities (13 units with a yield of <30%).

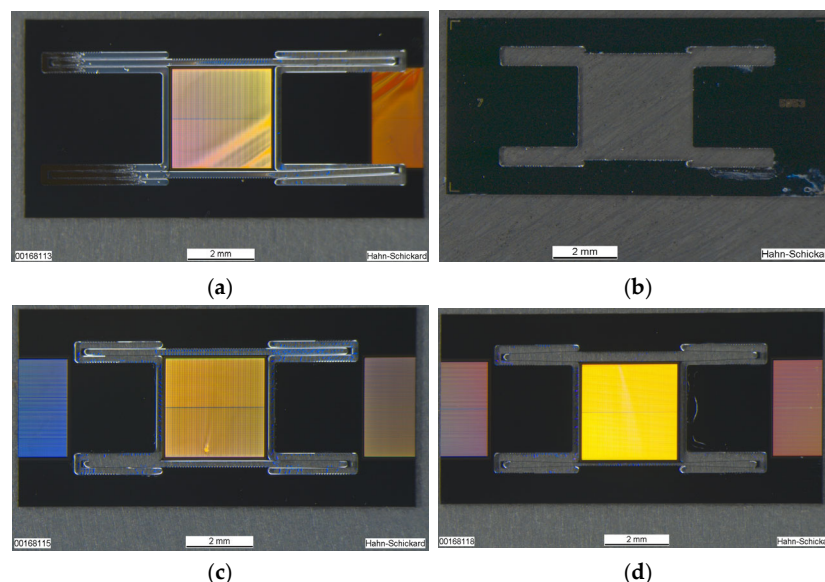


Figure 12. Common defects that occurred by the etching process: (a) structure not etched fully through; (b) springs etched away; (c) broken springs; (d) intact spring structure.

2.3. Materials and Methods for Proof of Concept

To demonstrate that the microstructures are suitable for the target application, samples of the manufactured microstructures in bulk silicon were attached to the bottom of a piezo stage using a gel pad mounting, as depicted in Figure 13.

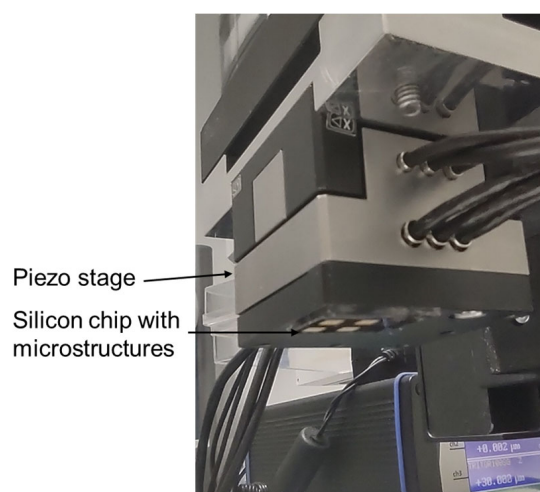


Figure 13. Test setup to verify the suitability of the microstructures.

The z-distance to the optical module containing a vertical cavity surface-emitting laser (VCSEL) with a lens and photodiodes with transimpedance amplifiers was adjusted based on maximization of the signal amplitude. In addition, the x-y position of the chip was adjusted so that the index mark (ref) lay within the range of motion of the piezo actuator.

Subsequently, the piezo stage was moved over a total displacement of 80 μm in 250 nm steps via software control and the photodiode signals were recorded automatically. Finally, the signals were interpolated using a numerical software analysis script.

3. Results

The previously mentioned analysis script was used to create diagrams and generate numeric output for several key numbers, which will be discussed in this section.

3.1. Raw Signals

Figure 14 shows the raw signals (sine, cosine and reference signals) provided by the optical module during the movement of the microstructures relative to the laser spot.

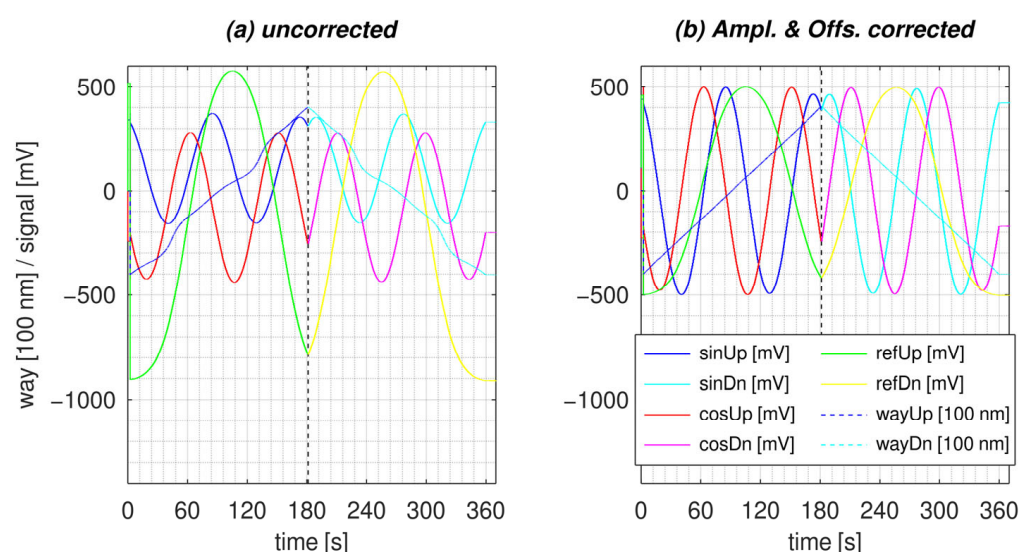


Figure 14. Amplitude and offset correction of signals and interpolation.

First the microstructures move forward (Up), then in the middle of the diagram the motion is reversed (down/'Dn'). The interpolated way, as obtained from the raw signals, is also plotted, visible as a delta-shaped curve. Presumably due to angular misalignment in the three degrees of freedom resulting from the mounting of the gel pad, the signal amplitudes at the photodiodes were unequal. This led to inaccuracies in the ATAN2-interpolation method, causing a waved curve for the measured displacement instead of a straight line. This is shown in the left graph of Figure 14. As the distortion is symmetrical during forward and backward movement, an inaccuracy of the position or movement of the actuator is improbable. In a first measurement attempt, there had been friction between a part of the optical module and the chip with the gratings, which resulted in unsymmetrical errors. However, in this first attempt, the amplitudes of the signals were quite similar, which points to an alignment problem in the subsequent measurements.

3.2. Signal Corrections

By applying amplitude and offset correction, as would be done in any interpolation circuit or microcontroller [27], these inaccuracies could be significantly reduced, as can be seen in the right graph of Figure 14. As expected, the measured displacement now yields a nearly linear characteristic curve. The noise in this setup was in the range of 3.6 nm, and the non-linearity amounted to approximately $\pm 0.3 \mu\text{m}$ following the amplitude and offset correction.

3.3. Further Improvements

Before and after the corrections, the interpolated curve did not show any local extrema, which makes it unambiguous and well-suited for application of a polynomial or harmonic linearization curve-fitting equation in the interpolation circuit or microcontroller. It is expected that this will reduce nonlinearity to values close to the noise level. Furthermore, electronic noise can be significantly reduced by applying a high-quality 24-bit Analog–Digital Converter (ADC), instead of the 16-bit system employed in the last measurements. Also, a mechanically stiffer setup can reduce mechanical vibrations/noise between the optical module and chip. The according measurement results are shown in Figure 15. Here, the measured distance was twice as large as in Figure 14. It was started at the reference mark, then traveled 160 μm ('Up'), then the motion was reversed, traveling 320 μm ('Dn'), and finally 160 μm up back to the reference mark. Offset- and amplitude-corrected signals were plotted together with the interpolated signal (diagonal lines).

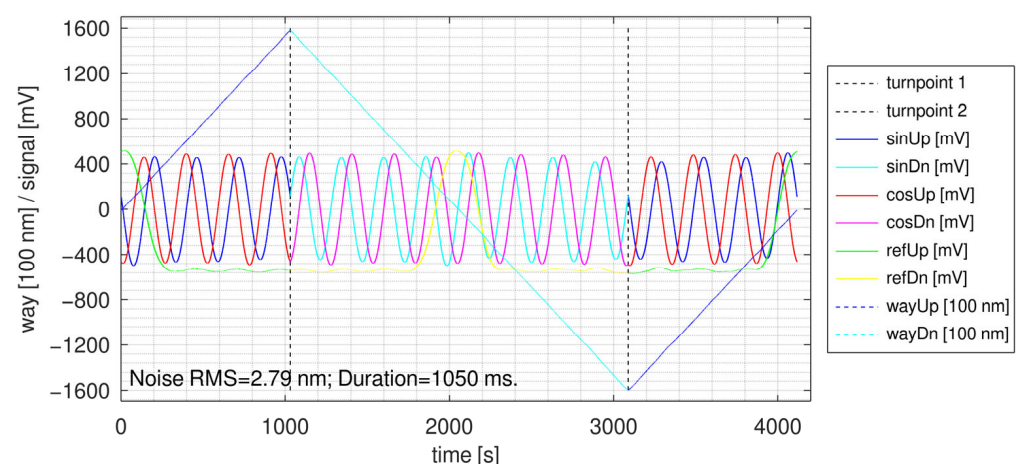


Figure 15. Measurement using the 2nd setup; note the RMS noise of <2.8 nm during >1 s.

To illustrate the possibilities for further signal improvement via software, Figure 16 shows the effect of a harmonic linearization approach. The graph shows the linearity error of the raw signal determined by subtracting a straight line from the measured and ATAN2-interpolated data after offset and amplitude correction (Uncorr.). Also shown are the determined fit function (Fit) and the result of correcting the input data using this fit (Corr.). Tests have shown that harmonic fitting generates superior results compared to polynomial fitting of the same data (polynomial fitting is not shown here). However, it is possible that a look-up table combined with linear or spline interpolation of the primarily ATAN2-interpolated data might achieve even better results. Harmonic fitting was adapted because of the harmonic nature of the linearity error and its reasons in distortions of the sine and cosine signals. The harmonic fit works by transforming the data into the frequency space using a fast Fourier transform (FFT) as available in the ARM “Cortex M Software Interface Standard” (CMSIS) “Digital Signal-Processing” (DSP) Library, hardware accelerated and optimized for Cortex M4 and more recent microcontroller architectures. Subsequently, the required harmonics are inverse-transformed and scaled into wave signal space, so that the wavy input wave is distorted by the harmonic function (a linear combination of phase-shifted cosine functions with adjusted frequency and amplitude) and thus corrected. The approach becomes efficient by only using the necessary harmonics, similar to the well-known JPEG image compression algorithm. Further improvements at the harmonic fit might be possible when using a suitable windowing function. The fit was included in the microcontroller software and performed well over several measurements. However, no statistical data were obtained, as the fit was merely intended as a proof of concept, showing

that significant improvements of the linearity are possible by means of software because of the sensor's reproducible behavior.

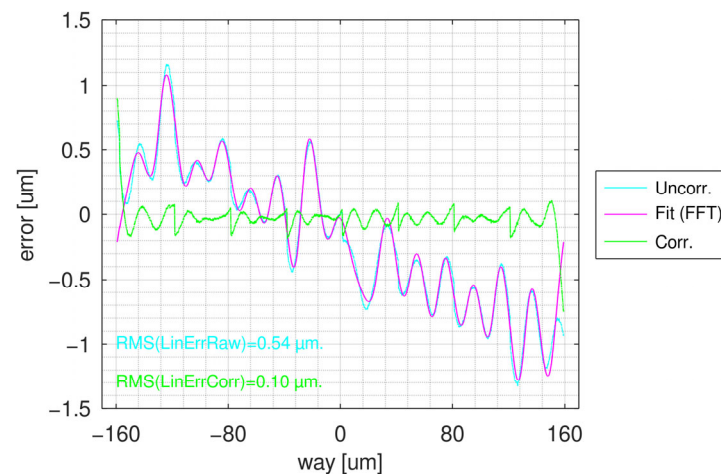


Figure 16. Linearity error of measurement above, corrected by harmonic fit to RMS of 100 nm (still using 16-bit ADC).

3.4. Results of Improved Setup

As can be seen in previous figures, the noise was reduced to less than 2.8 nm RMS, and the linearity error (still using the same 16-bit ADC) was reduced to 100 nm RMS. In total, about 10 tests of the RMS were carried out, always as part of one of the other measurements. The standard deviation was in the range of 1.7 to 2.3 nm RMS. When compared to the movement of 320 μm , this is less than 350 ppm. In reality, the movement for the accelerometer will be smaller than that, which will reduce the requirements for the fit, probably improving this number further.

3.5. Accelerometer Setup and First Evaluation

In a next step, the silicon chips with springs etched into the bulk silicon to form an inertial mass, while the gratings were located on the surface of the inertial mass itself, were tested. After packaging the passive silicon accelerometer element with the optical module in a very stiff casing (see Figure 17) featuring steel with a very low coefficient of thermal expansion, the displacement of the inertial mass can be detected optically.

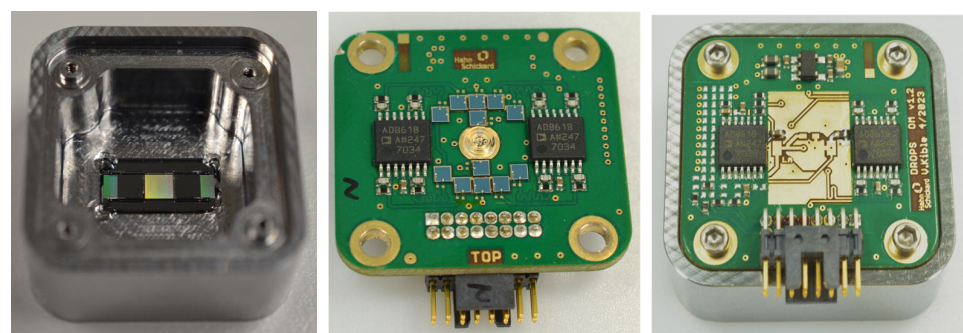


Figure 17. Accelerometer based on MEMS and readout by optical module PCB (from left to right: casing with inertial mass; read head with laser diode, lens and photodiodes; assembled demonstrator).

The conversion of the raw analog signals to displacement data is done in an interpolator module (IPM) using an algorithm based on amplitude and offset correction, ATAN2 interpolation, and a harmonic correction function in the Soft-IPM. Several PCBs (Printed

Circuit Board) of the IPM were built. The IPM can be stacked on top of the optical module but can also be cable-connected if feasible.

This accelerometer technology was expected to have excellent long-term drift characteristics, as both the mechanical stresses caused by different materials and their respective coefficients of thermal expansion and the number of required manufacturing steps have been reduced to an absolute minimum. These two factors are considered the primary causes of long-term drift in current silicon-based accelerometers that rely on capacitive sensing principles.

However, in the first long-term measurement to demonstrate this behavior under constant acceleration using the Soft-IPM, a time-delayed and low-pass-filtered effect of changing air humidity on the experimental setup was observed (Figure 18); this problem could be solved using a hermetically sealed case. Currently, the optical module PCB is mounted onto the (open) case with an air gap of about 0.3 mm, which exposes inner parts to ambient conditions. Displayed in this graph, there are simultaneously measured curves for relative humidity at the Device under Test (DUT) sensor, DUT temperature and the DUT output signal amplified by 10. Changes in humidity can possibly either affect the adhesive used for attaching the die to the case or the optical module PCB itself by absorbing humidity and swelling and thus changing the output signals.

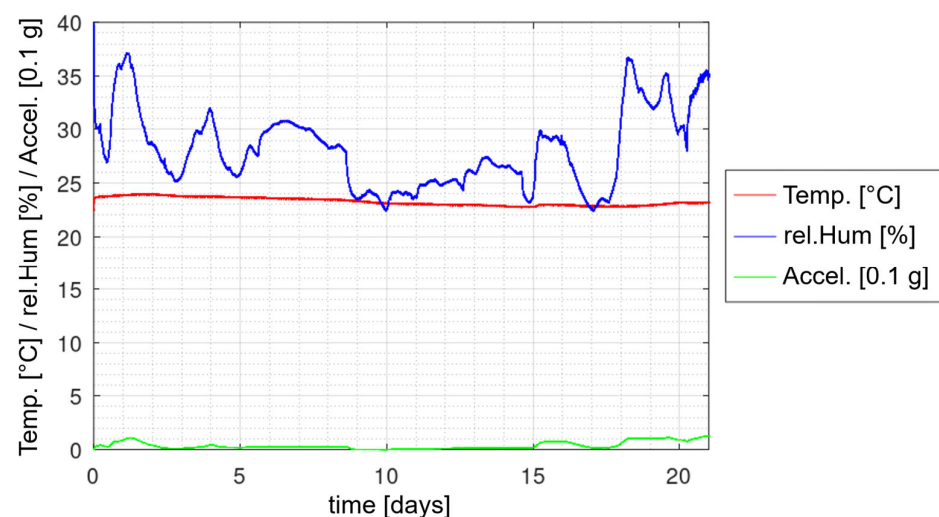


Figure 18. Normalized measured signals of a long-term test over 21 days: red/temperature, blue/rel. humidity, green/acceleration $\times 10$ (sensor signal).

According to the measured data, there was a clear correlation between the change in humidity and the changes in the sensor response. Temperature and humidity control usually needs a climate chamber using a fan and pumps, which are sources of vibration and will therefore distort the results. A solution to test the sensor in a climate chamber while it is fixed on a massive granite table under the climate chamber is planned for the future to investigate the correlation between drift, humidity and temperature.

4. Discussion

Overall, the developed NIL process proved highly suitable for fabricating optical gratings for the application in the accelerometers. This was verified by measurements performed on a piezo stage, in which the grating was displaced relative to an optical module comprising a laser diode, lens, photodiodes, and transimpedance amplifiers.

The inaccuracies observed during the measurements are presumably attributable primarily to the measurement setup itself and only to a minor extent to contamination of the NIL structures on the chip.

While it is possible that uneven roughness within the cavities caused by etching artifacts or photoresist residues on top of the etched bosses might additionally modulate the signal amplitude, these effects should mainly occur when distances are significantly greater than 80 μm but can be significantly reduced or eliminated by further improvements in the process steps after the NIL itself. For example, optimized photoresist removal can eliminate residues from the cavity areas, and a silicon-on-insulator (SOI) process can reduce roughness within the cavities, although both measures would likely increase the cost of the silicon chip.

In the next step, the silicon chips were modified by etching folded springs into the silicon substrate to form the inertial mass, while the gratings were positioned on the surface of the inertial mass itself. The etching process itself was unstable, resulting in varying thicknesses of the springs, which is a drawback for the measurement accuracy of the demonstrator. The parameters selected for the etching process were not ideal for reproducibly manufacturing springs with precise geometric dimensions, and the yield was too low. For further investigations, the etching process must be improved to enhance the yield and quality of the springs. Moreover, in their current design, the springs are unstable and therefore fragile. Nevertheless, the deflection of the inertial mass could be optically detected after the passive silicon acceleration sensor element had been assembled with the optical module.

The expected excellent long-term drift characteristics for this accelerometer technology could not yet be proven. One possible explanation could be the influence of moisture, a hypothesis that requires verification through further investigation. Another observation was that the power supply PCB heats up significantly during operation ($>60\text{ }^{\circ}\text{C}$). In this case, the electrical circuit must be optimized through the use of different components so that no heat is conducted into the sensor. Potential countermeasures for future measurements include also controlling environmental conditions within a climate chamber or using a hermetically sealed housing.

In any case, more acceleration sensors need to be manufactured, and further measurements and investigations need to be done for a better understanding of the behavior of the presented sensor technology. Furthermore, the key specifications of the acceleration sensor must be verified, such as the measurement range, linearity range, resonant frequency, shock resistance, and behavior of the sensor at various temperatures. It was no longer possible to determine these parameters within the scope of this project.

5. Summary and Outlook

This article presents a novel technology for optical accelerometers using the excellent properties of pure silicon and offers high signal interpolation capabilities. The main component of the sensor is a silicon-based inertial mass suspended on springs, the deflection of which is read out by means of a laser via an optical module. The grating located on the inertial mass was fabricated using a NIL process combined with an additional etching step. The manufacturing process for the inertial mass is also described in this work.

A demonstrator was designed and built, and the first measurements were performed. The results of the measurements verify the optical readout principle and demonstrate the great potential of this approach. The position of the inertial mass can be detected with high precision; however, the long-term measurement for proving the low drift behavior of the demonstrator shows some cross-sensitivity. The assumption is that this could be induced by the adhesive for attaching the initial mass under the influence of humidity. Further research is required in the future for a better understanding of this behavior. In addition, the key specifications of the acceleration sensor must be verified, and further sensors need to be manufactured to obtain statistical data of the measurements.

Also, the NIL and etching processes should be improved to enhance the precision of the grating, the inertial mass, and the springs and, in this way, generate more accurate measurement results. Furthermore, for reducing the overall size and cost, it is intended to modify the MEMS springs to a more compact meander-type design. This will eventually lead to accelerometers with low long-term drift in the near future.

Due to the simple design of the optical acceleration sensor technology, based on a printed circuit board as an optical module, low manufacturing costs can be expected after industrial implementation, so this concept could also be interesting for other sensor applications where relative motion needs to be measured, such as linear measuring scales or distance sensors.

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