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Silicon Nitride Interface Engineering for Fermi Level Depinning and Realization of Dopant-Free MOSFETs

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Abstract: Problems with doping in nanoscale devices or low temperature applications are widely known. Our approach to replace the degenerate doping in source/drain (S/D)-contacts is silicon nitride interface engineering. We measured Schottky diodes and MOSFETs with very thin silicon nitride layers in between silicon and metal. Al/SiN/*p*-Si diodes show Fermi level depinning with increasing SiN thickness. The diode fabricated with rapid thermal nitridation at 900 °C reaches the theoretical value of the Schottky barrier to the conduction band $\Phi_{SB,n} = 0.2$ eV. As a result, the contact resistivity decreases and the ambipolar behavior can be suppressed. Schottky barrier MOSFETs with depinned S/D-contacts consisting of a thin silicon nitride layer and contact metals with different work functions are fabricated to demonstrate unipolar behavior. We presented *n*-type behavior with Al and *p*-type behavior with Co on samples which only distinguish by the contact metal. Thus, the thermally grown SiN layers are a useful method suppress Fermi level pinning and enable reconfigurable contacts by choosing an appropriate metal.

Keywords: Schottky barrier lowering; Fermi level depinning; dopant alternative; interface engineering

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1. Introduction

The ability to modify the conductivity of semiconductors with impurity doping is one of the central ingredients of modern complementary metal-oxide-semiconductor (CMOS) technology enabling electron, as well as hole conduction, p-n-junctions, bi-polar, and field-effect transistors (FETs). However, in today's deep nanoscale MOSFETs even at very high dopant concentrations only a few dopants reside in typical source/drain contact volumes resulting in strong variability of the electrical device characteristics [1]. Furthermore, the nanoscale size leads to an increase in the ionization energy of dopants due to a dielectric mismatch [2–4], as well as dielectric and quantum confinement effects [5,6]. In turn, this yields increasing parasitic source/drain resistances with decreasing spatial dimensions of devices. Although a mere replacement of doped regions with metals appears attractive, the Schottky barrier that forms at metal-semiconductor contacts due to Fermi level pinning severely impacts the electrical behavior of FETs: So-called Schottky barrier devices exhibit a deteriorated off-state with impaired switching and high leakage, as well as a lower on-state performance compared to conventional FETs with doped source/drain electrodes. As a result, alternatives to impurity doping are much sought-after.

A promising approach to replace impurity doping with metals is to reduce the impact of the Schottky barrier by depinning the Fermi level. This can be accomplished by inserting an ultrathin insulator in-between the metal and the semiconductor [1,7–10]. This interlayer strongly reduces the density of so-called metal-induced gap states (MIGS) that are the main reason for Fermi level pinning [11–13]. In addition, the dangling bonds at the silicon surface are saturated with the interlayer material [14,15]. In addition, when bringing two materials in contact, physical changes, e.g., mechanical stress or change of micro hardness can appear in each material due to the formation of a contact layer [16,17]. However,

mechanical stress of the contact metal in use (Al) is small for our measurement conditions at room temperature. Because of that, these effects are not explained in more detail. In contrast, metallurgical reactions [18] are considered as they change the electrical behavior of the semiconductor device.

Ultrathin Si_3N_4 layers grown with rapid thermal nitridation (RTN) are a promising interlayer material because of their fabrication and material properties. On the one hand, the nitridation of silicon surfaces can be carried out at uncritical process temperatures as a chemical reaction between silicon and NH_3 already starts to occur at 100 K [19]. The growth of silicon nitride (SiN) layers with a temperature dependent self-limiting process gives the advantage of very high tunability and reproducibility of the silicon nitride layer thickness between 0.8 nm and 2 nm. Since, the silicon nitride surfaces act as a diffusion barrier that helps to prevent further unintended oxidation of the silicon surface the reproducibility of subsequent fabrication steps is improved as well. On the other hand, the SiN band gap is large enough to block MIGS and in addition has a moderate potential barrier of approximately 2 eV with respect to the silicon conduction and valence band which enables a high tunnel probability into each [20] and the flexibility to choose *n*- or *p*-type behavior independent of the interlayer material. In recent works, dopant-free ohmic contacts and *p*- or *n*-like switching behavior of Schottky barrier MOSFETs (SB-MOSFETs) were observed by using thermally grown silicon nitride [9,21,22]. By depinning the Fermi level with a 0.8 nm SiN layer different metal work functions were used to show unipolar *n*- and *p*-like switching behavior and ohmic current behavior [22].

In the present publication, we study the Schottky barrier height of Al/SiN/*p*-Si contacts modification with different SiN interlayers. Furthermore, we show the impact of this interface engineering towards the switching behavior of pseudo and top gate MOSFETs with metals with high and low work function in order to realize *n*- and *p*-type switching behavior with the same interlayer.

1.1. Metal-Semiconductor Contacts

Schottky barriers at a metal-semiconductor interface strongly deteriorate the electrical behavior of SB-MOSFETs as they cause high contact resistances and ambipolar switching behavior. In literature, there has been a long debate whether unsaturated dangling bonds and defects at the silicon surface or the MIGS are responsible for Fermi level pinning [21,23–27]. The current understanding is that MIGS are the dominant factor leading to Fermi level pinning at metal semiconductor interfaces in the vicinity of the charge neutrality level E_{CNL} of the semiconductor [13]. MIGS decay into the band gap of the semiconductor when a metal comes into contact with the semiconductor surface [11] (see Figure 1a). When Fermi level pinning is overcome with interface engineering, the metal work function can be used to adjust the effective barrier height (see Figure 1b).

The ability to change the Schottky barrier height at a metal-semiconductor interface by the metal work function is described by the pinning factor S_{MIGS} with

$$\frac{\delta\Phi_{\mathrm{SB}}}{\delta\Phi_{\mathrm{m}}} = S_{\mathrm{MIGS}} = \left(1 + q^2 \frac{\delta \times D_{\mathrm{MIGS}}}{\varepsilon_0 \varepsilon_{\mathrm{r}}}\right)^{-1} \tag{1}$$

where q is the electric charge, ε_0 the vacuum permittivity and ε_{r} is the relative permittivity of the material of which the Fermi level is pinned. D_{MIGS} and δ are the density of MIGS at the interface and the decay length, respectively, given by:

$$D_{\mathrm{MIGS}} = \frac{2}{a^2 \pi E_{\mathrm{g}}}, \qquad \delta = \frac{h^2}{2\pi m_0 a E_{\mathrm{g}}} \tag{2}$$

with h being Planck's constant, m_0 the free electron mass, a the lattice constant and E_{g} the band gap of the semiconductor. If the decay length δ in Equation (2) is interpreted as the thickness of the interface layer the metal-semiconductor contact can be regarded as a metal-insulator-semiconductor (MIS) capacitor. As a result, Equation (1) provides

the change of surface potential (i.e., $\delta\Phi_{SB}$) with changing gate potential ($\delta\Phi_m$) given by $1 + C_{MIGS}/C_{interface}$ with $C_{MIGS} \approx q^2 D_{MIGS}$ and $C_{interface} = \varepsilon_0\varepsilon_r/\delta$ being the density of MIGS and interface layer capacitors per area, respectively. If $C_{MIGS} \gg C_{interface}$, S_{MIGS} tends to zero, the Schottky barrier is hardly changed and hence the Fermi level is pinned. On the other hand, in the case $C_{MIGS} \ll C_{interface}$, $S_{MIGS} \approx 1$ and the so-called Schottky–Mott limit is reached [11–13,23]. Since both D_{MIGS} as well as δ are inversely proportional to E_g, Fermi level pinning occurs in materials with small band gaps. Insulators on the other hand are more or less depinned due to their large E_g. Figure 2 shows the pinning factor extracted from literature values for different insulators and semiconductors as a function of their band gap.

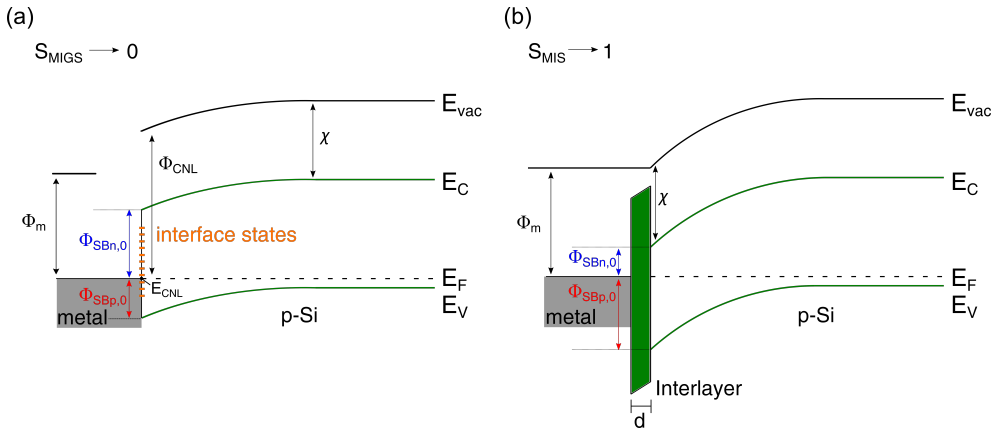

Figure 1. Band structure at metal-semiconductor contacts: (**a**) Metal/*p*-Si Schottky contact exhibiting Fermi level pinning around E_{CNL} that occurs due to a high density of interface states consisting of MIGS, as well as possible defects, dangling bonds, etc. (**b**) Metal/interlayer/*p*-Si interface: The interlayer blocks MIGS so that the band alignment is determined by the difference of metal work function and silicon electron affinity.

An effective work function Φ_{eff} that determines the band alignment of the Schottky contact can be described with help of the pinning factor [7,12,13]:

$$\Phi_{eff} = S_{MIGS}\Phi_m + (1 - S_{MIGS})\Phi_{CNL} \quad (3)$$

with Φ_{CNL} being the potential between E_{CNL} and the vacuum level E_{vac}. The charge neutrality level is the energy level at the interface due to the charge transfer between metal and semiconductor to compensate for surface states. Therefore, placing an interface layer with large band gap on top of a semiconductor with small E_g allows removing Fermi level pinning. In the following this will be discussed in more detail.

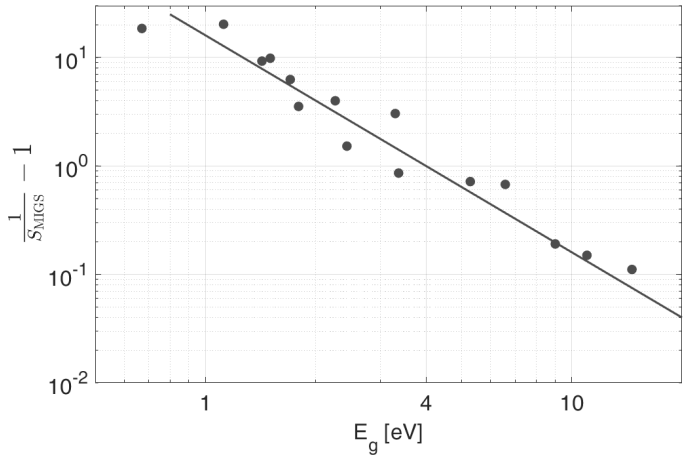

Figure 2. Pinning factor for different insulators and semiconductors from experimental data as a function of their band gap. The fit shows a $\frac{1}{S_{\mathrm{MIGS}}} - 1 = \frac{15}{E_g^2}$ dependency between band gap and S_{MIGS} [13].

1.1.1. Pinning Behavior without Interlayer ($S_{\mathrm{MIGS}} \to 0$)

From Figure 2, the pinning factor for silicon (E_g = 1.12 eV) of $S_{\mathrm{MIGS}} \approx 0.087$ can be extracted resulting in rather strong Fermi level pinning. Hence, the Schottky barrier height is nearly independent of the metal work function in use and the potential at the interface changes only slightly around the charge neutrality level E_{CNL}. Typical Schottky barriers at a pinned interface on n-Si are $\Phi_{\mathrm{SBn},0} = 0.8$ eV and $\Phi_{\mathrm{SBp},0} = 0.3$ eV with respect to the conduction and valence band, respectively, for metals with a rather high work function (see Figure 1a) [12,18].

1.1.2. Pinning Behavior with Interlayer ($S_{\mathrm{MIGS}} \to 1$) and Choice of Material

If an interlayer of thickness d is present, the density of MIGS at the metal-interlayer interface $D_{\mathrm{MIGS},0}$ decays exponentially across the interlayer. As a result, the reduced density of MIGS at the interlayer-silicon interface is a function of the interlayer thickness $D_{\mathrm{MIGS}}(d)$ which is given by:

$$D_{\mathrm{MIGS}}(d) = D_{\mathrm{MIGS},0}\, e^{-\frac{d}{\delta_{\mathrm{IL}}}} \tag{4}$$

where δ_{IL} is the decay length of the interlayer.

From Equation (1) and Equation (4) the Fermi level pinning at the interlayer-semiconductor interface is then given by [11,23]:

$$S_{\mathrm{MIGS}}(d) = \left(1 + q^2 \frac{D_{\mathrm{MIGS}}(d)(\delta_{\mathrm{Si}}\varepsilon_{\mathrm{IL}} + d\varepsilon_{\mathrm{Si}})}{\varepsilon_0(\varepsilon_{\mathrm{IL}} + \varepsilon_{\mathrm{Si}})}\right)^{-1} \tag{5}$$

with $\varepsilon_{\mathrm{IL}}$ the electric permittivity of the interlayer.

Since the interlayer has its own intrinsic pinning factor S_{IL} calculated according to Equation (1), combining the intrinsic pinning factor of the interlayer and the interlayer dependent pinning factor of the semiconductor, Equation (5) is extended to the effective pinning factor of the whole MIS structure [23]:

$$S_{\mathrm{MIS}} = \left(1 + \frac{\varepsilon_{\mathrm{IL}}(1 - S_{\mathrm{IL}})e^{-\frac{d}{\delta_{\mathrm{IL}}}}(\delta_{\mathrm{Si}}\varepsilon_{\mathrm{IL}} + d\varepsilon_{\mathrm{Si}})}{S_{\mathrm{IL}}\delta_{\mathrm{IL}}(\varepsilon_{\mathrm{IL}} + \varepsilon_{\mathrm{Si}})}\right)^{-1} \tag{6}$$

Equation (6) suggests that Fermi level depinning can be achieved either with $S_{\mathrm{IL}} \to 1$, $\delta_{\mathrm{IL}} \to 0$ or $d \to \infty$. However, one has to keep in mind that this yields an exponentially

reduced transmission of carriers (cf. Equations (1) and (2)) and hence unacceptably high contact resistivities as confirmed with Wentzel–Kramers–Brillouin (WKB) simulations [23].

Another important point needs to be mentioned at this stage of the discussion: When searching for an appropriate interface material, the band alignment between the silicon bands and the interlayer is critical. It appears preferable to choose an insulator with high band gap but small conduction or valence band offsets $\Delta E_C(\Delta E_V) \approx 0$ in order to obtain proper contacts to the conduction and valence bands, respectively (cf. Figure 3b) [13,23]. Simulations [1,28] and experiments [23] show that TiO_2 and even more ZnO are materials that yield substantially improved *n*-type contacts while blocking holes. Materials with band alignment close to the valence band could be NiO or $CuAlO_2$ [7,28] which has been confirmed experimentally [28]. However, the band gaps of the mentioned materials are rather small (3.2–3.6 eV) and the charge neutrality point of, e.g., ZnO is close to the conduction band. As a result, the demonstrated low contact resistivities of ZnO and TiO_2 are rather due to a repinning of the Fermi level close to the conduction band. Hence, for proper *n*-type and *p*-type contacts on the same chip, two different materials are required. However, from a fabrication point of view, this requirement of two different, very thin insulators is a drawback. Moreover, during deposition of oxides (such as the TiO_2, ZnO, NiO, etc.) and a possible subsequent annealing step, a SiO_x layer usually forms that will impact the respective contact properties.

In the case considered here, we aim at using a single material as depinning layer. To this end, Fermi level repinning at the metal-interlayer interface needs to be avoided. Taking into consideration that typical metals cover a work function range of approximately 2.5 eV and that the Schottky barrier needs to be modified across the band gap of silicon, a material satisfying $S_{MIGS} = 1.12\,\text{eV}/2.5\,\text{eV} = 0.45$ (cf. Equation (1)) needs to be chosen. From Figure 2, it is apparent that the band gap of such an interlayer needs to be $E_g \geq 4$ eV. Silicon nitride with a band gap of 5.1 eV, a conduction band offset of ≈2 eV and the fact that extremely thin layers can be grown thermally with high precision and reproducibility that prevent oxide growth of the silicon surface make SiN an ideal candidate material as depinning layer (cf. Figure 3a).

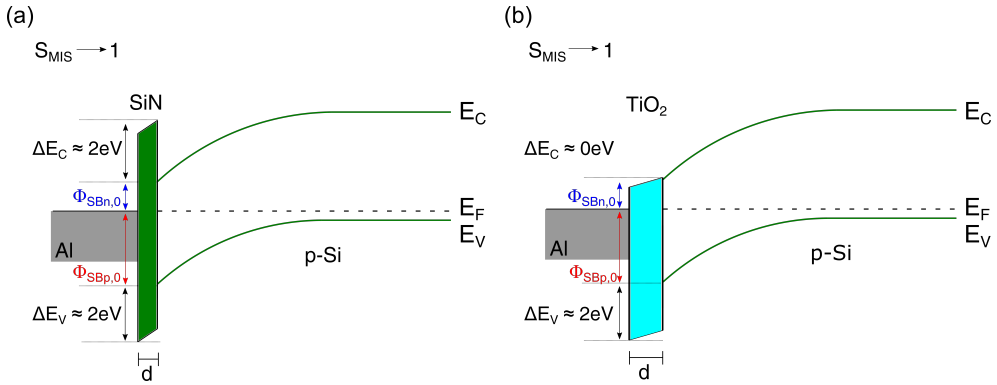

Figure 3. Comparison of band alignments for Schottky contacts with (**a**) a SiN interlayer and (**b**) a TiO_2 interlayer.

2. Materials and Methods

2.1. Fabrication of Schottky Diodes

Al/SiN/*p*-type Si Schottky diodes were fabricated without and with SiN interlayers in order to investigate the Fermi level depinning as a function of thermally grown SiN layer thickness. A 50 nm *p*-doped silicon-on-insulator (SOI) with a resistivity of 5–10 Ω cm and a buried oxide (BOX) layer of 100 nm substrate was used. The SOI layer was patterned into mesa structures using optical lithography and a SF_6/O_2 dry etching process. Subsequently, another optical lithography and ion implantation of boron with a dose of 5×10^{15} cm^{-2} at 2 kV acceleration voltage were carried out in order to realize one ohmic contact region for each Schottky diode. After resist ashing and a Piranha clean (H_2SO_4:$H_2O_2 = 3:1$), the

dopants were activated at 940 °C for 13 s in 2000 sccm Ar at 1000 mbar in a rapid thermal annealing tool. ECV measurements of dummy samples implanted and activated with the same parameters confirm a doping concentration of 9×10^{-19} cm^{-3} at the doped Si surface. Prior to the fabrication of the SiN layer, a RCA-clean at 80 °C [29] was performed followed by a short HF-dip (1%) immediately before the nitridation process in order to remove the native oxide from the silicon surface. Rapid thermal nitridation in 2000 sccm ammonia (NH_3) at 1000 mbar for 60 s at different temperatures was conducted in order to grow the SiN layers. The resulting thickness of the SiN layer can be adjusted very precisely by varying the temperature of the process (see Figure 4) as the diffusion of nitrogen through the grown SiN layer is a self-saturating process where the maximal diffusion length depends almost exclusively on the temperature. Since the temperature does not only influence the thickness but also the quality of the SiN layer, as the dissociation of NH_3 is dependent on temperature as well, the different SiN layers will be referred to their growth temperature and not their thickness.

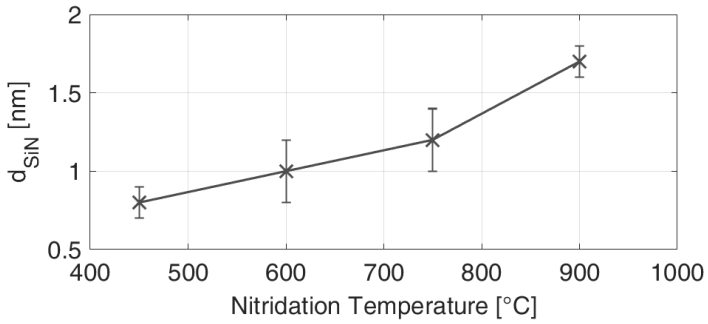

Figure 4. SiN thickness achieved by rapid thermal annealing of Si substrates in NH_3 at different temperatures for 60 s.

The metal contacts were fabricated by a deposition of 150 nm Al on top of the whole sample surface with electron-beam physical vapor deposition (EBPVD). Subsequently, the Al film was patterned with optical lithography and commercially available Al etch (TechniEtch Al80, MicroChemicals) to form the Schottky contacts. Afterwards, optical lithography and a buffered oxide etch (BOE) were performed, to etch the SiN (and native oxide in case of the reference sample without interlayer) in order to open the ohmic contact areas for metallization. After resist removal with aceton and isopropanol, samples were immediately mounted for EBPVD of 150 nm Al followed by structuring the ohmic contacts with optical lithography and Al wet etch. Finally, a post metal annealing (PMA) in N_2/H_2 forming gas at 400 °C for 30 min was performed. In order to characterize the impact of the PMA process, *I–V* measurements were taken before and after PMA. The measurements were carried out with a Keithley 4200-SCS parameter analyzer using two pre-amplifiers. Figure 5 shows the schematic cross-section of the Schottky diode.

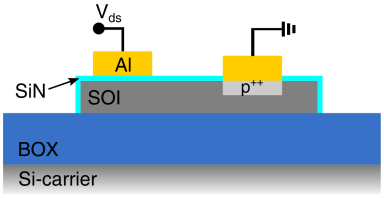

Figure 5. Schematic assembly of Schottky diodes with Al/SiN/*p*-Si Schottky contact and p^{++} doped ohmic contact.

2.2. Fabrication of Schottky Barrier MOSFETs

Characteristic of Schottky barrier MOSFETs are Schottky S/D-contacts without additional doping. So the fabrication of such devices reduces to the following: The SOI substrate consist of SOI: 10^{15} cm^{-3} Boron doped 80 nm *p*-Si and 2 µm BOX. The structuring

of the Si mesa structures was performed as described above. After resist ashing, a Piranha clean with subsequent RCA-process was carried out. An HF-dip removed the native oxide immediately before the rapid thermal nitridation process (300 sccm NH_3/1000 sccm Ar gas mixture at 1000 mbar for 60 s, Annealsys AS-One system (Montpellier, France)). When using Al as a contact metal, 150 nm Al were deposited with EBPVD on the whole sample surface and the contacts were patterned, as described above. When using Co as a contact metal, the samples were patterned with optical lithography to perform a lift-off process after 150 nm EBPVD deposition of Co. The samples have not been annealed after contact formation. In its simplest form, the handle wafer of the SOI wafer can be used as large area back gate yielding a so-called pseudo MOSFET as schematically shown in Figure 6a.

In order to fabricate top gate MOSFETs, processing continued with atomic layer deposition (ALD) at 300 °C of 20 nm Al_2O_3 as the gate oxide. Afterwards, 150 nm Al as gate metal have been EBPVD deposited and top gate structures have been patterned with optical lithography and wet chemical etching of Al as described before. Finally, a PMA was performed in N_2/H_2 for 30 min at 400 °C. It should be mentioned that due to the fabrication process the area underneath the gate electrode is covered with SiN between Si and Al_2O_3, too. A schematic cross-section of a top gated Schottky barrier MOSFETs is shown in Figure 6b.

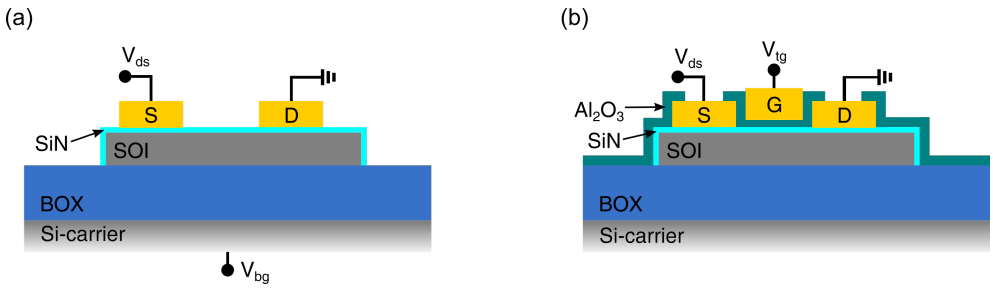

Figure 6. Schematic cross-sections of Schottky barrier MOSFETs with metal/SiN/*p*-Si contacts and (**a**) back gate (pseudo MOSFET) or (**b**) a top gate electrode.

2.3. Extraction of Schottky Barrier Heights

The forward current characteristics of a Schottky diode described by the thermionic emission model [12] is given by Equation (7) which is valid for voltages $V > 3kT/q$.

$$I = I_S \left(\exp\left(\frac{qV}{nkT} \right) - 1 \right) \tag{7}$$

where V is the voltage across the diode, k the Boltzmann constant and T the absolute temperature. n is a dimensionless ideality factor, that takes non-idealistic diode behavior into account. I_S is the so-called saturation current [30] that is defined as:

$$I_S = AA^*T^2 \exp\left(\frac{q\Phi_{SB}}{kT} \right) \tag{8}$$

with A being the effective contact area, A^* the effective Richardson constant and Φ_{SB} the Schottky barrier height. The Richardson constant is defined as:

$$A^* = \frac{4\pi q m^* k^2}{h^3} \tag{9}$$

with m^* being the effective mass of the charge carriers. Experimental values differ slightly from the calculated values so that for practical applications A^* can be considered as 30 A cm^{-2} K^{-2} for *p*-doped silicon and 110 A cm^{-2} K^{-2} for *n*-doped Silicon [12]. Taking into account the series resistance of the diode by considering the device as a series combination

of the diode and a resistor with resistance R, the voltage across the diode V will be replaced by $V = V_{app} - IR$ with V_{app} being the applied voltage leading to Equation (7)

$$I = I_S \left(\exp\left(\frac{q(V_{app} - IR)}{nkT} \right) - 1 \right). \tag{10}$$

The Schottky barrier was extracted by the method presented by Cheung and Cheung [31]. This method has the benefit that the Schottky barrier, ideality factor and series resistance can be obtained by a single *I-V* measurement of the forward current. Combining Equation (8) to (10), using the current density J instead of the current I and solving for V_{app} gives

$$V_{app} = R \cdot A \cdot J + n\Phi_{SB} + \frac{nkT}{q} \ln\left(\frac{J}{A^* T^2} \right). \tag{11}$$

Then, computing the derivative $\frac{d(V_{app})}{d(\ln J)}$ yields

$$\frac{d(V_{app})}{d(\ln J)} = R \cdot A \cdot J + \frac{nkT}{q}. \tag{12}$$

As a result, plotting the derivative $\frac{d(V_{app})}{d(\ln J)}$ of experimental data as a function of J yields $R \cdot A$ as the slope and $\frac{nkT}{q}$ as the y-axis intercept, and, thus, enables obtaining R and n. In order to extract the Schottky barrier Φ_{SB}, a function $H(J)$ is defined with help of Equation (11) giving another linear dependency:

$$H(J) \equiv V_{app} - \frac{nkT}{q} \ln\left(\frac{J}{A^* T^2} \right) = R \cdot A \cdot J + n\Phi_{SB}. \tag{13}$$

Here, the y-axis intercept will give the Schottky barrier Φ_{SB} with n determined as discussed above. Furthermore, the slope of the $H(J)$ plot will be $R \cdot A$ again. Comparing the resistance values extracted from the two plots allows reconfirming the results and hence the consistency of the method.

In addition to the approach detailed so far, a simple method for the extraction of Φ_{SB} and n based on Equation (7) is performed. Plotting $\ln(I)$ over V_{app} gives the slope of the linear region as $\frac{q}{nkT}$ and the saturation current I_S as the y-axis intercept [30]. The Schottky barrier is then extracted by solving Equation (8) for Φ_{SB}. The values of both methods are compared for verification of the results.

3. Results and Discussion

3.1. Schottky Barrier Height for Different SiN Interlayers

The Schottky barrier height is extracted from Schottky diodes with different SiN interlayer thicknesses before and after PMA. Before PMA (Figure 7a), a dependency of the Schottky barrier on the interlayer thickness does not emerge clearly. $\Phi_{SB,p}$ is around 0.75 eV for the reference sample (compared to [32]), 450 °C SiN interlayer and 900 °C SiN interlayer and decreases to 0.65 eV for the diodes with SiN fabricated at 600 °C and 750 °C. After PMA (Figure 7b), the contact properties change dependent on the interlayer.

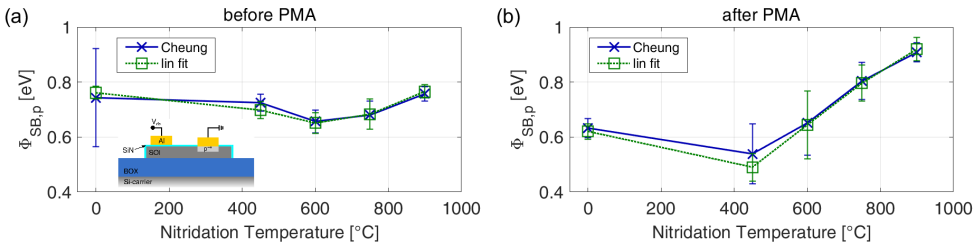

Figure 7. Schottky barrier of devices with different SiN interlayers (**a**) before PMA and (**b**) after PMA.

The Schottky barrier heights of the reference sample without an interlayer and the sample with thinnest (450 °C) SiN decrease with respect to the valence band to 0.63 eV and 0.51 eV, respectively, so that it is closer to the middle of the band gap. The barrier height of the SiN fabricated at 600 °C stays the same (0.65 eV) while it increases for the samples with thicker SiN layers, resulting in a small barrier to the conduction band ($E_g - \Phi_{SBp,0} = \Phi_{SBn,0}$). A SiN layer fabricated at 750 °C lowers the barrier to the conduction band to 0.32 eV after PMA. The thickest layer fabricated at 900 °C reduces the Schottky barrier to the conduction band to 0.2 eV which is the expected ideal value from $\Phi_{SBn,0} = \Phi_m - \chi_{Si}$ with $\Phi_{m,Al} = 4.25$ eV and $\chi_{Si} = 4.05$ eV. For further consideration of the influence of each SiN layer to the contact properties, the ideality factor and series resistance extracted from the same measurements should be evaluated.

3.2. Ideality Factor and Series Resistance

Without PMA, the series resistance for the Schottky barrier without a SiN interlayer is two orders of magnitude larger (374 MΩ/µm) than with a SiN interlayer (Figure 8a). It decreases after PMA, but still is much higher than the resistance of the devices with an interlayer. When having an interlayer, the values vary between 1 MΩ/µm and 16 MΩ/µm without PMA. The resistance and its deviations are smaller for thin SiN layers. After PMA (Figure 8b), the series resistance decreases for thicker layers towards 0.1 MΩ/µm, which is comparable to the magnitude of the resistance of the silicon channels of the SOI substrate without any applied gate voltage.

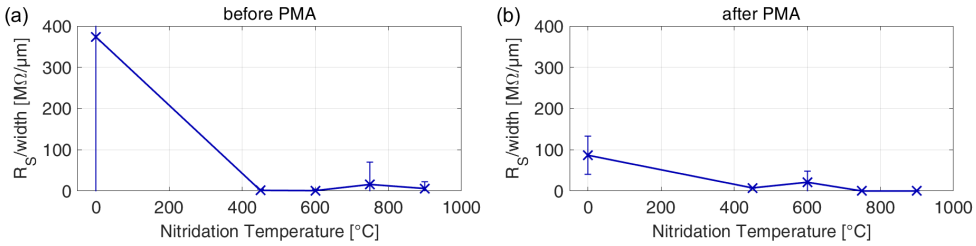

Figure 8. Series resistance (**a**) before PMA and (**b**) after PMA, extracted by the method of Cheung [31]. The series resistance is given in MΩ/µm in order to reduce the error caused by different device geometries.

However, for both thin SiN layers (450 °C and 600 °C), the series resistance has increased to 7 MΩ/µm and 21 MΩ/µm, respectively, though the tunnel probability increases for decreasing thickness of an interlayer [12]. The resistance of the 600 °C SiN layer device has not only increased, but so has the deviation. Considering the ideality factor (Figure 9), it is obvious, that these values differ from the expected behavior in the same way, since the ideality factor (Figure 9) increases to unreasonably high values with high deviations ($d_{SiN} = 0$ nm and 600 °C SiN) or n is not even evaluable anymore (450 °C) with Cheung's method.

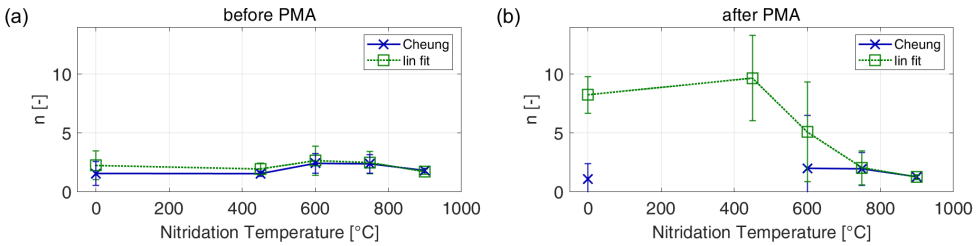

Figure 9. Ideality factor of Schottky diodes (**a**) before PMA and (**b**) after PMA.

The review of a single I_d-V_{ds}-measurement of each contact layer stack gives the reason for the differing behavior with regard to the ideality factor and series resistance. The ideal diode behavior with an exponential increase (linear regime in logarithmic scale) in forward direction for $V > 3kT/q$ until the series resistance dominates the current flow and a low reverse current is visible for all measurements before PMA (Figure 10a).

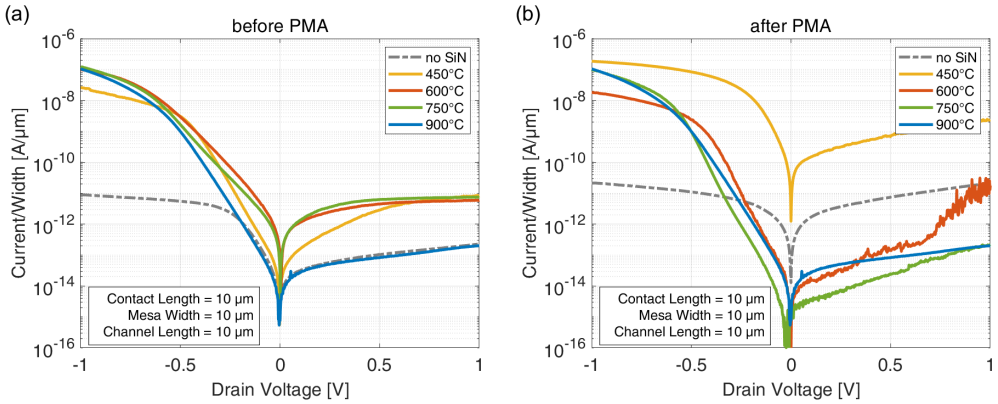

Figure 10. Single measurements of same geometry with different SiN thicknesses (**a**) before PMA and (**b**) after PMA.

However, after PMA (Figure 10b), the I_d-V_{ds} behavior of the samples without an interlayer and with the 450 °C SiN changes. An exponential increase in the current of the reference sample is not visible anymore and the reverse current is as high as the forward current. A linear plot would reveal a linear and symmetric I_d-V_{ds} behavior. The low absolute current can be explained by the high series resistance. For the sample with the 450 °C SiN layer the reverse current has increased severely and the forward current is rather linear than exponential.

Al/Si contacts without an interlayer are known to undergo a metallurgical reaction in high temperature processes [33]. After dissolving in aluminum up to its solubility limit during the high temperature process [34], silicon recrystallizes epitaxially at the Al/Si interface when it is cooled. This recrystallized silicon is heavily doped with Al [18], so a *p*-type layer has been formed resulting in a nearly ohmic contact at the Schottky barrier side of the device.

In order to find out why the diodes with the 450 °C SiN interlayer, that should act as a diffusion barrier, show similar I_d-V_{ds} behavior to the sample without interlayer, the SiN layers are investigated more thoroughly. The lower the temperature of the rapid thermal nitridation process, the higher is the hydrogen amount in the SiN layer [35]. A higher hydrogen concentration deteriorates the insulating properties [35]. Another observation is that the 450 °C SiN layer allows diffusion of oxygen during high temperature processes. In order to evaluate the physical barrier properties of the SiN layers, two tests were conducted. First, a Al/SiN/Si layer stack was fabricated compared to the diode process (but with a gas mixture for nitridation of 300 sccm NH_3/1000 sccm Ar). After PMA, the Al was wet chemically etched. SEM pictures (Figure 11) show a strong deterioration of the Si surface for the reference sample and of the Si/SiN surface of the one with the 450 °C SiN layer. When the SiN layer is not completely closed, Si will dissolve into Al and diffuse at the Al/SiN interface. Sankur et al. [36] measured that the effect of recrystallization is stronger at reentrant corners compared to a flat surface. Thus, the SEM pictures support the assumption of an metallurgical reaction on the contact area of the 450 °C SiN interlayer sample so that islands of strongly *p*-doped Si form after PMA, leading to an overcoming of the Schottky barrier towards a *p*-type ohmic behavior.

Second, the diffusion barrier of the SiN layers was characterized by a thermal oxidation process. This method has been used before [37] in order to characterize the density of SiN layers. The samples were fabricated in the same way as before until the thermal nitridation. Then, just after the thermal nitridation process, without opening the process chamber an oxidation process (1050 °C, 2000 sccm O_2, 240 s) was started. The resulting oxide thickness is measured with spectroscopic ellipsometry at multiple wavelengths. Figure 12 shows that the thin SiN layers (450 °C and 600 °C) hardly prevents the oxidation whereas thicker SiN layers reduce an oxidation drastically. Both tests indicate a porosity of the thin SiN layer.

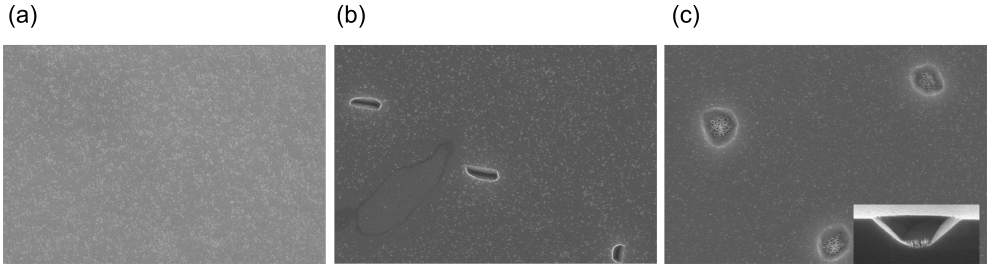

Figure 11. Sample surfaces of (**a**) Si + 900 °C SiN, (**b**) Si + 450 °C SiN, (**c**) Si without SiN, after Al deposition, PMA and subsequently wet chemical removal of Al.

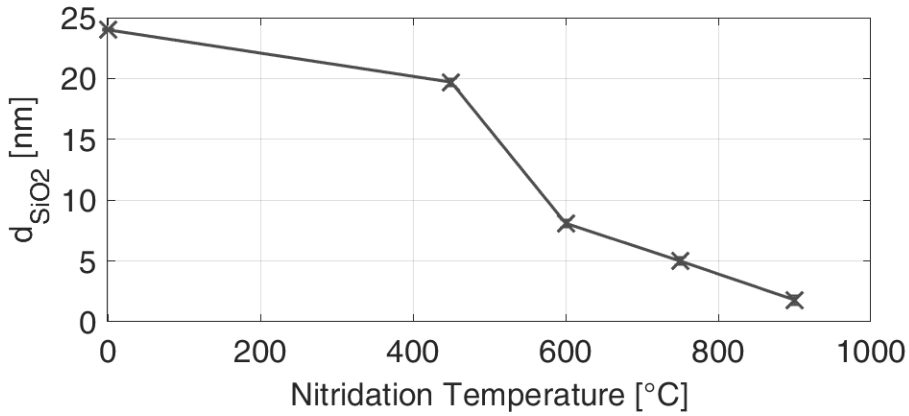

Figure 12. Oxide thickness grown through different SiN layers to point out the density of different SiN layers.

The large distribution of measured values of Φ_B, n, and R_S in the case of the °C SiN interlayer diode can be ascribed to the same defects observed for the thinnest SiN layer. However, they occur far less so that the defects do not determine the overall diode behavior.

3.3. Electrical Characteristics of SB-MOSFETs with Varying Interlayers

After depinning the Fermi level the work function of different contact metals can be used to obtain *n*- and *p*-type MOSFET behavior. Back gate controlled samples (see Figure 6a) have been fabricated without PMA. Figure 13a shows the switching behavior for a 450 °C and 900 °C SiN interlayer and a reference sample without an interlayer. When applying a back gate voltage to the sample with no interfacial layer, ambipolar switching behavior with no defined off-state is observed. Though the Schottky barrier heights before PMA do not show significant differences when inserting different SiN layers, a change in the switching behavior due to them is observed. For the 900 °C SiN interlayer, a strong *n*-type behavior is observed as the *p*-type current is strongly suppressed which leads to an I_{on}/I_{off}-ratio of 10^6. In case of the 450 °C SiN device the *p*-branch is less suppressed so that the switching behavior still shows ambipolar behavior but with a reduced *p*-type current compared to the reference sample. In addition, output characteristics (Figure 13b) show an exponential current increase for the reference sample while the current increases more linearly when adding the SiN interlayers.

The realization of unipolar switching behavior by modifying the Schottky barrier with Fermi level depinning and choosing a metal with appropriate work function was reported recently by Fischer et al. (Figure 14a). He characterized circular pseudo MOSFETs (*p*-Si SOI 200 nm, 200 nm BOX, no PMA) not only with Al to have a good contact towards the conduction band but also with Pt as a metal with a high work function.

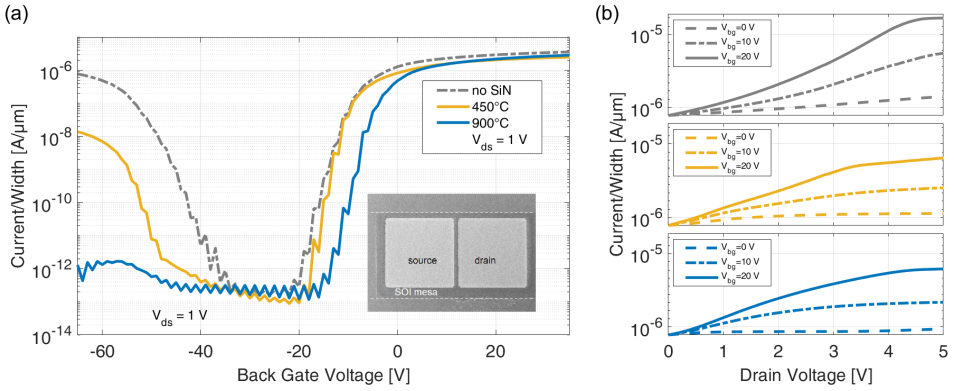

Figure 13. (**a**) Switching behavior ($V_{ds} = 1V$) and (**b**) output characteristics of pseudo MOSFETs using Al contacts and different SiN layer thicknesses without PMA (80 µm contact length and width, 5 µm channel length).

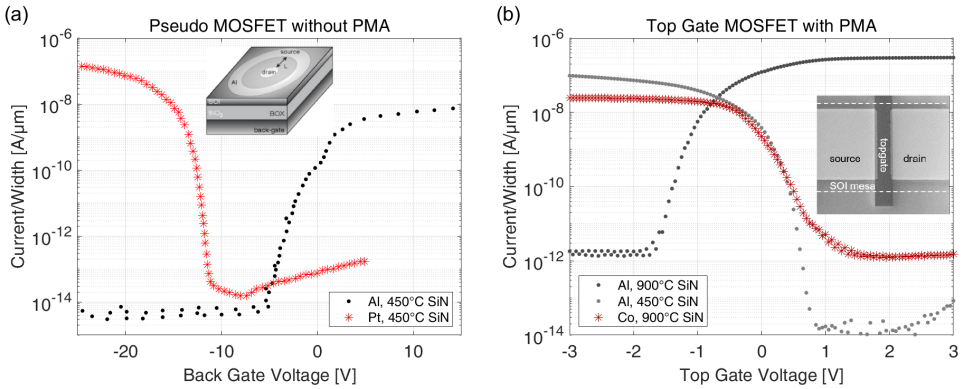

Figure 14. Comparison of *p*- and *n*-type switching behavior (**a**) as reported before with 450 °C SiN layer on a pseudo MOSFET without PMA ($r_d = 300$ µm, $r_s = 845$ µm, $L_{Ch} = 545$ µm) [22] and (**b**) measured on a top gate MOSFET with 450 °C and 900 °C SiN layer with PMA ($V_{ds} = -1$ V, 400 µm contact length and width, 45 µm channel length).

Using contact metals with higher work functions (e.g., Pt (≈5.65 eV), Ni (≈5.15 eV), Co (≈5 eV) [12]) a reduced Schottky barrier towards the valence band can be provided ($\Phi_{SBp,0} = E_g - \Phi_{SBn,0}$). That leads to a more *p*-type switching behavior as shown in Figure 14a (red curve) with an on-/off-ration of $I_{on}/I_{off} = 10^6$. As an interlayer a 450 °C SiN layer was used. The on current of the Pt device is slightly higher compared to the Al device which implies that the remaining Schottky barrier to the respective band is lower using Pt. Assuming perfect Fermi level depinning the remaining Schottky barrier in case of Pt towards the valence band is $\Phi_{SB,p} = -0.48$ eV what means a complete removal of the Schottky barrier between metal and valence band whereas for Al a small barrier of $\Phi_{SB,n} = 0.2$ eV remains towards the conduction band.

In order to demonstrate the same functionality on top gate controlled devices, we fabricated and characterized SOI top gate MOSFETs (see Figure 6b). Though Co has a lower work function than Pt, it is still high enough to obtain *p*-like switching behavior with a 900 °C SiN interlayer as shown in Figure 14b. A top gate voltage between −3 V to 3 V has been applied. An inverse subthreshold slope *S* of 343 mV/dec was measured. As the remaining Schottky barrier to the valence band of a ideal Co/SiN/Si contact with $\Phi_{SBp,0}$= 0.17 eV is higher compared to the Pt sample, the I_{on}/I_{off}-ratio ($I_{on}/I_{off} = 10^4$) is smaller as well.

The same measurement have been performed to Al contacts with 900 °C SiN and 450 °C SiN layer. As shown with the pseudo MOSFET measurements in Figure 13, the top gate controlled device with an 900 °C SiN layer shows just the same strong *n*-type behavior in accordance to the reduced Schottky barrier towards the conduction band.

Compared to the Co devices, an even steeper switching behavior of 163 mV/dec and $I_{on}/I_{off} = 10^5$ is measured. In contrast to the pseudo MOSFET measurements without PMA, the 450 °C SiN top gate device with Al contacts shows a *p*-type switching behavior with a strong suppressed *n*-type off-state current. This indicates a heavily Al doped silicon at the interface caused by the PMA due to a leaky SiN interface as already discussed above.

4. Conclusions

We measured Schottky barriers of Al/SiN/*p*-Si diodes showing Fermi level depinning with help of SiN interlayers. Increasing the process temperature at the rapid thermal nitridation process leads to higher thickness and improved layer quality. The diode fabricated at 900 °C reaches the theoretical value of the depinned Schottky barrier to the conduction band with Al as a metal of $\Phi_{SB,n} = 0.2$ eV. As Fermi level depinning of the Schottky barrier with the SiN interlayer has been proved, metals with different work functions can be used to modify the Schottky barrier. The effect of the modified barrier to the resulting switching behavior has been shown as the Schottky barrier MOSFETs turn from ambipolar to unipolar behavior with increasing interlayer thickness. Furthermore, we presented *n*-type behavior with Al and *p*-type behavior with Co with the same SiN interlayer. Thus, thermally grown SiN layers are a useful method suppress Fermi level pinning and enable reconfigurable contacts by choosing an appropriate metal.

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