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Review

Comprehensive Review of Wide-Bandgap (WBG) Devices: SiC MOSFET and Its Failure Modes Affecting Reliability

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Abstract: Silicon carbide (SiC) MOSFETs, as a member of the emerging technology of wide-bandgap (WBG) semiconductors, are transforming high-power and high-temperature applications due to their superior electrical and thermal properties. Their potential to outperform traditional silicon-based devices, particularly in terms of efficiency and operational stability, has made them a popular choice for power electronics. However, reliability issues about numerous failure types, including gate-oxide degradation, threshold voltage instability, and body diode degeneration, remain serious challenges. This article critically evaluates the key failure mechanisms that affect SiC MOSFET reliability and their impact on device performance. Furthermore, this paper discusses current advances in SiC technology, including both improvements and continued dependability difficulties. Key areas of future study are suggested, with an emphasis on improved material characterization, thermal management, and creative device architecture to improve SiC MOSFET performance and long-term reliability. The insights presented will help to improve the design and testing processes required for SiC MOSFETs' widespread use in critical high-power applications.

Keywords: WBG devices; SiC MOSFET; overview; failure modes

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1. Introduction

Switching losses in power electronics play a crucial role in electronic devices' efficiency. Currently, the most common semiconductor material used in power devices is silicon (Si). However, silicon's inherent physical limitations restrict its use in certain applications, preventing both discrete devices and modules made from Si from being viable in various fields. Since the 1950s, silicon (Si) has been the primary material used in the production of integrated circuits (ICs), meeting a wide range of requirements in a variety of applications. Si-based semiconductors are easy to produce and have very few imperfections. However, as is well known, silicon has reached its limits in terms of blocking voltage, heat resistance, efficiency, and operating speed [1]. As power devices based on silicon get closer to their material limits, researchers have launched several attempts to identify substitutes for Si-based power components for enhanced performance [2–4]. To overcome the limitations of silicon, researchers are investigating wide-bandgap (WBG) semiconductors, such as silicon carbide (SiC), gallium nitride (GaN), gallium oxide (Ga_2O_3), and diamond-based power devices. SiC includes many crystal types known as polytypes. These kinds of materials have various patterns of silicon (Si) and carbon (C) atoms, which affect how they transmit electricity, handle heat, reflect light, and maintain strength [1].

This paper provides a comprehensive analysis of SiC MOSFET failure modes, focusing on reliability challenges and long-term performance limitations. This analysis examines topics such as gate-oxide deterioration, threshold voltage instability, and body diode failure to illustrate the existing limits of SiC technology in power electronics. This research also intends to investigate alternative techniques for resolving these dependability challenges, such as advances in material characterization, heat control, and novel device architecture. Through this analysis, the paper hopes to offer future research approaches that will aid in the development of more reliable SiC MOSFETs, allowing for their wider acceptance in high-power, high-temperature applications.

2. Wide-Bandgap (WBG) Devices

Because of their greater bandgap, some semiconductors are categorized as wide-bandgap semiconductors. With a bandgap of 1.1 eV, silicon is not regarded as a semiconductor with a broad bandgap [5]. Table 1 shows that the bandgaps of WBG semiconductors are at least three times greater than those of Si.

Table 1. Physical properties of WBG devices [5–7].

Properties	Si	4H-SiC	GaN	Ga_2O_3	Diamond
Bandgap energy	1.1	3.2	3.4	4.7	5.5
Breakdown field (10^6 V/cm)	0.3	3	3.5	8	13
Electron mobility (10^3 cm^2/V.s)	1.3	0.9	1.5	0.3	2
Saturation drift velocity (10^7 cm/s)	1	2	2.5	2	1.5
Thermal conductivity (W/cm.k)	1.5	3.7	1.3	0.1	22.9

WBG materials have a higher breakdown field and bandgap, as shown in Table 1. As a result, power devices based on WBG semiconductors have greater breakdown voltage capabilities. Device layers can be made thinner at the same breakdown voltage levels by achieving significantly greater doping levels with a strong electric breakdown field. Drift-area resistances of the resulting WBG semiconductor-based power are less. This means that WBG devices have significantly lower ON resistance compared to Si-based devices at the same breakdown voltage [5–7].

Drift velocity is directly related to a semiconductor's high-frequency switching capacity or switching speed. Since the drift velocities of WBG materials are more than double those of Si, it is anticipated that power devices based on WBG semiconductors would be able to switch at greater frequencies than those based on Si.

The benefits of WBG semiconductors include increased radiation hardening and high-temperature functioning. The thermal energy of the electrons in the valence band rises with temperature. They possess enough energy at a specific temperature to migrate into the conduction band. Avoiding this uncontrolled conduction is necessary. For Si, this occurs at a temperature of around 150 °C [5]. Since the bandgap energy of WBG semiconductors is larger, it takes more thermal energy for electrons in the valence band to migrate to the conduction band. In many comparisons SiC outperforms Si counterparts without losing electrical properties. GaN devices have greater high-frequency performance and a higher level of breakdown than Si devices among the wide-bandgap semiconductors that are now on display for the mid-power range application sector. Devices with less than 200 V now dominate the GaN device industry [8]. The market for 600 V GaN devices is predicted to develop rapidly. GaN is primarily used for low-voltage applications, while SiC is preferred for high-voltage applications.

As of right now, Ga_2O_3 is a little-known wide-bandgap semiconductor for use in power electronics. The mid-to-high power range is its objective. Its future course is yet unknown.

The disadvantage of Ga_2O_3 is its weaker heat conductivity as compared to SiC [7]. Device processing technology is already well developed in SiC devices. Reliability is crucial in the realm of high-power electronics, where its primary use is found. SiC MOSFETs have been employed in medium-voltage applications in recent years because of their improved switching performance and voltage capabilities, as discussed in Figure 1. SiC MOSFETs are among the most promising alternatives to Si-based IGBTs for medium-voltage, high-power converter applications [2].

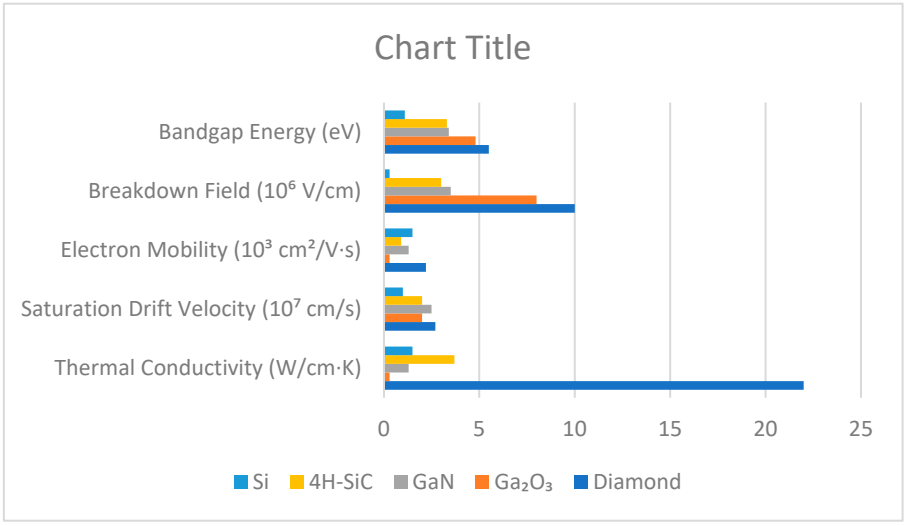


Figure 1. Comparative properties of different WBG materials [2].

2.1. Material Advantages of SiC for Power Electronic Devices

Due to its special combination of characteristics, silicon carbide, a wide-energy-gap semiconductor, is ideal for a wide range of electronic industrial applications. When compared to other semiconductors with wide energy gaps, SiC's physical characteristics—such as a strong electric field, high saturation drift velocity, and superior thermal properties—place it at the forefront of renewed interest in semiconductor material and device development [8]. SiC offers several benefits thanks to the quick progress in single-crystal substrate production technology [9]. Furthermore, the ability to deposit a silicon-like thermal SiO_2 layer on SiC makes it easier to produce SiC MOS-based electronics. Given the demonstrated effectiveness and success of MOS-based devices in fields like storage (nonvolatile memory) [10] and high-power/high-temperature electronics, SiC is acknowledged as the ideal semiconductor with the ability to completely transform electronic system design.

When it comes to power switching device development, unipolar devices—field-effect transistors (FETs) in particular—have received the most attention [11]. There are other varieties of these FETs, such as JFET, MOSFET, and MESFET. Si MOSFETs have become the industry standard in low-power electronic applications requiring fast switching rates for several convincing reasons [12]. Nevertheless, because of silicon's comparatively low breakdown field and the drift region's rapid rise with increasing blocking voltage, the use of Si MOSFETs is often limited to 500 V and below. The high breakdown field and other promising characteristics of SiC material make SiC MOSFETs very attractive as high-power switching device choices. A SiC power device's particular ON resistance is expected to be substantially lower—roughly 100–200 times lower—than that of a silicon device with a comparable rating [13]. SiC's significantly lower thermal minority carrier generation results in lower leakage currents, enabling higher operating temperatures and greater tolerance for power dissipation-induced self-heating in devices. Furthermore, SiC has three times the thermal conductivity of Si, and at room temperature even more than copper. This suggests

that the device's heat extraction process is more effective and reduces the need for further device cooling.

The development of 3C SiC devices is hampered by the absence of technique for growing 3C SiC bulk crystals and the inferior material quality of 3C SiC heteroepitaxial produced on Si. These polytypes are the most promising for electronic device materials because 4H and 6H SiC single-crystal wafers are readily available and of consistently high quality. Table 2 lists the physical and electrical characteristics of these three common polytypes at room temperature, with Si serving as a reference [14]. For most SiC electrical devices, 4H SiC is the favored polytype due to its much higher carrier mobility than 6H SiC [14,15]. Furthermore, 4H SiC will be especially advantageous from 6H SiC's intrinsic mobility anisotropy, which reduces conduction parallel to the crystallographic c-axis, making it especially well suited for vertical power devices. The development of higher-mobility 4H SiC has largely overshadowed the substantial progress made in achieving far better 3C SiC via heteroepitaxy on low-tilt-angle 6H SiC substrates [16,17].

Table 2. Material properties of all WBGs at 300K [14,15].

Property	Si	3C SiC	6H SiC	4H SiC
Dielectric constant	11.8	9.7	9.7	9.7
Energy gap (eV)	1.12	2.39	3.03	3.26
Critical field Ee (MV/cm)	0.3	1.5	3.2	3
Electron mobility (cm^2/Vs)	1400	750	370	800
Hole mobility (cm^2/Vs)	600	40	90	115
Electron drift velocity ($\times 10^7$ cm/s)	1	2.5	2	2
Thermal conductivity (W/cm.K)	1.5	5	4.9	4.9

2.2. Major Intrinsic Advantages of SIC Devices

Early leaders in microelectronics predicted limitations in Si-MOSFET applications in the high-power range and anticipated obstacles to be overcome with new materials-based technologies [3]. Wide-bandgap semiconductors are expected to provide the foundation of the next generation of power devices, with four significant intrinsic advantages:

- Semiconductors' large band gaps enable operation at high electric fields. Because wide-bandgap materials have high-impact ionization energy, large electric fields may be reached without ionized carrier avalanche multiplication. Because of this, wide-bandgap semiconductors have an electric field for accelerating carriers that is many times greater than that of silicon. Breakdown voltages in wide-bandgap semiconductor devices are many times higher than in silicon devices [18–21].
- The inherent connection between a semiconductor's intrinsic carrier concentration and energy gap allows for operation at high temperatures. A smaller concentration of intrinsic carriers is obtained with a wider gap. Wide-bandgap semiconductors, in contrast to silicon, have a greater transition temperature between intrinsic conductivity and doping-dominated extrinsic conduction. Wide-bandgap material-based devices have the benefit of operating at high temperatures [22,23].
- Wide-bandgap semiconductor devices may operate at high frequencies by shrinking in size, which is made possible by the strong electric field that allows for the use of larger doping concentrations in the active portion of the devices. As a result, the input and output capacitances of wide-bandgap semiconductor devices are decreased, opening the door to higher-frequency operation [24].
- Wide-bandgap semiconductors may operate at high current densities because of their high thermal conductivity and electron drift velocity. These characteristics offer the capacity to manage high current densities with low resistances [25].

3. SiC MOSFET Characteristics

SiC technology has matured over time, and most significant semiconductor businesses are making investments in their SiC product line. Performance measurements make the benefits of SiC vs. Si apparent from a device perspective [26]. They have the lowest R_{DSON} that is currently available. When feasible, the statistics pertain to the TO-247 package, which is the most widely used and all-purpose package for individual devices. According to observations made in 650 V SiC devices, they can resist higher currents and, consequently, powers than Si devices that have the same $R_{DS\text{-}ON}$ [27]. Additionally, they are comparable in terms of gate fees. They show lower input capacitance from a dynamics perspective, but larger rise/fall durations and delays. In comparison to 900 V Si MOSFETs, 1200 V SiC devices have noticeably lower R_{DSON}. They also function with more current and power than their 650 V counterparts.

Apart from single devices, there are modules that combine many devices. These devices are specifically made to improve heat dissipation and reduce parasitic effects, which are especially troublesome in high-frequency operations [28]. They aid in the achievement of a notable power density by facilitating high-voltage and -current activities. SiC MOSFETs and SiC power diodes, available in a range of configurations, including half-bridge, full-bridge, and chopper, are featured in these modules, enabling the application of many power topologies. They also have a variety of external parts, such as thermocouples or NTCs for monitoring operating temperatures [27]. The following are the most common detailed characteristics of SiC MOSFETS.

3.1. Gate-to-Source Voltage (V_{gs})

The V_{gs} of a SiC MOSFET is the voltage applied between the MOSFET's gate and source terminals. It controls whether the MOSFET is on or off. When V_{gs} exceeds the threshold voltage (Vth), the MOSFET turns on, allowing current to flow from drain to source. When the V_{gs} is below Vth or zero, the MOSFET turns off, preventing current flow.

Compared to Si-MOSFETs, SiC MOSFETs have a comparatively poor transconductance. As a result, to get the lowest V_{ds} saturation value at a high drain current, a greater gate-to-source voltage is needed. Low V_{ds} saturation is reached by Si-MOSFETs at 8 to 10 V on the gate to source. On the other hand, low V_{ds} saturation is usually achieved using SiC MOSFETs with a V_{gs} value of 15–20 V. When the SiC MOSFET is functioning as a variable resistance, a greater V_{gs} transition is needed to reach the turn-on threshold voltage. A negative V_{gs} level is necessary during turn-off due to the SiC MOSFET's quick switching speed and low turn-on threshold. For SiC devices, a drive of between -2 V and -5 V is advised, depending on the device [27–30].

3.2. Threshold Voltage Shift

One of the SiC MOSFET's appealing features is its strong gate threshold voltage stability under prolonged positive gate voltage application. After several hours, there is virtually little change in the threshold voltage; it stays constant. Nevertheless, the threshold shift may be greater than that brought on by a positive gate voltage if a continuous negative voltage is given to the gate for a longer amount of time; for example, the threshold may decrease by 0.5 V or more.

Maintaining threshold voltage stability is crucial for silicon MOSFETs. Significant variations in threshold voltage can impact switching behavior in multiple ways [29].

- Timing changes during switching because of the switch functioning in a regime that was not considered during design;
- Undesired conduction below the threshold;
- Inability to turn off.

Recent analyses [24–26] show that in some planar MOSFETs, as in Figure 2, a positive shift in the threshold voltage (Vth) is observed during the first stress phase. This shift is caused by electrons being trapped at interface/border traps at the SiO_2/SiC contact. The time dependency of this process is logarithmic, which is compatible with a self-limiting mechanism. As the stress duration grows, more electrons are repelled by the trapped electrons, which lowers the rate of trapping.

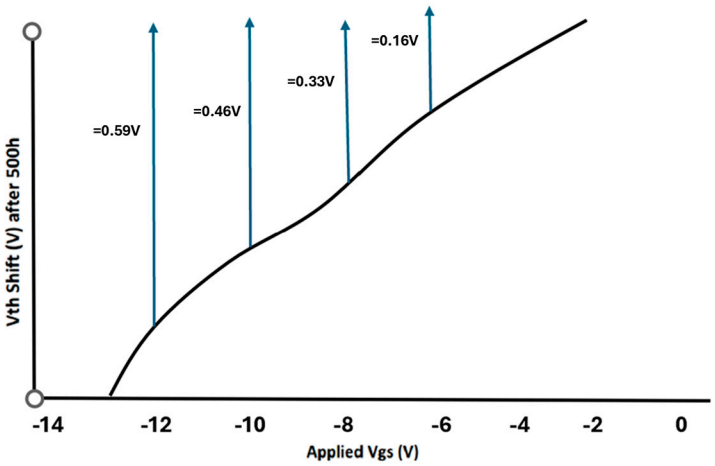


Figure 2. Example of behavior of Vth under 500 h of operation [24,26].

A negative shift in the threshold voltage (Vth) is observed in a later phase, and only over a crucial stress voltage threshold. Impact ionization inside oxide is thought to be the cause of this phenomenon, since it creates holes that are then re-trapped within the oxide. Rate equations have been used to explain the behavior of this secondary process, which has been seen to have an exponential time dependency [26]. A positive threshold voltage shift might enhance the device's on resistance and conduction loss. A negative threshold voltage shift may increase the chance of false turn-on and possibly shoot-through failure on the synchronous switch [31].

3.2.1. Threshold Voltage Shift Characteristics Under Fast Switching

In real-time switching applications, SiC MOSFETs alternate between ON and OFF states. This can produce a shift in the threshold voltage, known as a dynamic threshold voltage shift (DTVS) or Vth hysteresis. This effect is especially pronounced with high-speed switching. Recent research has recently explored how DTVS affects the reliability of SiC MOSFETs with time, ranging from nanoseconds [32] to microseconds (µs) to seconds [33]. An important consideration in Vth reliability measurements for SiC MOSFETs is the switching time, which is the period between shutting off the gate bias and beginning the operation.

According to [33], SiC MOSFETs exhibit large dynamic threshold voltage shifts during high-speed switching. Their findings show that with a gate bias of −10 V, the threshold voltage can vary by about −4 V, affecting switching behavior by increasing current overshoot and changing turn-on losses. This highlights the significance of knowing DTVS to improve the reliability of SiC MOSFETs in high-frequency applications. The study also includes ultrafast characterization methods, which provide important insights into transient voltage behavior.

The influence of high gate voltage (VGH) on threshold voltage (Vth) was studied by [34], where the gate voltage was changed from −5 V to three different levels: 15 V, 17.5 V, and 20 V. At the same time, the drain voltage was maintained at 100 volts. This study helped to clearly understand how varied gate voltage levels affect Vth over time, as shown in Figure 3.

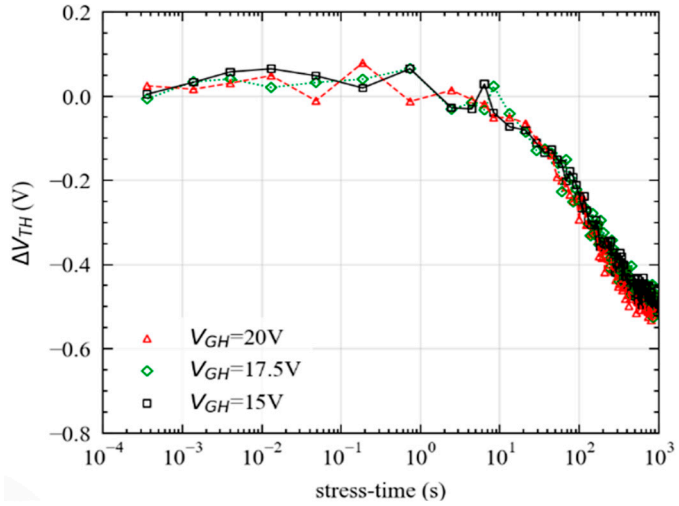


Figure 3. Vth drift during stress at different levels of high gate voltage (VGH) at stress time [34].

3.2.2. Threshold Voltage Shift Characteristics Under High Temperature

Ref. [35] explains how the gate oxide wears out when both electricity and temperature are applied. When the device is given a positive V_{gs}, the Vth shift does not change linearly with temperature and has a turning point caused by electron traps. According to [36], when the SiC MOSFET is biased at +25 and +30 V, the ΔVth initially falls and then increases with temperature, reaching a turning point at 200 °C. Electron traps have an increased effect on releasing charge between 150 °C and 200 °C. Above 200 °C, an accumulation of negative charge in the oxide becomes the dominant effect.

Semiconductor manufacturers constantly attempt to decrease defects in gate oxide. It was demonstrated in [37] that adding a heavily doped n-type channel layer to the MOSFET structure may help reduce changes in threshold voltage under stress. Furthermore, ref. [34] shows that gate-oxide technology may provide long-term durability at high temperatures if the stress on the gate oxide is managed at a reasonable level. It demands careful consideration when measuring gate drive voltages for each system.

Several studies have looked at how temperature influences the threshold voltage (Vth) shift in various semiconductor devices. In [38], it was discovered that when temperature falls, both mobility and Vth rise, but junction leakage current and off-state power consumption decrease. Similarly, Ref. [39] found that large Vth changes are visible at very high temperatures because of electron trapping during the poling process. According to [40], gate voltage and ambient temperature both increase the Vth shift. Furthermore, Ref. [41] showed that threshold changes caused by charge trapping alter the temperature dependency of gate leakage currents and ON-state resistance. In [42], it was discovered that reading data at a temperature other than writing can result in a significant number of failed bits, indicating a strong Vth temperature effect. These investigations illustrate the important role of temperature in Vth stability across various kinds of semiconductor devices.

3.3. ON Resistance of SiC MOSFET

The ON resistance ($R_{ds\text{-}ON}$) of a SiC MOSFET refers to the resistance between the drain and source when fully turned on. It determines how much power is lost to heat as current flows through the device. SiC MOSFETs have lower $R_{ds\text{-}ON}$ than silicon MOSFETs, which means they are more efficient, generate less heat, and perform better in high-power applications. However, $R_{ds\text{-}ON}$ might rise over time due to aging, heat stress, or avalanche occurrences, reducing the device's efficiency.

With respect to medium-power applications, the SiC MOSFET is a more attractive device because of its lower conduction resistance than the Si-MOSFET. It also has the capacity to

function well at greater temperatures and faster switching speeds [26]. A comparison of Si and SiC MOSFETs is shown in Figure 2, emphasizing the ON resistance with respect to the breakdown voltage. With a forward voltage drop of 3 V, or roughly five times that of a Si PN junction diode, the PiN diode makes up the SiC MOSFET body diode. However, in comparison to a Si PN diode, the reverse recovery time is significantly shorter [40].

Due to the extremely short practical switching times of SiC MOSFETs, even a tiny difference in the series-connected SiC MOSFET's switching speeds might cause significant voltage balance issues. Therefore, it is critical to comprehend the foundations of SiC MOSFETs to better grasp the voltage-sharing behavior amongst the series-connected devices [43].

SiC MOSFET devices are a good fit for medium-voltage power converters because of their exceptional performance and features. Rapid switching, however, can cause high dV/dt and/or di/dt and therefore high surge voltages, spike currents, high-frequency leakage currents, and other electromagnetic interference (EMI) problems in high-voltage applications [44,45].

4. The SiC MOSFET Failure Modes and Their Implications for Reliability

4.1. Gate Oxide Layer Failure

Within the field of semiconductor technology, for the past twenty years, research publications have consistently focused on the dependability of silicon carbide (SiC) metal-oxide semiconductor field effect transistor (MOSFET) gate oxides [46]. This ongoing debate mainly arises from the fact that SiC MOSFETs are different from their silicon (Si) counterparts in that the gate-oxide layer is thinner, and a stronger electric field is applied. One important characteristic that needs to be closely monitored in SiC MOSFETs is the high electric field, which is usually indicated by the maximum gate voltages of −20 V for the OFF state and +20 V for the ON state. Investigations involving the prolonged application of either of these voltages have shown that the threshold voltage rises with time [47]. This phenomenon has been described in the literature, underlining the need to understand the consequences of prolonged exposure to specific gate voltages. Although technical advancements, particularly in second-generation SiC MOSFETs, have reduced the impact slightly, a notable change of roughly 0.25 V is still predicted. For those researching and working in the field of semiconductor devices, this nuanced perspective provides essential insights into the development and contemporary difficulties concerning the dependability of SiC MOSFET gate oxides [48].

As-grown SiO_2 gate oxide on SiC has dense interface and bulk oxide traps. Additionally, the energy distribution of these traps is asymmetric, with a concentration in the top half of the band gap [49,50]. The suggested gate voltages for silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFETs) in the current semiconductor technological landscape are −5 V and +20 V. Though designers might be concerned with this direction, new studies have examined the complexities of extended exposure to high gate voltages and how they affect the threshold voltage. Studies show that when a high gate voltage is applied continuously over a lengthy period, the threshold voltage shifts noticeably [49]. When a strong electric field is applied, electrons flow through the oxide layer. When they reach the anode, some obtain enough energy to create impact ionization, which results in holes. These holes go back into the oxide but are easily trapped since they move much more slowly than electrons. This suggests hole trapping occurs more frequently in SiO_2. When the stress time exceeds one second, Vth starts shifting positively, eventually increasing. This shows that electron trapping takes place over hole trapping, and indicates the dominance of hole trapping in the SiO_2 caused by impact ionization, as shown in Figure 4.

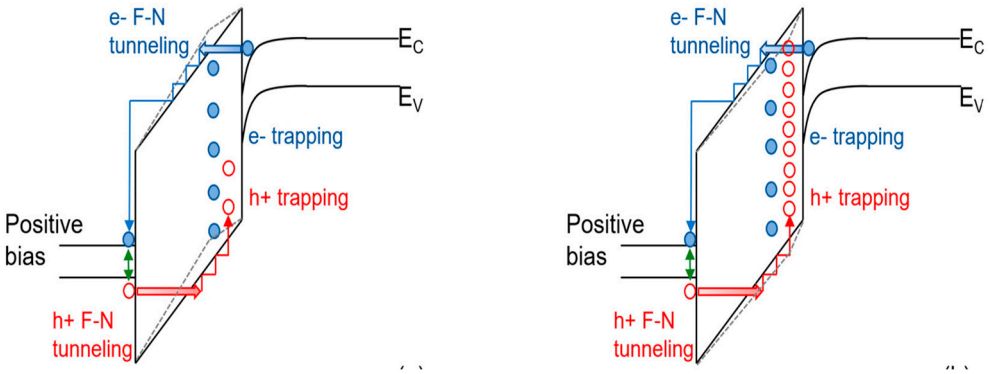


Figure 4. Electron- and hole-trapping dominance under positive gate bias [51].

This change, however, is reversible when the opposite gate voltage is applied. This dynamic is especially important in switched applications, where the gate voltage often changes between ON and OFF states.

In the study of semiconductor technology, manufacturers are constantly improving gate-oxide production procedures to reduce impurities in certain places. The trapped negative charge in the oxide decreases the mobile charge in the inversion layer, raises the threshold voltage, and limits mobility via Coulomb scattering. When the bias is reversed, the interface traps above the Fermi level rapidly depopulate, while the trapped charge in the oxide tunnels back to the SiC substrate. After post-oxidation annealing with NO, nitrogen atoms passivate the majority of the oxide and interface defects, minimizing transient trapping. As a result, the channel carrier density is greatly increased, the threshold voltage is reduced, and field-effect mobility increases.

4.2. Body Diode Failure

A critical reliability concern is the deterioration of the body diode, which is based on a PN junction. The deterioration is the result of the creation of basal-plane dislocations. Improving the material's epitaxial quality is important to overcome this problem [49,50]. According to research published in [52,53], the performance of the body diode declines when exposed to continuous forward current. This deterioration emerges as increasing forward voltage, which leads to greater power dissipation during conduction at a given current level. These findings highlight the significance of knowing the behavior of the body diode, particularly its implications for MOSFET designs and operating efficiency in a variety of circuit topologies.

Traditionally, this problem is solved by implementing a silicon carbide (SiC) Schottky barrier diode (SBD). In comparison to other diodes, this one has a lower forward voltage and a faster recovery time [54,55]. By adding an SBD, the system's flyback current management pathway is diversified, hence reducing the body diode's deterioration. Figure 5 [37] compares the reverse recovery properties of 650 V SiC planar, trench, and cascode devices to a silicon super-junction MOSFET. The SiC MOSFETs show superior body diode performance, with a decreased peak negative current. Overall, SiC devices perform better than silicon SJ MOSFETs, but the best option depends on the application's switching frequency.

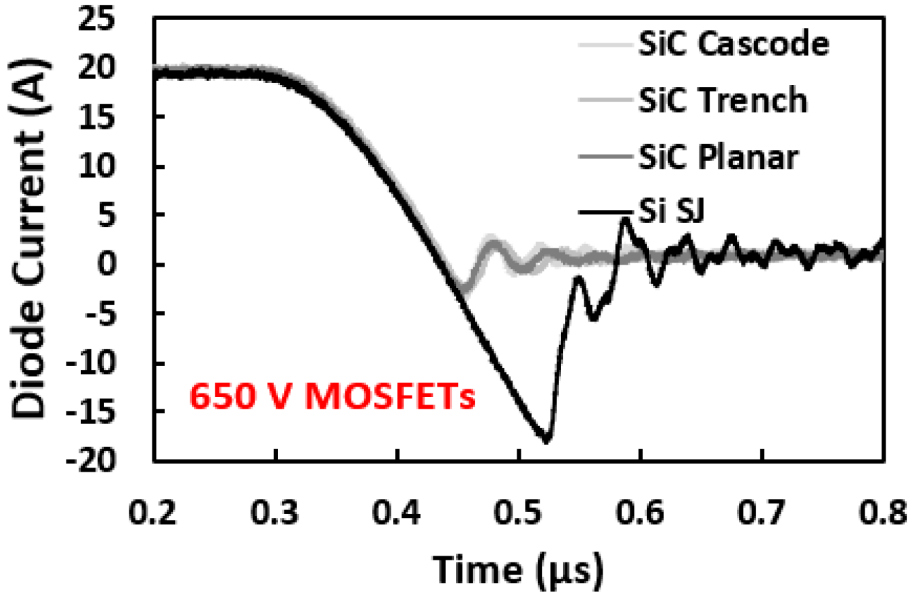


Figure 5. Body diode switching characteristics for 650 V MOSFETs [37].

But it is important to remember that this approach has a price, namely, the need for more SiC substrate, which raises the SiC MOSFET's production costs overall. As demonstrated in [56], the addition of an n-type channel layer has proved useful in improving the dependability of a SiC MOSFET, notably in terms of gate threshold voltage changes. Furthermore, the introduction of this layer provides an alternate channel for reverse currents, successfully protecting the body diode from deterioration. The extra cost that comes with the proposed design is less expensive than the other method, which adds a second Schottky barrier diode (SBD). This is explained by the fact that the MOSFET design naturally incorporates the n-type channel layer, removing the requirement for an additional silicon carbide (SiC) substrate.

Another solution, the quality of SiC epitaxial growth, is critical in avoiding reliability concerns like body diode deterioration in SiC MOSFETs. Defects generated during epitaxial development can increase forward voltage drop and power dissipation in the body diode, accelerating its degradation over time:

Simulation-Based Optimization: Traditional trial-and-error approaches for optimizing SiC epitaxial growth are time-consuming and expensive. To overcome this, simulation methods have been developed to efficiently optimize growth parameters [57].

High Growth Rates with Trichlorosilane (TCS): Research has shown that using TCS as a silicon precursor allows for high epitaxial growth rates in 4H-SiC. Optimal epilayers were obtained at 1600 °C, with a TCS flow rate of 12 sccm and a C/Si ratio of 0.42, resulting in satisfactory surface morphology [58].

Step-Controlled Epitaxy: Recent advancements in silicon carbide (SiC) epitaxial growth have concentrated on refining approaches to improve material quality and device performance. A major advancement is the step-controlled epitaxy approach, which allows for the creation of single-phase SiC crystals by precisely manipulating the substrate's surface steps during the chemical vapor deposition process. This approach has proved useful in creating high-quality epitaxial layers with fewer flaws, which improves the performance of SiC-based devices [59].

Buffer-Layer Utilization: Implementing a $Si_{1-X}Ge_X$ buffer layer between the Si substrate and the SiC epitaxial layer has been found to reduce defects and improve the overall quality of the SiC epi-film. Optimizing the carbonization temperature and Ge concentration is crucial for achieving these improvements [60].

Large-Area Uniform Graphene Growth: By optimizing the temperature field during the thermal breakdown of 4H-SiC, large-area uniform monolayer epitaxial graphene may be produced, which is useful in a variety of applications [61].

Researchers can decrease flaws in body diodes by improving epitaxial growth techniques like step-controlled epitaxy and buffer-layer use. This results in increased diode reliability, lower conduction losses, and better long-term performance for SiC-based power devices.

4.3. Gate Leakage Current Failure

A switching device needs to tolerate short-circuit currents that are up to 10 times the rated current for a short period of time, especially if the application is included in a safety mechanism like a DC circuit breaker [58]. Similarly, silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are expected to withstand difficult switching circumstances, needing careful consideration of the pressures applied to the device. The voltage and current waveforms of a 1200 V 150 A SiC MOSFET under the pulse test settings in [62] describes the device experiencing peak currents of 600 A, which is equal to four times its nominal rating. According to the findings of [62], when a short circuit occurs, the whole DC bus voltage manifests itself across the semiconductor device. This phenomenon causes the introduction of an electric field, which, at sufficiently high levels, initiates a reach-through effect. This effect causes increased leakage currents from the gate to the source. It is critical to note that the gate-oxide-layer thickness in SiC MOSFETs is lower than that of Si MOSFETs, making them more vulnerable to the impact.

When a short-circuit event occurs, the device temperature rises, which causes further leakage currents to appear. As a result, this phenomenon causes the gate oxide to deteriorate, as the forced leakage current passes through this layer that is situated between the device's gate and source [53,63].

To conclude the numerical thresholds for acceptable leakage levels before failure, the key findings are summarized below:

Gate Leakage Current as a Failure Indicator: A study provided an efficient screening method based on the relationship between initial gate leakage current and oxide failure time at a constant gate voltage. The study implies that monitoring early gate leakage could be used to predict oxide reliability [64].

Gate Leakage Current Thresholds in Degradation Monitoring: In SiC MOSFET condition monitoring, a large gate leakage current is required for the estimate to exceed the threshold level, indicating MOSFET degeneration. According to the study, a threshold level of estimated leakage may be set as low as 3 mA without causing a false-positive monitoring signal [65].

Gate Leakage Current in Short-Circuit Events: According to Ref. [64], SiC MOSFETs can break down in few microseconds owing to thermal runaway or gate failure during short-circuit events. This emphasizes the necessity of understanding gate leakage behavior in these kinds of conditions.

Impact of Load Current on Gate Leakage Current Failure

According to studies, when the load current increases, so does the stress on the gate-oxide layer, resulting in faster deterioration. This causes an increase in gate leakage current, which can have a major impact on the device's reliability and performance. For example, ref. [66] discovered that higher load currents under high-temperature environments pushed faster deterioration of the gate oxide, resulting in increased leakage currents and changes in the threshold voltage. Ref. [67] determined how the load current influences gate-oxide reliability in SiC MOSFETs by evaluating the effect of the active channel. It was discovered that applying high-load currents had significant effects on the performance of the gate oxide, increasing its deterioration. According to the study, the active channel in the SiC MOSFET has

a significant influence on how the load current affects gate-oxide deterioration. According to the research, greater load currents cause more electrical stress on the gate oxide, increasing the risk of oxide wear and, as a result, increasing gate leakage current. This study underlines the need for careful design and operational management to minimize the impact of load currents on gate-oxide integrity.

Ref. [68] includes experimental data that tell how different operating circumstances are, including load currents and change gate leakage currents. It was found that increasing load current could increase gate leakage currents, especially at high gate voltages. As the load current increases, so does the stress on the gate oxide, resulting in increased electron migration and quicker degradation of the oxide layer.

When load currents are high, they accelerate the degradation of the gate oxide, leading to an increase in gate leakage currents.

4.4. Avalanche Events Causing Failure

An avalanche event is characterized by a voltage spike that exceeds the device's breakdown voltage. This allows current to pass through the MOSFET, resulting in power dissipation and a rapid increase in internal temperature [69].

An avalanche event is more likely to occur in designs that include switching current via an inductive circuit, as shown in Figure 6 [70]. This event results from the energy stored in the inductive load, which, when released, causes a voltage spike that exceeds the switching device's breakdown voltage.

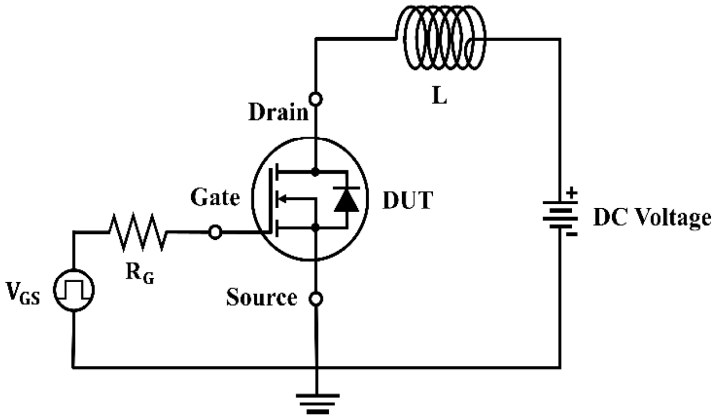


Figure 6. UIS test circuit for avalanche testing of SiC MOSFETs [70].

Since the stored energy is transmitted to the load, much thought goes into making sure that the device's voltage rating is greater than the expected voltage spike in traditional inductive switching designs, such as those seen in flyback converters [63]. However, there are situations in which stray inductances in current channels and other similar components expose electronics to unanticipated voltage spikes. On the other hand, an avalanche state is foreseen in certain conditions, such as regenerative braking, and is appropriately taken into consideration during the design phase.

The fact that the current passing through the device at the time of the event causes deterioration in the material layers of the current route is extremely important. This deterioration shows up as a quantifiable impact and raises the device's Rds(on) value. This deterioration is sustained by more avalanche occurrences, which raise the Rds(on) value over time. The ensuing consequence is that the device's power dissipation increases when it is turned on, requiring more cooling techniques to maintain a safe working temperature. It is necessary to foresee and account for this increased power dissipation at the system design stage by including additional cooling devices to handle the steady rise over time.

Figure 6 [70] shows the test circuit for unclamped inductive switching (UIS), used to evaluate the avalanche reliability of the SiC MOSFET. Even though avalanche occurrences are not unique to SiC-based systems, they are nonetheless very important in determining the design's overall dependability, especially considering how common power electronics are in today's world [71].

4.4.1. Impact of Avalanche Events on ON Resistance Causing Failure

Avalanche events in silicon carbide (SiC) MOSFETs can significantly reduce device performance, notably due to an increase in ON resistance. This deterioration is mostly due to damage to the gate-oxide layer and changes in the device's internal structure caused by the high-energy conditions seen during avalanche breakdowns.

Ref. [72] found that after having high-energy dynamic avalanche events, SiC MOSFETs showed higher ON resistance due to damage in the gate oxide and the development of traps in the semiconductor, which restricted electron mobility. In their experiments, they found a significant increase in ON resistance after recurrent avalanche stress. Similarly, ref. [73] shows that frequent avalanche breakdown events damage the gate oxide in SiC MOSFETs, resulting in worse switching performance and higher ON resistance.

Ref. [74] indicated a significant rise in ON resistance following exposure to recurrent avalanche stress, which was related to the permanent creation of flaws in the gate-oxide layer. Furthermore, ref. [75] found that the cumulative influence of avalanche occurrences resulted in an increase in ON resistance, especially when subjected to high-voltage overcurrent pulses. These experimental results show a strong link between avalanche events and higher ON resistance, emphasizing the need to address avalanche stress when designing SiC MOSFETs for high-power applications. The loss in performance caused by increasing ON resistance is a crucial aspect in deciding the device's long-term reliability.

4.4.2. Environmental Effects on Reliability of SiC MOSFET

Research on silicon carbide (SiC) MOSFETs often emphasizes their improved electrical qualities over typical silicon (Si) MOSFETs. However, it is critical to evaluate how these devices operate in real-world environments, such as humidity, mechanical stress, and radiation exposure, particularly in demanding applications such as aerospace and industry.

Humidity effects: Humidity significantly affects the reliability and performance of silicon carbide (SiC) MOSFETs. Exposure to high-humidity environments can cause a negative shift in the devices' threshold voltage, as well as a drop in maximum transconductance and drain current. The degradation is caused by moisture-induced corrosion of metal contacts and interconnects, which increases device resistance [76]. Furthermore, studies show that thermo-mechanical stress caused by power cycling could accelerate humidity-induced degradation. Thermal stress can cause delamination and micro-cracks, which can allow moisture to enter and compromise device integrity [51]. In addition, prolonged exposure to high-humidity and -temperature conditions has been shown to cause corrosion in SiC devices, which stresses the importance of complete humidity robustness validation in design and application [77].

Temperature effects: Temperature has an important impact on the performance and reliability of silicon carbide (SiC) MOSFETs. Elevated temperatures can cause a rise in ON resistance, which results in larger conduction losses [78]. On commercial SiC power MOSFETs, significant changes in device properties over 125 °C were found. In addition, [77], which compared temperature-sensitive electrical properties of SiC MOSFETs at extremely high temperatures, showed the devices' capacity to operate under such conditions, stressing the need to understand temperature-dependent behaviors [79]. Analyzing the thermal performance of SiC MOSFETs under various situations showed that thermal management is crucial, as the

maximum junction temperature decreased by over 31.7 °C and the junction temperature swing decreased by 46%.

Mechanical Stress: Ref. [80] investigated SiC MOSFET failure processes during short-circuit events, indicating that these devices face significant electrical, thermal, and mechanical stresses. The findings showed that the combined effects of high temperature and mechanical stress degrade the gate oxide and increase leakage currents, ultimately leading to device failure. The study highlighted the need for better device packaging and stress-reduction approaches to improve SiC MOSFET reliability. Another study [81] investigated the combined electrical, thermal, and mechanical stress in SiC MOSFETs during short-circuit periods. The study presented improved test methodologies for assessing failure modes and reliability limits in 4H-SiC power MOSFETs. The findings showed that excessive mechanical stress accelerates degradation, especially when paired with numerous high-power switching events. This study concluded that thorough stress analysis and enhanced heat management measures are required to increase devices' life. Furthermore, ref. [82] investigated the degradation of SiC MOSFETs under accelerated stress in power-factor correction (PFC) converters. Using an online monitoring system, Ref. [83] found that mechanical stress from repetitive power cycling resulted in greater threshold voltage changes and growing ON resistance (RDS(on). Ref. [84] found that packaging-induced mechanical stress causes a huge performance decline, requiring more effective mechanical design and stress-reducing materials.

5. Conclusions and Future Directions

A thorough examination of silicon carbide (SiC) MOSFETs, including their failure mechanisms, reliability issues, and benefits over conventional silicon-based devices, has been presented in the review article. SiC MOSFETs are perfect for high-power and high-temperature applications because of their wide-bandgap (WBG) characteristics, which provide notable gains in power efficiency, thermal performance, and operational stability. SiC MOSFETs are superior in certain ways due to their unique material characteristics, but these qualities also present special reliability issues that must be resolved before SiC MOSFETs are widely used.

While earlier generations of SiC MOSFETs had significant advantages in terms of power efficiency and high-temperature operation, later advances in device design have improved their performance even further. The latest generation of SiC MOSFETs have lower ON resistance, better short-circuit-withstanding capabilities, and improved switching properties, making them more appropriate for high-power and high-frequency applications. Furthermore, current research into material optimization, packaging methods, and failure mitigation tactics solves reliability challenges, providing long-term stability under harsh environmental conditions. As SiC MOSFETs are of interest in many kinds of industries, including automotive, aerospace, and renewable energy, future developments will most likely focus on further decreasing power losses, increasing efficiency, and improving robustness to meet the growing demands of next-generation power electronics.

This study has covered in detail key failure processes, including high-temperature device deterioration, threshold voltage instability, and gate-oxide degradation. The study emphasizes that even while SiC MOSFETs have advanced significantly, especially in the areas of material quality and device design, further research is necessary to address the reliability issues that still exist.

Despite the progress made in SiC MOSFET technology, further research is necessary in a few areas to improve the dependability and efficiency of these devices:

1. Improved Material Characterization: Future studies should concentrate on creating more sophisticated methods to identify flaws in SiC materials, especially those affect-

ing the junctions and gate oxide. More resilient SiC MOSFETs may result from our growing understanding of the atomic-level nature and behavior of these flaws.

2. Dependability in Adverse Environments: Further investigation is required to determine the long-term dependability of SiC MOSFETs in adverse environments, including intense radiation, extremely high temperatures, and high-frequency operations. This is especially significant given their use in the military, aerospace, and other vital industries.
3. Better Device Architecture: Some of the existing reliability problems may be resolved by more device architecture innovation, such as the creation of innovative gate architectures and passivation layers. Investigating novel materials for passivation and gate oxides may potentially provide answers to the SiC MOSFET deterioration issues.
4. Packaging and Thermal Management: Another critical area for future study is the development of sophisticated packaging methods that can withstand the greater thermal loads associated with SiC MOSFETs. Reaching the maximum potential of SiC devices in high-power applications would require effective thermal control.
5. Integration with Developing Technologies: New avenues for power electronics may be created by combining SiC MOSFETs with other developing technologies, such as wide-bandgap semiconductors like gallium nitride (GaN). The development of hybrid systems that combine the advantages of GaN and SiC may result in devices with previously unheard-of performance levels.

To summarize, SiC MOSFETs provide notable benefits over conventional silicon-based devices and constitute a substantial advancement in the field of power electronics. However, resolving the dependability issues mentioned in this study is necessary for their acceptance. To ensure SiC MOSFETs' role in power electronics going forward and to fully realize their potential, more research and development in the aforementioned areas is necessary.

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References

1. Thakur, A.; Kumari, S. A comprehensive review of wide band-gap semiconductors technology. *Int. J. Adv. Res. Innov. Ideas Educ.* **2023**, *9*, 417–422.
2. Ning, T.; Yuan, Y.; Kang, C.; Li, H.L. Review of Si IGBT and SiC MOSFET based on hybrid switch. *Chin. J. Electr. Eng.* **2019**, *5*, 20–29. [CrossRef]
3. Alves, L.F.S.; Gomes, R.C.M.; Lefranc, P.; De Alves Pegado, R.; Jeannin, P.; Luciano, B.A.; Rocha, F.V. Sic Power Devices in Power Electronics: An Overview. In Proceedings of the Brazilian Power Electronics Conference (COBEP), Juiz de Fora, Brazil, 19–22 November 2017; pp. 1–8.
4. Zhang, J. Power Electronics in Future Electrical Power Grids. In Proceedings of the IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Little Rock, AR, USA, 8–11 July 2013; pp. 1–3.
5. Agarwal, A.K. An Overview of Sic Power Devices. In Proceedings of the International Conference on Power, Control and Embedded Systems, Allahabad, India, 29 November–1 December 2010; pp. 1–4.
6. Shenai, K.; Scott, R.S.; Baliga, B.J. Optimum semiconductors for high-power electronics. *IEEE Trans. Electron Devices* **1989**, *36*, 1811–1823. [CrossRef]
7. Xue, H.; He, Q.; Jian, G.; Long, S.; Pang, T.; Liu, M. An overview of the ultrawide bandgap Ga_2O_3 semiconductor-based schottky barrier diode for power electronics application. *Nanoscale Res. Lett.* **2018**, *13*, 12. [CrossRef] [PubMed]

8. Zhang, H.; Tolbert, L.M. Efficiency impact of silicon carbide power electronics for modern wind turbine full scale frequency converter. *IEEE Trans. Ind. Electron.* **2011**, *58*, 21–28. [CrossRef]
9. Chen, X.; Yang, X.; Xie, X.; Peng, Y.; Xiao, L.; Chen, S.; Li, H.; Hu, X.; Xu, X. Research progress of large size SiC single crystal materials and devices. *Light Sci. Appl.* **2023**, *12*, 28. [CrossRef]
10. He, Y.; Moore, D.C.; Wang, Y.; Ware, S.; Ma, S.; Pradhan, D.K.; Hu, Z.; Du, X.; Kennedy, J.; Glavin, N.R.; et al. Al0. 68Sc0. 32N/SiC based metal-ferroelectric-semiconductor capacitors operating up to 900 C. *arXiv* **2024**, arXiv:2411.16652.
11. Wang, R.; Boroyevich, D.; Ning, P.; Wang, Z.; Wang, F.; Mattavelli, P.; Ngo, K.T.D.; Rajashekara, K.A. high-temperature SiC three-phase AC-DC converter design for >100°C ambient temperature. *IEEE Trans. Power Electron.* **2013**, *28*, 555–572. [CrossRef]
12. Zhang, L.; Zheng, Z.; Lou, X. A review of WBG and Si devices hybrid applications. *Chin. J. Electr. Eng.* **2021**, *7*, 1–20. [CrossRef]
13. Langpoklakpam, C.; Liu, A.-C.; Chu, K.-H.; Hsu, L.-H.; Lee, W.-C.; Chen, S.-C.; Sun, C.-W.; Shih, M.-H.; Lee, K.-Y.; Kuo, H.-C. Review of Silicon Carbide Processing for Power MOSFET. *Crystals* **2022**, *12*, 245. [CrossRef]
14. Glass, R.C.; Henshall, D.; Tsvetkov, V.F.; Carter, C.H., Jr. SiC-seeded crystal growth. *MRS Bull.* **1997**, *22*, 30. [CrossRef]
15. Tsvetkov, V.F.; Allen, S.T.; Kong, H.S.; Carter, C.H., Jr. Recent Progress in SiC Crystal Growth. In Proceedings of the International Conference on Silicon Carbide and Related Materials, Tsukuba, Japan, 28 October–2 November 1995; Volume 7, pp. 73–84.
16. ROHM Semiconductor. Application Note for Sic Power Devices and Modules. Rev.003. 2014. Available online: https://fscdn.rohm.com/en/products/databook/applinote/discrete/sic/common/sic_appli-e.pdf (accessed on 25 February 2025).
17. Marcuzzi, A.; Favero, D.; Santi, C.D.; Meneghesso, G.; Zanoni, E.; Meneghini, M. A Review of SiC Commercial Devices for Automotive: Properties and Challenges. In Proceedings of the International Conference on Electrical and Electronic Technologies for Automotive (AEIT AUTOMOTIVE), Modena, Italy, 17–19 July 2023; pp. 1–6.
18. Liu, T.; Zhu, S.; White, M.H.; Salemi, A.; Sheridan, D.; Agarwal, A.K. Time-Dependent Dielectric Breakdown of Commercial 1.2 kV 4H-SiC Power MOSFETs. *IEEE J. Electron Devices Soc.* **2021**, *9*, 633–639. [CrossRef]
19. Masin, F.; De Santi, C.; Lettens, J.; Franchi, J.; Domeji, M.; Moens, P.; Meneghini, M.; Meneghesso, G.; Zanoni, E. non-monotonic threshold voltage variation in 4H-SiC metal–oxide semiconductor field-effect transistor: Investigation and modeling. *J. Appl. Phys.* **2021**, *130*, 14. [CrossRef]
20. Zheng, Y.; Potera, R.; Witt, T. Characterization of Early Breakdown of SiC MOSFET Gate Oxide by Voltage Ramp Tests. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, 21–25 March 2021.
21. Wang, J.; Zhao, T.; Li, J.; Huang, A.Q.; Callanan, R.; Husna, F.; Agarwal, A. Characterization, modeling, and application of 10-kv sic mosfet. *IEEE Trans. Electron Devices* **2008**, *55*, 1798–1806. [CrossRef]
22. Whitaker, B.; Passmore, B.; McNutt, M.T.; Lostetter, A.; Ericson, M.N.; Shane, S.; Charles, F.; Britton, L.; Mantooth, A.; Lamichhane, R.; et al. High-Temperature SiC Power Module with Integrated SiC Gate Drivers for Future High-Density Power Electronics Applications. In Proceedings of the IEEE Workshop on Wide Bandgap Power Devices and Applications, Knoxville, TN, USA, 13–15 October 2014; pp. 36–40.
23. Funaki, T.; Balda, J.C.; Junghans, J.; Kashyap, A.S.; Mantooth, H.A.; Barlow, F.; Kimoto, T.; Hikihara, T. Power conversion with SiC devices at extremely high ambient temperatures. *IEEE Trans. Power Electron.* **2007**, *22*, 1321–1329. [CrossRef]
24. Abou-Alfotouh, A.M.; Radun, A.V.; Chang, H.; Winterhalter, C. A 1-MHz hard-switched silicon carbide DC–DC converter. *IEEE Trans. Power. Electron.* **2006**, *21*, 880–889. [CrossRef]
25. Wrzecionko, B.; Bortis, D.; Kolar, J.W. A 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system. *IEEE Trans. Power Electron.* **2014**, *29*, 2345–2358. [CrossRef]
26. Rabkowski, J.; Peftitsis, D.; Nee, H.P. Parallel-operation of discrete SiC BJTs in a 6-kW/250-kHz DC/DC boost converter. *IEEE Trans. Power Electron.* **2014**, *29*, 2482–2491. [CrossRef]
27. Whitaker, B.; Barkley, A.; Cole, Z.; Passmore, B.; Martin, D.; McNutt, T.; Lostetter, A.; Lee, J.; Shiozaki, K. A high-density, high-efficiency, isolated on-board vehicle battery charger utilizing silicon carbide power devices. *IEEE Trans. Power Electron.* **2014**, *29*, 2606–2617. [CrossRef]
28. Liang, Z. Status and Trends of Automotive Power Module Packaging. In Proceedings of the International Symposium on Power Semiconductor Devices and Ics, Bruges, Belgium, 3–7 June 2012; pp. 325–331.
29. Millan, J. A review of WBG Power Semiconductor Devices. In Proceedings of the International Semiconducter Conference (CAS), Sinaia, Romania, 15–17 October 2012; pp. 57–66.
30. Agarwal, A.; Callanan, R.; Das, M.; Hull, B.; Richmond, J.; Ryu, S.-H.; Palmour, J. Advanced HF SiC MOS devices. In Proceedings of the European Conference on Power Electronics and Applications, Barcelona, Spain, 8–10 September 2009; pp. 5952–5961.
31. Gonzalez, J.O.; Alatise, O. Impact of BTI-induced threshold voltage shifts in shoot-through currents from crosstalk in SiC MOSFETs. *IEEE Trans. Power Electron* **2021**, *36*, 3279–3291. [CrossRef]
32. Puschkarsky, K.; Grasser, T.; Aichinger, T.; Gustin, W.; Reisinger, H. Understanding and Modeling Transient Threshold Voltage Instabilities in SiC MOSFETs. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Burlingame, CA, USA, 11–15 March 2018; pp. 1–10. [CrossRef]

33. Jiang, J.; Tang, X.; Tan, K.; Hu, Z.; Tian, M.; Xu, Y.; Li, H.; Zhu, W.; Li, H.; Hu, C.; et al. Characterization of Threshold Voltage Shift in SiC MOSFETs Under Nanosecond-Range Switching and Its Impact on High- Frequency Applications. *IEEE Trans. Electron Devices* **2024**, *71*, 4227–4232. [CrossRef]
34. Cioni, M.; Bertacchini, A.; Mucci, A.; Zagni, N.; Verzellesi, G.; Pavan, P.; Chini, A. Evaluation of Vth and R_{ON} Drifts during Switch-Mode Operation in Packaged SiC MOSFETs. *Electronics* **2021**, *10*, 441. [CrossRef]
35. Suganuma, K. *: Wide Bandgap Power Semiconductor Packaging: Materials, Components, and Reliability (Woodhead Publishing Series in Electronic and Optical Materials)*; Woodhead Publishing: Sawston, UK, 2018.
36. Chen, C.; Cai, Y.; Sun, P.; Zhao, Z. Threshold voltage instability of SiC MOSFETs under very-high temperature and wide gate bias. *IET Power Electron.* **2024**, *17*, 2393–2404. [CrossRef]
37. Alatise, O.; Deb, A.; Bashar, E.; Ortiz Gonzalez, J.; Jahdi, S.; Issa, W. A Review of Power Electronic Devices for Heavy Goods Vehicles Electrification: Performance and Reliability. *Energies* **2023**, *16*, 4380. [CrossRef]
38. Santini, T.; Sebastien, M.; Florent, M.; Phung, L.V.; Bruno, A. Gate Oxide Reliability Assessment of a SiC MOSFET for High Temperature Aeronautic Applications. In Proceedings of the IEEE ECCE Asia Downunder-5th IEEE Annual International Energy Conversion Congress Exhibition, Melbourne, Australia, 3–6 June 2013; pp. 385–391.
39. Goel, N.; Tripathi, A. Temperature effects on Threshold Voltage and Mobility for Partially Depleted SOI MOSFET. *Int. J. Comput. Appl.* **2012**, *42*, 21.
40. Shivendra, K.; Rathaur, A.D.; Chang, E.Y. Impact of temperature on threshold voltage instability under negative bias in ferroelectric charge trap (FEG) GaN-HEMT. *Appl. Phys. Lett.* **2024**, *125*, 102–104. [CrossRef]
41. Poli, S.; Reggiani, S.; Denison, M.; Ghani, E.; Gnudi, A.; Baccarani, G. Temperature Dependence of the Threshold Voltage Shift Induced by Carrier Injection in Integrated STI-Based LDMOS Transistors. *IEEE Electron Device Lett.* **2011**, *32*, 791–793. [CrossRef]
42. Etoz, B.; Gonzalez, J.O.; Deb, A.; Jahdi, S.; Alatise, O. Impact of Threshold Voltage Shifting on Junction Temperature Sensing in GaN HEMTs. In Proceedings of the 24th European Conference on Power Electronics and Applications (EPE'22 ECCE Europe), Hanover, Germany, 5–9 September 2022; pp. P.1–P.9.
43. Ho, C.N.-M.; Breuninger, H.; Pettersson, S.; Escobar, G.; Canales, F. A comparative performance study of an interleaved boost converter using commercial Si and SiC diodes for PV applications. *IEEE Trans. Power Electron.* **2013**, *28*, 289–299. [CrossRef]
44. Lostetter, A.; Hornberger, J.; McPherson, B.; Reese, B.; Shaw, R.; Schupbach, M.; Rowden, B.; Mantooth, A.; Balda, J.; Otsuka, T.; et al. High-temperature silicon carbide and silicon on insulator based integrated power modules. In Proceedings of the 2009 IEEE Vehicle Power and Propulsion Conference, Dearborn, MI, USA, 7–10 September 2009; pp. 1032–1035.
45. Wood, R.A.; Salem, T.E. Evaluation of 1200-V, 800-A All-SiC Dual Module. *IEEE Trans. Power Electron.* **2011**, *26*, 2504–2511. [CrossRef]
46. Horio, M.; Iizuka, Y.; Ikeda, Y. Packaging technologies for SiC power modules. *Fuji Electr. Rev.* **2011**, *58*, 75–80.
47. Schorner, R.; Friedrichs, P.; Peters, D.; Stephani, D. Significantly improved performance of MOSFETs on silicon carbide using the 15RSiC polytype. *IEEE Electron Device Lett.* **1999**, *20*, 241–244.
48. Gurfinkel, M.; Xiong, H.D.; Cheung, K.P.; Suehle, J.S.; Bernstein, J.B.; Shapira, Y. Characterization of Transient Gate Oxide Trapping in SiC MOSFETs Using Fast I–V Techniques. *IEEE Trans. Electron Devices* **2008**, *55*, 2004–2012. [CrossRef]
49. Li, D.; Zhang, Y.; Tang, X.; He, Y.; Yuan, H.; Jia, Y.; Song, Q.; Zhang, M.; Zhang, Y. Effects of 5 MeV Proton Irradiation on Nitrided SiO_2/4H-SiC MOS Capacitors and the Related Mechanisms. *Nanomaterials* **2020**, *10*, 1332. [CrossRef] [PubMed]
50. Dasa, M.K.; Sumakeris, J.J.; Hull, B.A.; Richmond, J. Evolution of Drift-Free, High Power 4H-SiC PiN Diodes. *Mater. Sci. Forum* **2006**, *527–529*, 1329–1334. [CrossRef]
51. Shi, L.; Qian, J.; Jin, M.; Bhattacharya, M.; Houshmand, S.; Yu, H.; Shimbori, A.; White, M.H.; Agarwal, A.K. Gate Oxide Reliability in Silicon Carbide Planar and Trench Metal-Oxide-Semiconductor Field-Effect Transistors Under Positive and Negative Electric Field Stress. *Electronics* **2024**, *13*, 4516. [CrossRef]
52. Dasgupta, S.; Kaplar, R.J.; Marinella, M.J.; Smith, M.A.; Atcitty, S. Analysis and Prediction of Stability in Commercial, 1200 V, 33A, 4H-SiC MOSFETs. In Proceedings of the IEEE International Reliability Physics Symposium, Anaheim, CA, USA, 15–19 April 2012. pp. 3D.3.1–3D.3.5.
53. Wang, Z.; Shi, X.; Xue, Y.; Tolbert, L.M.; Wang, F.; Blalock, B.J. Design and performance evaluation of overcurrent protection schemes for silicon carbide (SiC) power MOSFETs. *IEEE Trans. Ind. Electron.* **2014**, *61*, 5570–5581. [CrossRef]
54. She, X.; Huang, A.Q.; Lucía, Ó.; Ozpineci, B. Review of silicon carbide power devices and their applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 8193–8205. [CrossRef]
55. Adamowicz, M.; Giziewski, S.; Pietryka, J.; Krzeminski, Z. Performance Comparison of SiC Schottky Diodes and Silicon Ultra Fast Recovery Diodes. In Proceedings of the 7th International Conference-Workshop Compatibility and Power Electronics (CPE), Talinn, Estonia, 1–3 June 2011; pp. 144–149.
56. Ranstad, P.; Nee, H.P. On dynamic effects influencing IGBT losses in soft-switching converters. *IEEE Trans. Power Electron* **2011**, *26*, 260–271. [CrossRef]

57. Wu, D.; You, H.; Wang, X.; Zhong, S.; Sun, Q. Experimental Investigation of Threshold Voltage Temperature Effect During Cross-Temperature Write–Read Operations in 3-D NAND Flash. *IEEE J. Electron Devices Soc.* **2021**, *9*, 22–26. [CrossRef]
58. Tian, J.; Tang, Z.; Tang, H.; Fan, J.; Zhang, G. Simulation of Epitaxial Growth of Silicon Carbide in a Horizontal Hot-wall CVD Reaction Chamber. In Proceedings of the 20th China International Forum on Solid State Lighting & 9th International Forum on Wide Bandgap Semiconductors, Xiamen, China, 27–30 November 2023; pp. 14–17. [CrossRef]
59. Gang, J.; Sun, G.S.; Ning, J.; Kiu, X.F.; Zhao, Y.M.; Wang, L.; Zhao, W.S.; Zeng, Y.P.; Ji, G. High epitaxial growth rate of 4H-SiC using TCS as silicon precursor. In Proceedings of the 9th International Conference on Solid-State and Integrated-Circuit Technology, Beijing, China, 20–23 October 2008; pp. 696–698. [CrossRef]
60. Suda, J. SiC and GaN from the viewpoint of vertical power devices. In Proceedings of the 74th Annual Device Research Conference (DRC), Newark, DE, USA, 19–22 June 2016; p. 1. [CrossRef]
61. Zimbone, M.; Zielinski, M.; Barbagiovanni, E.G.; Calabretta, C.; Via, F.L. 3C-SiC grown on Si by using a Si1-xGex buffer layer. *J. Cryst. Growth* **2019**, *519*, 29. [CrossRef]
62. Schrock, J.A.; Ray, W.B.; Lawson, K.; Bilbao, A.; Bayne, S.B.; Holt, S.L.; Cheng, L.; Palmour, J.W.; Scozzie, C. High-mobility stable 1200-V, 150-A 4H-SiC DMOSFET long-term reliability analysis under high current transient conditions. *IEEE Trans. Power Electron.* **2015**, *30*, 2891–2895. [CrossRef]
63. Cannata, G.; De Caro, S.; Panarello, S.; Scimone, T.; Testa, A.; Russo, S. Reliability Assessment of Avalanche Mode Operating Power MOSFETs Through Coffin Manson Law Based Mathematical Models. In Proceedings of the International Symposium on Power Electronics, Electrical Drives, Automation and Motion, SPEEDAM, Ischia, Italy, 18–20 June 2014; pp. 139–145.
64. Zhang, F.; Chen, X.; Yu, C.; Lu, S.; Xu, X.; Hu, X.; Li, T.; Zhao, X.; Zhang, Y.; Wang, R. Large-Area Uniform Epitaxial Graphene on SiC by Optimizing Temperature Field. In Proceedings of the 13th China International Forum on Solid State Lighting: International Forum on Wide Bandgap Semiconductors China, Beijing, China, 15–17 November 2016; pp. 54–57. [CrossRef]
65. Shi, L.; Qian, J.; Jin, M.; Bhattacharya, M.; YU, H.; White, M.H.; Anant, K. An Effective Screening Technique for Early Oxide Failure in SiC Power MOSFETs. In Proceedings of the IEEE 10th Workshop on Wide Bandgap Power Devices & Applications, Charlotte, NC, USA, 4–6 December 2023; pp. 1–4. [CrossRef]
66. Shi, L.; Qian, J.; Jin, M.; Bhattacharya, M.; Yu, H.; White, M.; Agarwal, A.K.; Shimbori, A. Evaluation of Burn-in Technique on Gate Oxide Reliability in Commercial SiC MOSFETs. In Proceedings of the IEEE International Reliability Physics Symposium (IRPS), Grapevine, TX, USA, 14–18 April 2024; pp. 1–6. [CrossRef]
67. Zhang, M.; Li, H.; Yang, Z.; Zhao, S.; Wang, X.; Ding, L. Short Circuit Protection of Silicon Carbide MOSFETs: Challenges, Methods, and Prospects. *IEEE Trans. Power Electron.* **2024**, *39*, 13081–13095. [CrossRef]
68. Cai, Y.; Sun, P.; Chen, C.; Zhang, Y.; Zhao, Z.; Li, X. Investigation on Gate Oxide Degradation of SiC MOSFET in Switching Operation. *IEEE Trans. Power Electron.* **2024**, *39*, 9565–9578. [CrossRef]
69. Domeij, J.; Franchi, B.; Buono, K.; Lee, K.-S.; Park, C.-S.; Choi, S.; Sunkari, S.; Das, H. Avalanche Rugged 1200 V 80 m SiC MOSFETs with State-of-the-Art Threshold Voltage Stability. In Proceedings of the IEEE 6th Workshop Wide Bandgap Power Devices and Applications (WiPDA), Atlanta, GA, USA, 31 October–2 November 2018; pp. 114–117.
70. Jang, M.-S.; Jeong, J.-H.; Lee, H.-J. Analysis of Ruggedness of 4H-SiC Power MOSFETs with Various Doping Parameters. *Appl. Sci.* **2023**, *13*, 427. [CrossRef]
71. Pu, S.; Akin, B.; Yang, F. Active Channel Impact on SiC MOSFET Gate Oxide Reliability. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition (APEC), Online, 14–17 June 2021; pp. 1250–1255. [CrossRef]
72. Zhu, S.; Liu, T.; White, M.H.; Agarwal, A.K.; Salemi, A.; Sheridan, D. Investigation of Gate Leakage Current Behavior for Commercial 1.2 kV 4H-SiC Power MOSFETs. In Proceedings of the IEEE International Reliability Physics Symposiym (IRPS), Monterey, CA, USA, 21–25 March 2021; pp. 1–7. [CrossRef]
73. Östling, M.; Ghandi, R.; Zetterling, C.-M. SiC Power Devices—Present Status, Applications and Future Perspective. In Proceedings of the IEEE 23rd International Symposium on Power Semiconductor and Devices, San Diego, CA, USA, 23–26 May 2011; pp. 10–15.
74. Hosseinzadehlish, M.; Jahdi, S.; Yuan, X.; Ortiz-Gonzalez, J.; Alatise, O. High-Energy Dynamic Avalanche to Failure by Incremental Source-Voltage Increase in Symmetric Double-Trench & Asymmetric Trench SiC MOSFETs. *IEEE Open J. Ind. Appl.* **2024**, *5*, 235–252. [CrossRef]
75. Takamori, T.; Wada, K.; Saito, W.; Nishizawa, S.-I. Paralleled SiC MOSFETs Circuit Breaker with a SiC MPS Diode for Avalanche Voltage Clamping. *IEEE Open J. Power Electron.* **2024**, *5*, 392–401. [CrossRef]
76. Fu, H.; Wei, J.; Liu, S.; Wu, W.; Sun, W. Repetitive-avalanche-induced Electrical Degradation and Optimization for 1.2kV 4H-SiC MOSFETs. In Proceedings of the IEEE 26th International Symposium on Physical and Failure Analysis of Integrated Circuits (IPFA), Hangzhou, China, 2–5 July 2019; pp. 1–4. [CrossRef]
77. Li, Z.; Jiang, J.; He, Z.; Hu, S.; Shi, Y.; Zhao, Z.; He, Y.; Chen, Y.; Lu, G. The Influence of Special Environments on SiC MOSFETs. *Materials* **2023**, *13*, 16–18. [CrossRef] [PubMed]

78. Hanfa, M.; Hoffmannb, F.; Brunkoc, A.; Petersd, J.-H.; Clausnere, S.; Kaminskif, N. Power Cycling Performance of 3.3 kV SiC-MOSFETs and the Impact of the Thermo-Mechanical Stress on Humidity Induced Degradation. *Solid State Phenom.* **2024**, *360*, 195–204. [CrossRef]
79. Ngwashi, D.K.; Phung, L.V. Recent review on failures in silicon carbide power MOSFETs. *Microelectron. Reliab.* **2021**, *123*, 114169. [CrossRef]
80. Chen, Z.; Yao, Y.; Danilovic, M.; Boroyevich, D. Performance Evaluation of SiC Power MOSFETs for High-Temperature Applications. In Proceedings of the 15th International Power Electronics and Motion Control Conference (EPE/PEMC), Novi Sad, Serbia, 4–6 September 2012. pp. DS1a.8-1-DS1a.8-9. [CrossRef]
81. Lu, X.; Wang, L.; Yang, Q.; Yang, F.; Gan, Y.; Zhang, H. Investigation and Comparison of Temperature-Sensitive Electrical Parameters of SiC mosfet at Extremely High Temperatures. *IEEE Trans. Power Electron.* **2023**, *38*, 9660–9672. [CrossRef]
82. Yao, K.; Yano, H.; Tadano, H.; Iwamuro, N. Investigations of SiC MOSFET Short-Circuit Failure Mechanisms Using Electrical, Thermal, and Mechanical Stress Analyses. *IEEE Trans. Electron Devices* **2020**, *67*, 4328–4334. [CrossRef]
83. Yu, R.; Jahdi, S.; Alatise, O.; Ortiz-Gonzalez, J.; Munagala, S.P.; Simpson, N. Measurements and Review of Failure Mechanisms and Reliability Constraints of 4H-SiC Power MOSFETs Under Short Circuit Events. *IEEE Trans. Device Mater. Reliab.* **2023**, *23*, 544–563. [CrossRef]
84. Chen, J.; Jiang, X.; Li, Z.; Yu, H.; Wang, J. Investigation on Degradation of SiC MOSFET Under Accelerated Stress in PFC Converter. In Proceedings of the IEEE Energy Conversion Congress and Exposition (ECCE), Baltimore, MD, USA, 29 September–3 October 2019; pp. 6174–6178. [CrossRef]

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