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Verification of Design and Process for Optimal Large-Area Substrate Eutectic Bonding in SiP Packaging

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Abstract

A ceramic-packaged, dual-layer-stacked System-in-Package (SiP) architecture combines the hermeticity of ceramic substrates with the superior radio frequency (RF) performance of organic substrates to meet the demands for high-density integration, cost-effectiveness, and high performance. This study investigates the issues of thermal mismatch, solder joint contamination, and void formation during the large-area eutectic bonding of the lower organic substrate using Pb70In30 solder through simulation and an experimental approach. The results indicate that: (a) the post-bonding warpage of the organic substrate can be reduced to under 80 μm by optimizing its copper layer thickness, dielectric layer thickness, and cavity/slot distribution, and (b) flux pretreatment can be employed to reduce the Pb70In30 solder in an N_2/H_2 mixture at a eutectic temperature of 285 °C and a pressure of 1.5 kPa effectively promotes solder spreading, prevents solder joint contamination, and yields a void formation percentage below 10%, a shear strength of 23.66 MPa, and solder overflow exceeding 90%, thereby satisfying the requirements for reliable large-area eutectic bonding. These findings offer guidance for the packaging process design of ceramic-packaged, dual-layer-stacked SiPs.

Keywords: 3D-SiP; organic substrate; multilayer stacking; warpage; void percentage

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1. Introduction

Multifunctionality, high performance, and miniaturization represent key developmental trends in electronic information systems [1]. To meet the high-integration demands of next-generation equipment, conventional planar integration technologies are approaching their limits. This necessitates a shift toward three-dimensional (3D) stacking to address the high-density integration challenges of broadband RF components [2]. 3D-SiP technology enables high-density integration through multilayer wiring and 3D micro-assembly processes, facilitating the three-dimensional (3D) assembly [3] of multi-chip circuits. This approach contributes to enhanced product reliability and package miniaturization, exhibiting broad application prospects in military, aerospace, and related fields. A 3D-SiP solution

based on a Through-Ceramic-Via (TCV) packaging substrate stacked with a dual-layer high-density interconnect (HDI) substrate can significantly enhance product integration density while reducing its volume and weight [4]. The structure of a ceramic-packaged, dual-layer-stacked 3D-SiP is illustrated in Figure 1 [5]. A high-density ceramic packaging substrate serves as a hermetic constituent of the SiP. Together with a metal frame and a lid, it forms a hermetic TCV ceramic package shell. Externally, Ball Grid Array (BGA) solder balls serve as the input/output interconnect interface for the TCV package shell. Internally, BGA solder balls are utilized to interconnect the two stacked HDI substrates, enabling the 3D assembly of multi-chip circuits. This design balances hermeticity with multilayer RF signal transmission, thereby meeting the requirements for high integration density, cost-effectiveness, and high performance.

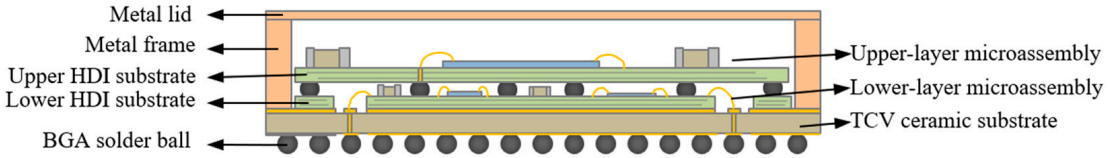


Figure 1. Schematic of a ceramic-packaged, dual-layer-stacked SiP structure [5].

Figure 2 presents a simplified flowchart of the soldering assembly process for the ceramic-packaged, dual-layer-stacked SiP, which employs a multi-temperature-gradient soldering process [6]: (a) hermetic soldering of the TCV ceramic substrate to the metal frame; (b) soldering of the lower HDI substrate inside the ceramic package; (c) package-on-package (PoP) stacking of the dual-layer HDI substrates; and (d) soldering of surface-mount components onto the upper HDI substrate. Based on the established soldering processes and requirements, a complete soldering assembly temperature gradient is summarized in Table 1.

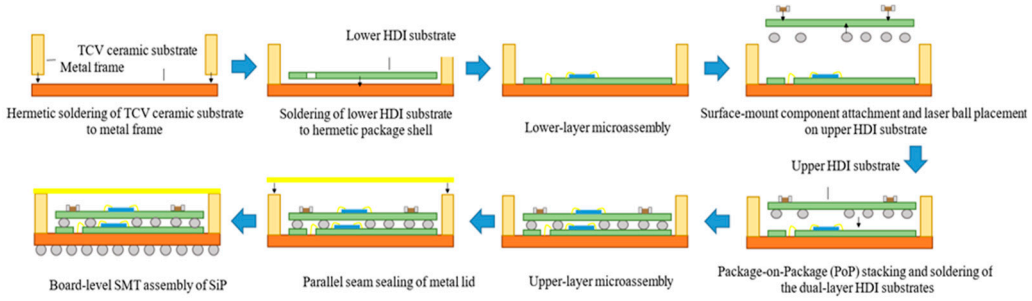


Figure 2. Flowchart of the soldering assembly process for a ceramic-packaged, dual-layer-stacked SiP.

Table 1. Soldering assembly temperature gradients for a ceramic-packaged, dual-layer-stacked SiP.

Soldering Temperature Gradient	Solder	Soldering Temperature	Functions
Level I	Au80Sn20	280 °C	Hermetic soldering of TCV ceramic substrate to metal frame
Level II	Pb70In30	250 °C	Soldering of lower HDI substrate in ceramic package
Level III	SAC305 (Sn96.5Ag3.0Cu0.5)	217 °C	Soldering of surface-mount components on upper HDI substrate PoP stacking soldering of the upper HDI substrate
Level IV	Sn63Pb37	183 °C	Board-level assembly of SiP

Among the soldering temperature gradients outlined above, Levels I, III, and IV utilize solders and processes that are well-established and widely adopted in the industry [7]. The Level II soldering temperature gradient—specifically, the large-area eutectic bonding between the TCV package shell and the lower HDI substrate—constitutes a pivotal step that links preceding and subsequent steps in the multi-temperature-gradient assembly process. It capitalizes on the superior RF performance [8] of the HDI substrate and the vertical interconnect and hermetic packaging capabilities [9] of the TCV substrate to form the foundation for BGA inter-layer connections. Nevertheless, detailed studies on its specific process methodology remain scarce. The large-area eutectic bonding between the TCV package shell and the lower HDI substrate presents the following challenges: (1) Thermal mismatch [10]: A significant thermal mismatch between the HDI and TCV substrates leads to warpage exceeding 80 μm in the HDI substrate after bonding. This excessive warpage poses a substantial risk of defective or missing solder joints during subsequent BGA stacking, as illustrated in Figure 3. (2) Void formation: Although In-Pb solders exhibit good fatigue resistance [11,12], they are prone to oxidation and have poor wettability. These characteristics can lead to void formation during large-area eutectic bonding, which subsequently compromises heat dissipation in high-power chips [13]. (3) Solder joint contamination: The eutectic process using In–Pb series solders may result in pad contamination from flux or solder residues, compromising the gold-wire bonding strength.

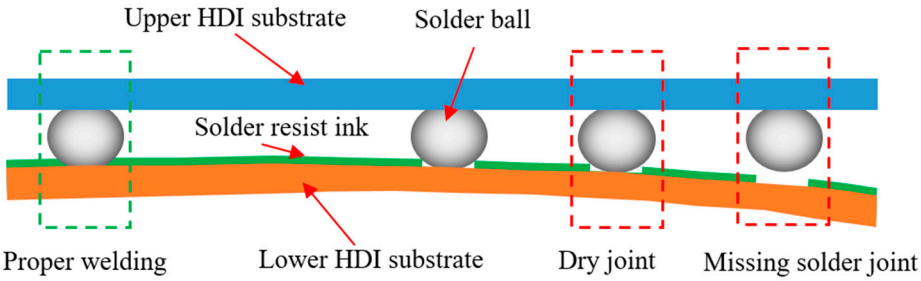


Figure 3. Substrate warpage leading to ball-placement failure. Note: The areas outlined in green indicate proper assembly between the TCV package shell and the HDI substrate, while those outlined in red show incorrect assembly caused by warpage at the HDI substrate interface.

This study aims to examine the effects of the HDI substrate's structural parameters and soldering process parameters (e.g., reducing atmosphere, temperature, and pressure) on HDI substrate warpage, void formation, mechanical properties, and pad contamination during the large-area eutectic bonding process in dual-layer SiP packaging. These findings provide valuable insights for improving 3D-SiP quality and lay a practical foundation for its engineering application.

2. Experimental Meterials and Methods

2.1. Experimental Materials

The materials used in the experiments are as follows: Direct Plated Copper (DPC) ceramic substrates (22.5 mm × 15 mm) with NiAu plating (Ni 4–5 μm, Au 3–4 μm); HDI Substrate 1 (20.3 mm × 12.8 mm) with NiPdAu plating (Ni 3–6 μm, Pd 0.075–0.15 μm, Au 0.08–0.2 μm); HDI Substrate 2 (3 mm × 3 mm) with NiPdAu plating (Ni 3–6 μm, Pd 0.075–0.15 μm, Au 0.08–0.2 μm); Pb70In30 Solder Preform 1 (20.1 mm × 12.6 mm × 0.05 mm) and Pb70In30 Solder Preform 2 (3 mm × 3 mm × 0.05 mm); copper pressure blocks with weights of 1.5 g, 13 g, 26 g, 39 g, and 78 g; and reducers including INDIUM 007 flux, formic acid gas, and N_2/H_2 mixture.

2.2. Experimental Equipment, Instruments, and Software

The equipment, instruments, and software used in the experiments are as follows: Vacuum eutectic oven (TORCH AV3-3), manufactured by Beijing Torch Smt Incorporated Company, Beijing, China. thermal deformation measurement system (INSIDIX TDM Compact3), manufactured by Insidix, Grenoble, France.bond tester (Nordson DAGE 4000 plus), manufactured by Nordson DAGE, Aylesbury, UK. contact angle goniometer (CAM-9F), manufactured by Shanghai Xuan Yi Chuang Xi Industrial Equipment Co., Ltd., Shanghai, China. CT testing system (EFPscan 2150), manufactured by Tianjin Sanying Precision Instrument Co., Ltd., Tianjin, China. microscope (KEYENCE VHX-S770E), manufactured by KEYENCE Corporation, Osaka, Japan. scanning electron microscope (SEM) (MIRA3), manufactured by TESCAN, Brno, Czech Republic. dual-beam FIB (Helios G4 CX & ULTIM MAX), manufactured by Thermo Fisher Scientific, Waltham, MA, USA and Oxford Instruments, Oxford, UK respectively. ANSYS Workbench 15.0, and CATIA 2017.

2.3. Experimental Procedure

First, simulation analysis was conducted to investigate the influence of structural parameters on the warpage of the HDI substrate during eutectic bonding. Subsequently, the effects of key process parameters—namely, the reducing atmosphere (formic acid gas or N_2/H_2 mixture), eutectic temperature, and eutectic pressure—on the large-area soldering quality of the HDI substrate were evaluated. The evaluation criteria included void formation, mechanical properties, and pad contamination. Finally, the optimal eutectic bonding of the HDI substrate was performed based on the integrated simulation and experimental results. The detailed procedure is described below:

2.3.1. Warpage Simulation of the HDI Substrate

Conventional modeling approaches for HDI substrate simulation are challenging due to their intricate multilayer wiring and high density of interlayer vias, which lead to difficulties in model construction, poor mesh quality, and high computational cost. TraceMapping technology overcomes these limitations by directly mapping the wiring and via patterns from EDA data onto simplified 3D block elements. The material properties of each layer are approximated based on equivalent copper-fill ratios. This approach significantly simplifies mesh generation and reduces computational demands. The modeling and simulation workflow comprised the following steps:

(1) The properties of key materials in HDI substrates (such as the elastic modulus, Poisson's ratio, coefficient of thermal expansion, thickness, etc., of the copper cladding layer, dielectric layer, and solder mask layer) were configured, as shown in Figure 4 and Tables 2 and 3.
(2) The copper layer and dielectric layer were modeled in CATIA, with the modeling elements including the length, width, thickness, and cavities/grooves of each layer, as shown in Figure 4.
(3) The model was exported in STP format and imported into ANSYS Workbench for meshing.
(4) The wiring, vias, and cavity/slot structures of the actual product were imported through ODB++ files. The material, layer thickness, and material properties for each layer were defined.
(5) A eutectic temperature load of 270 °C was applied, with weak springs and large deflection enabled.
(6) The simulation was calculated and solved.

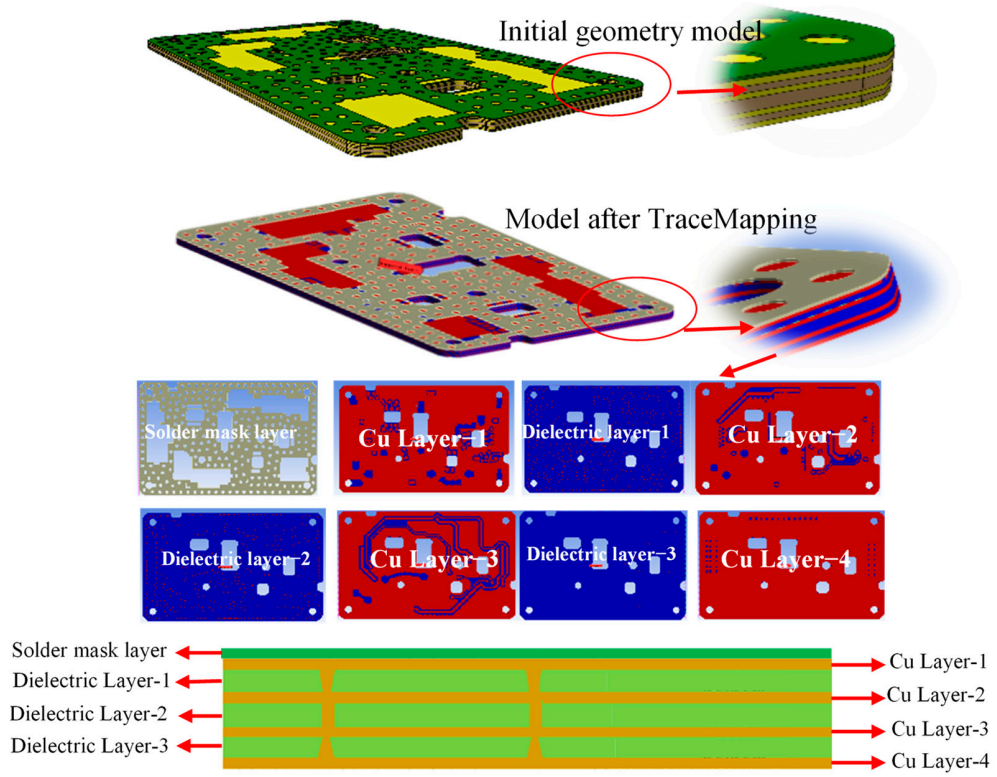


Figure 4. HDI substrate model and stack-up structure. Note: Color representation: Gray/Dark Green indicates the solder mask layer; Red/Orange represents the mapped copper layers (Cu Layer-1 to Cu Layer-4); Blue/Light Green denotes the dielectric layers.

Table 2. Properties of materials in the HDI substrate.

	Elastic Modulus E/ Gpa	Poisson's Ratio	CTE/ ppm/°C	Density/ kg/m^3	Yield Strength /Mpa	Tangent Modulus/ Mpa
Copper layer	110	0.34	18	8300	200	80
Dielectric layer	21	0.18	X:9; Y:9; Z:20@ < 260 °C, 80@ > 260 °C	1800	/	/
Solder mask layer	4.4	0.18	60	1550	/	/

Table 3. Thickness of material in each HDI substrate layer.

Element	Description	Thickness/μm
Copper layer	Top layer (Layer 1)	20, 30, 40, 50, 60
	Inner layer (Layer 2)	40
	Inner layer (Layer 3)	40
	Bottom layer (Layer 4)	40
Dielectric layer	Top layer (Layer 1)	50, 80
	Inner layer (Layer 2)	100
	Bottom layer (Layer 3)	50, 80
Solder mask layer	Layer 0	25

2.3.2. Eutectic Bonding Experiment for HDI Substrates

The critical process parameters influencing the eutectic bonding of HDI substrates include reducing atmosphere, eutectic temperature, and eutectic pressure. The procedure of the eutectic bonding experiment is as follows:

(1) Oxide reduction experiment. First, Pb70In30 Solder Preform 1 was placed on the surface of HDI Substrate 1 and subjected to different reduction pretreatments (INDIUM 007 flux, formic acid gas, and N_2/H_2 mixture) in the vacuum eutectic oven (TORCH AV3-3) at 220 °C. Then, the wettability of the pretreated Pb70In30 Solder Preform 1 was evaluated by contact angle measurement using the contact angle goniometer (CAM-9F). Finally, the morphology and composition of the bonding pads on HDI Substrate 1 under different reducing atmospheres were analyzed using the microscope (KEYENCE VHX-S770E), SEM (MIRA3), and dual-beam FIB (Helios G4 CX & ULTIM MAX) to assess pad contamination.

(2) Eutectic bonding experiment—eutectic temperature. First, based on the results of Step 1, a suitable reducing atmosphere was selected, and the eutectic experiment was conducted in a vacuum eutectic oven (TORCH AV3-3) at different temperatures (280 °C, 285 °C, 290 °C, and 295 °C). Pb70In30 Solder Preform 1 was used with HDI Substrate 1 under the pressure block of 39 g. Pb70In30 Solder Preform 2 was used with HDI Substrate 2 under the pressure block of 1.5 g. After eutectic bonding, the void area of HDI Substrate 1 was analyzed using the CT testing system (EFP scan 2150), and the bonding interface and composition were examined using the microscope (KEYENCE VHX-S770E) and SEM (MIRA3). Finally, the shear strength of the bonded HDI Substrate 2 was measured using the bond tester (Nordson DAGE 4000 Plus).

(3) Eutectic bonding experiment—eutectic pressure. First, based on the results of Step 2, a suitable eutectic temperature was selected, and the eutectic experiment was conducted in a vacuum eutectic oven (TORCH AV3-3) under different applied pressures (13 g (0.5 kPa), 26 g (1 kPa), 39 g (1.5 kPa), and 78 g (3 kPa)). Pb70In30 Solder Preform 1 was used with HDI Substrate 1. After eutectic bonding, the void area of HDI Substrate 1 was analyzed using the CT testing system (EFP scan 2150), and the solder overflow under different pressures was examined using the microscope (KEYENCE VHX-S770E).

2.3.3. Physical Verification Experiment

Based on the simulation results from Section 2.3.1 and the eutectic experiment results from Section 2.3.2, suitable HDI substrate structural parameters and eutectic process parameters were first selected. Physical HDI substrates were then fabricated and subjected to eutectic bonding. Subsequently, the warpage of the HDI substrates was measured using the thermal deformation measurement system (INSIDIX TDM Compact3). Finally, the void area and the interconnection condition of the inter-layer BGA in the HDI substrate were analyzed using the CT testing system (EFP scan 2150).

3. Experiment Results and Discussion

3.1. Results and Discussion of HDI Substrate Warpage

HDI substrates are prone to warpage during processes such as baking for moisture removal, bonding between the TCV ceramic substrate and the lower HDI substrate, and stacked bonding of the upper and lower HDI substrates [5]. HDI substrate warpage is primarily caused by the CTE mismatch among various materials [14]. This is closely related to material selection, structural design, and manufacturing processes [5,15–17]. Compared with the upper HDI substrate, the lower HDI substrate has its entire backside as a metal layer for soldering to the TCV substrate, while its front side serves as the solder mask layer for BGA interconnection and therefore requires a green solder mask coating. The lower HDI substrate exhibits poor structural symmetry, leading to more pronounced warpage. To address the warpage issue of the lower HDI substrate, the effects of copper layer thickness,

dielectric layer thickness, and cavity/slot location on HDI substrate warpage were analyzed via simulation.

(1) Analysis of the effect of the copper layer

The thickness of the front-side solder mask layer on the lower HDI substrate is positively correlated with the surface copper layer thickness; an increase in the latter leads to a corresponding increase in the former. The poor structural symmetry of the lower HDI substrate leads to significant warpage. Meanwhile, the copper layer thickness directly affects the stiffness of the HDI substrate. Excessively thin copper layers degrade the substrate stiffness, which cannot effectively counteract the high-temperature deformation of the surface solder mask layer. Therefore, balancing the copper layer thicknesses in the HDI substrate is necessary.

Simulations were performed on a typical lower HDI substrate structure. Under the condition of a consistent stack-up structure, dielectric thickness, and other factors, while keeping the copper thickness of the two inner layers at 40 µm and the bottom layer at 40 µm, the surface copper thickness was reduced from 60 µm to 30 µm. The simulation results indicate that the Z-direction deformation of the organic substrate decreased to approximately 15 µm, and the deformation mode transitioned progressively from a "crying face" to a "smiling face". These results are shown in Figure 5 and Table 4.

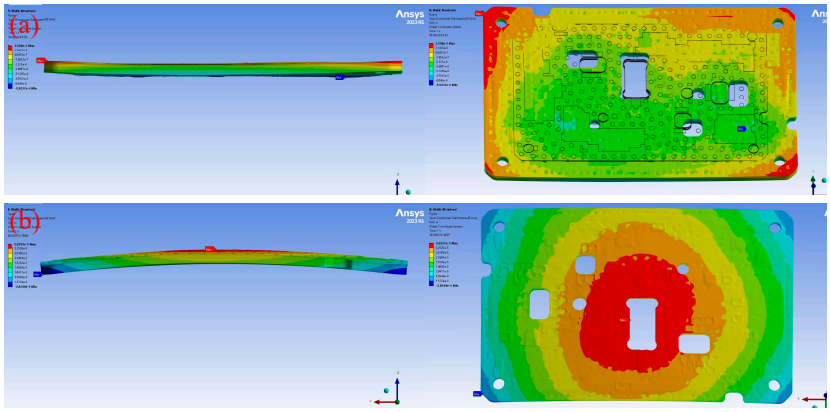


Figure 5. Effect of Copper and Dielectric Layer Thicknesses on HDI Substrate Warpage under Symmetric Cavity/Slot Structure: (**a**) Crying-Face Warpage; (**b**) Smiling-Face Warpage.

Table 4. Thickness and Warpage of Different Layers in HDI Substrate.

Description	Symmetric Cavity/Slot								Asymmetric Cavity/Slot
	Model 0	Model 1	Model 2	Model 3	Model 4	Model 5	Model 6	Model 7	Model 8
Solder mask/µm	25	25	25	25	25	25	25	25	25
Cu-L1/um	30	30	20	40	50	60	30	30	30
Dielectric 1/µm	50	80	50	50	50	50	50	80	50
Cu-L2/um	40	40	40	40	40	40	40	40	40
Dielectric 2/µm	100	100	100	100	100	100	100	100	100
Cu-L3/um	40	40	40	40	40	40	40	40	40
Dielectric 3/µm	50	80	50	50	50	50	80	50	50
Cu-L4/um	40	40	40	40	40	40	40	40	40
Deformation Feature	Smiling face	Smiling face	Smiling face	Smiling face	Crying face	Crying face	Crying face	Smiling face	Twist
Warpage/µm	13	21	34	18	30	40	17	38	27

(2) Analysis of the effect of the dielectric layer

Dielectric layers, serving as insulation and a physical support structure for circuits, are generally thicker than copper layers and have a lower Young's modulus. Therefore, they are more prone to deformation under thermal stress. Simulation revealed that, with the thickness of Dielectric Layer 2 in the HDI substrate held constant at 100 μm, increasing only the thickness of Dielectric Layer 1 to 80 μm increased the HDI substrate warpage from 13 μm to 37 μm, while remaining a "smiling face" type warpage. When only increasing the thickness of Dielectric Layer 2 to 80 μm, the organic substrate warpage increased from 13 μm to 17 μm. However, the warpage type changed to a "crying face". The results are shown in Table 4. Therefore, the thickness and symmetry of each dielectric layer significantly affect the overall substrate warpage. The middle dielectric layer should be thicker than the other layers to establish a baseline warpage, while the thicknesses of the other layers should be as symmetrical as possible about the center layer to fine-tune the warpage magnitude.

(3) Analysis of the effect of cavity/slot

The lower HDI substrate requires cavities/slots to achieve RF signal interconnection with the TCV substrate. However, cavities/slots affect the overall stiffness and internal stress of the substrate, thereby influencing its warpage after high-temperature processes. To study the effect of cavities/slots on HDI substrate warpage, different cavity/slot structures were simulated under the same layer thickness conditions. The results are shown in Figure 6 and Table 4. The simulation results indicate that an HDI substrate with a single large cavity/slot on the side exhibits overall deformation more than 10 μm larger than that of a structure with distributed smaller cavities/slots, and the warpage modes are completely different. Therefore, priority should be given to symmetrical cavity/slot layouts in cavity/slot design.

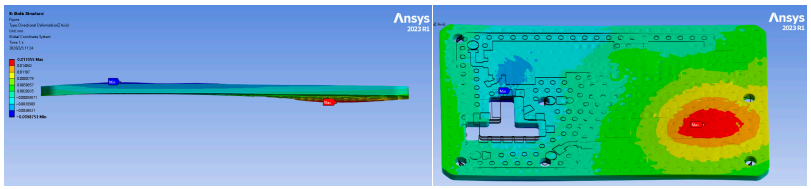


Figure 6. Twisted Warpage of HDI Substrate Caused by Asymmetric Cavity/Slot Structure.

Based on the comprehensive simulation analysis, the minimum warpage of the HDI substrate was 13 μm under the following conditions: the inner two copper layers were both 40 μm thick; the top and bottom copper layers were 30 μm and 40 μm thick, respectively; the top, middle, and bottom dielectric layer thicknesses are 50 μm, 100 μm, and 50 μm respectively; the front-side solder mask thickness is 25 μm; and a distributed symmetric cavity/slot design is adopted, the minimum warpage of the HDI substrate is 13 μm.

3.2. Results and Discussion of HDI Substrate Eutectic Experiment

(1) Effect of reducing the atmosphere on eutectic results

In-based solders are prone to oxidation, easily forming a stable layer of In_2O_3 on the surface during preparation and packaging, thereby hindering wetting and spreading after melting [18]. Therefore, removing surface oxides and preventing their formation are key to using Pb70In30 for bonding. Flux, as a soldering activator, is widely used in electronic soft soldering to remove oxide layers on solder surfaces while protecting the solder from re-oxidation. While the flux method can effectively remove oxides, its volatiles readily contaminate the vacuum eutectic oven chamber [19] and enter the gap between the solder

layers on the HDI substrate and the DPC substrate. During subsequent assembly heating, trapped flux may seep out and contaminate the product. Consequently, soldering of the lower HDI substrate within the ceramic package must employ a flux-free process. Common active gases in vacuum eutectic processes are N_2/H_2mixture and formic acid gas. However, the ability of these reducing gases to remove oxides from In-based solder surfaces is limited. The authors found in preliminary research that flux pretreatment combined with active gas reduction significantly improves the wettability of In-based solder surfaces.

The contact angle results for Pb70In30 Solder Preform 1 after different reduction treatments are shown in Figures 7 and 8. The contact angle of the as-received Pb70In30 solder preform was 96.81°. After undergoing different reduction treatments using flux, a flux + N_2/H_2 mixture, and flux + formic acid, the contact angles were measured at 78.47°, 60.19°, and 50.53°, respectively. After different reduction treatments, the contact angle on the Pb70In30 solder preform surface decreased significantly, indicating improved wettability.

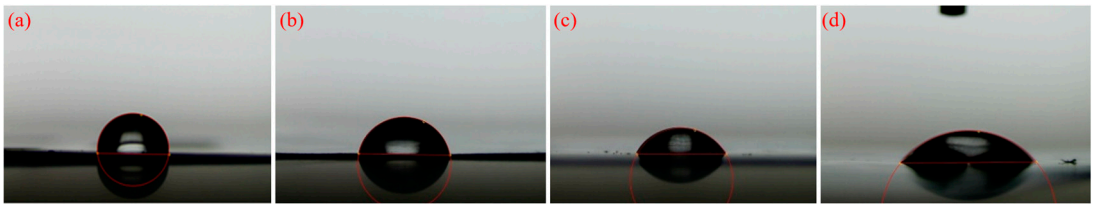


Figure 7. Contact Angle Images of Pb70In30 Solder Preform under Different Conditions: (**a**) Original State; (**b**) Flux Reduction; (**c**) Flux + N_2/H_2 Reduction; (**d**) Flux + Formic Acid Reduction.

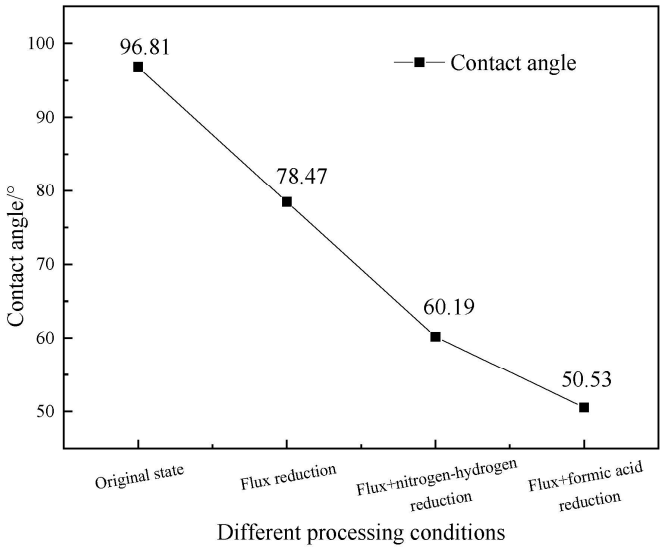


Figure 8. Contact Angles of Pb70In30 Solder Preform under Different Conditions.

The condition of the gold-plated pads on the HDI substrate after different reduction treatments of the Pb70In30 solder preform is shown in Figure 9. The gold-plated pad after flux + N_2/H_2 reduction did not turn black, whereas the pad after flux + formic acid reduction turned black. SEM and EDS analyses were performed on the non-blackened and blackened pads (Figures 10 and 11). The non-blackened pad surface was flat, exhibited no protruding particles, and contained mainly C, O, Au, and Pd. The blackened pad surface was rough, with small protruding particles, and contained mainly C, O, Au, In, and Pd. Comparison indicates that In is an anomalous element.

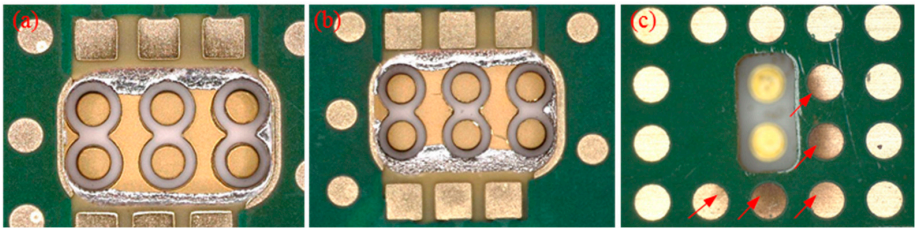
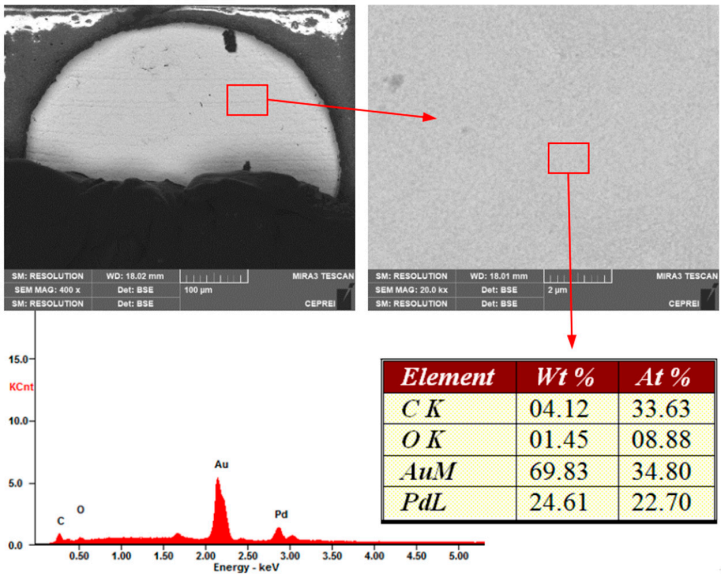
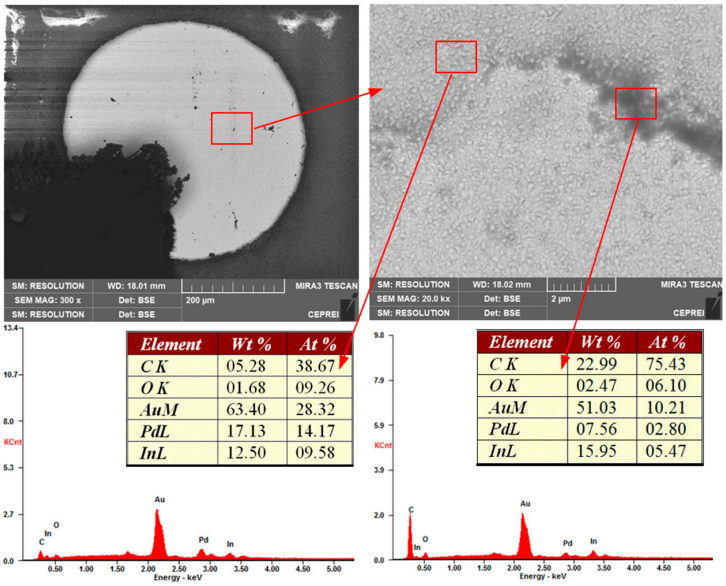


Figure 9. Surface Condition of Gold-Plated Pads on HDI Substrate: (**a**) Original State; (**b**) Flux + N_2/H_2 Reduction; (**c**) Flux + Formic Acid Reduction. Note: The areas indicated by the red arrows in the figure are contaminated gold-plated pads.



Element	Wt %	At %
C K	04.12	33.63
O K	01.45	08.88
AuM	69.83	34.80
PdL	24.61	22.70

Figure 10. SEM and EDS Images of Non-Blackened Pad Surface. Note: The red polyline and its peaks in the spectrum represent the detected characteristic X-ray signals, with peak positions corresponding to carbon (C), oxygen (O), gold (Au), and palladium (Pd) elements. The color red is used to highlight this core spectral data, ensuring its prominence against the background.



Element	Wt %	At %
C K	05.28	38.67
O K	01.68	09.26
AuM	63.40	28.32
PdL	17.13	14.17
InL	12.50	09.58

Element	Wt %	At %
C K	22.99	75.43
O K	02.47	06.10
AuM	51.03	10.21
PdL	07.56	02.80
InL	15.95	05.47

Figure 11. SEM and EDS Images of Blackened Pad Surface. Note: Red highlighting identifies key spectral peaks (e.g., Au) and principal components (e.g., Au, Pd), consistent with Figure 10, to emphasize core results.

The blackened pad was further cleaned with isopropanol and diluted hydrochloric acid (5 wt%) under ultrasonication, followed by wiping. Neither the blackening nor the surface residue diminished or disappeared, indicating that organic contamination or surface oxidation was not the primary cause. Further FIB cross-sectional analysis of the blackened pad (Figure 12) revealed a continuous foreign layer on the pad surface, approximately 0.1 μm thick, consisting mainly of C, O, Ni, Cu, Au, In, and Pd. Based on its elemental composition and the inability to remove it with alcohol/acid cleaning, the black foreign layer is an alloy layer formed between In from the Pb70In30 solder and Au from the gold-plated pad during soldering, resulting in pad blackening.

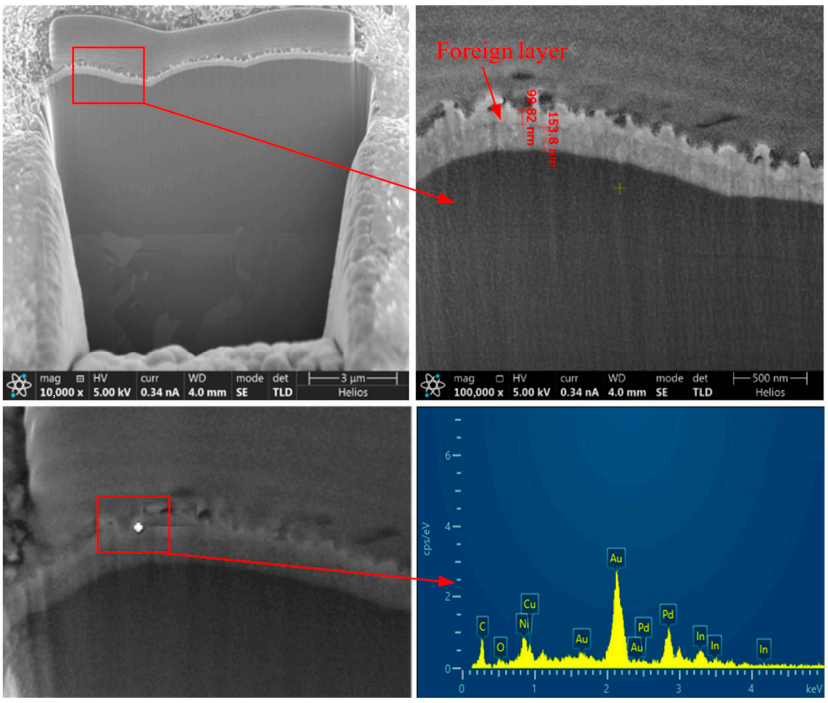


Figure 12. FIB Analysis Images of Blackened Pad Surface.

Formic acid, as a reducing gas, replaces oxygen atoms via carboxyl groups to form compounds, which decompose at high temperatures to form elemental metals or dissolve into the molten solder, thereby eliminating the adverse effects of metal oxides on solderability. The reactions of formic acid with In_2O_3 at different temperature ranges are as follows:

$$In_2O_3 + 6HCOOH = 2In(COOH)_3 + 3H_2O \ (150\ ^\circ C < T < 200\ ^\circ C) \quad (1)$$

$$2In(COOH)_3 = 2In + 6CO_2 + H_2 \ (T > 200\ ^\circ C) \quad (2)$$

When the temperature reaches 160 °C, formic acid reacts with the oxides on the Pb70In30 solder surface to form indium formate. When it reaches 220 °C, indium formate decomposes into elemental indium [20]. However, as indium formate is removed via sublimation and decomposition [21], the Pb70In30 solder has not yet reached its molten state, easily causing indium deposition around the solder, thus contaminating the pads.

Based on the above analysis, flux pretreatment combined with N_2/H_2 reduction is more suitable for Pb70In30 eutectic bonding.

(2) Effect of temperature on eutectic results

The void area in HDI substrate soldering at different eutectic temperatures is shown in Figures 13 and 14. As the eutectic temperature increased from 280 °C to 295 °C, the

solder wettability improved, and the void area decreased from 5.24% to 3.31%. The void area at 285 °C was 4.75%. All void areas at the different temperatures met the requirement of "void area less than 10%" specified in GJB 548C-2021 [22].

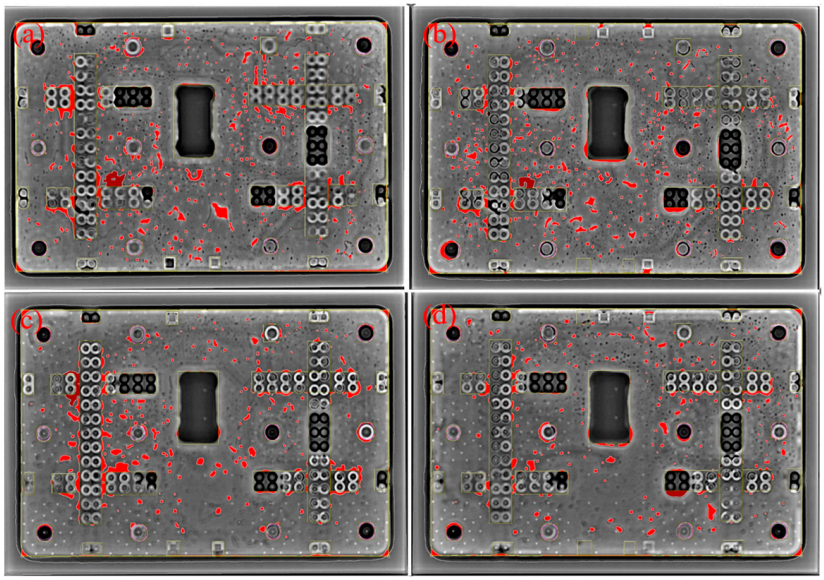


Figure 13. Voids (Red) in HDI Substrate Soldering at Different Eutectic Temperatures: (**a**) 280 °C; (**b**) 285 °C; (**c**) 290 °C; (**d**) 295 °C.

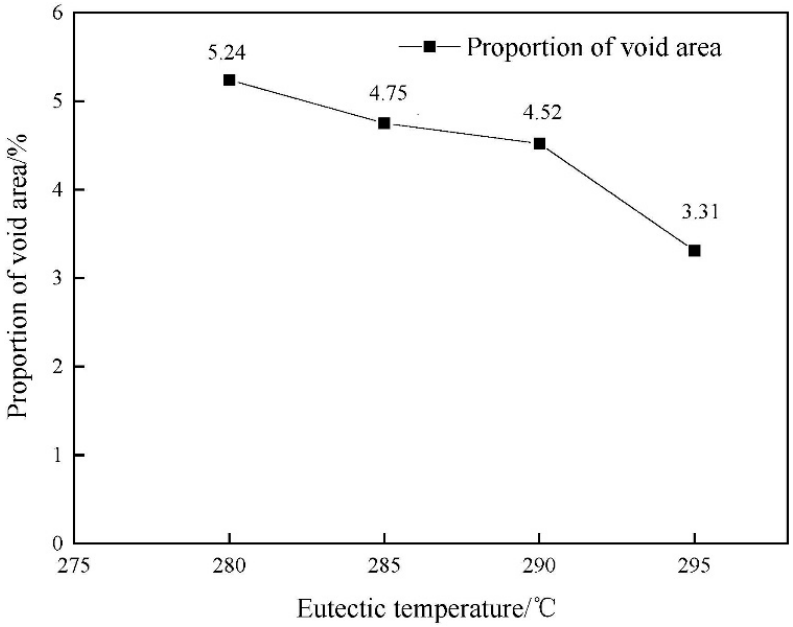


Figure 14. Void Formation Area in HDI Substrates at Different Eutectic Temperatures.

The shear strength of the HDI substrate at different eutectic temperatures is shown in Figure 15. As the eutectic temperature increased, the shear strength initially rose and then declined, reaching a maximum value of 23.66 MPa at 285 °C. The bonding interfaces of the HDI substrate at different eutectic temperatures are shown in Figures 16 and 17. On the HDI substrate side, the plating is NiPdAu. Due to the barrier effect of the Pd layer and the thin Au layer (0.08–0.2 μm), the thickness of the intermetallic compound (IMC) $AuIn_2$ did not change significantly with increasing temperature.

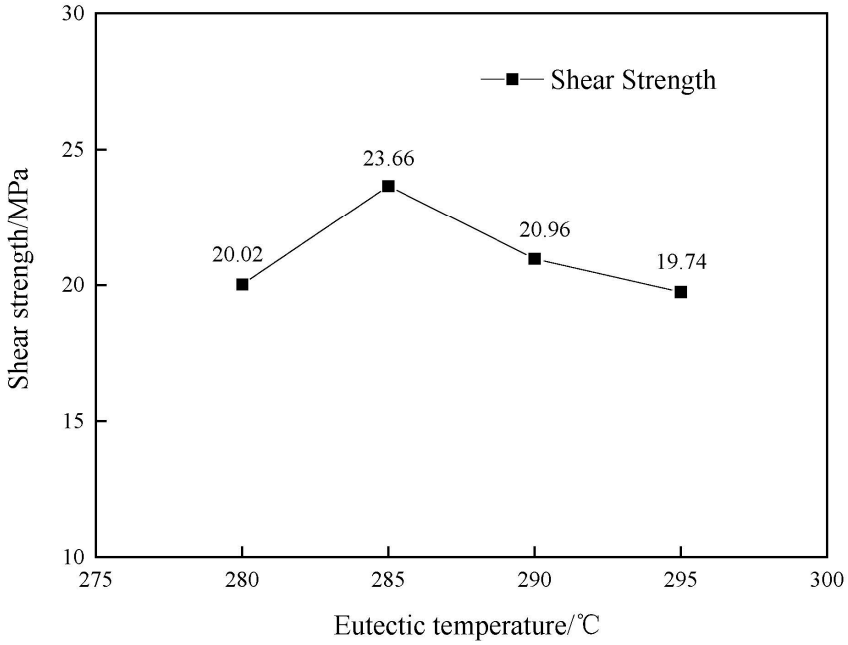


Figure 15. Shear Strength of HDI Substrate at Different Eutectic Temperatures.

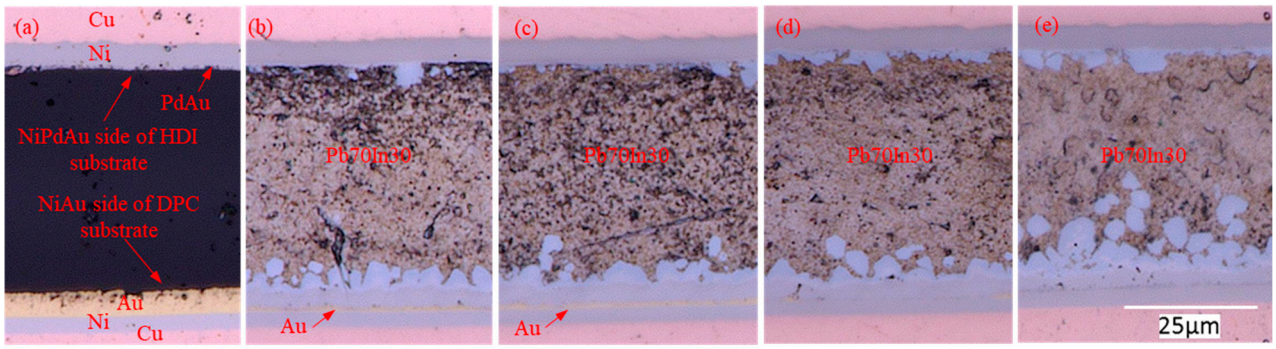


Figure 16. Bonding Interfaces of HDI Substrate at Different Eutectic Temperatures: (**a**) As-Received Interface; (**b**) 280 °C; (**c**) 285 °C; (**d**) 290 °C; (**e**) 295 °C.

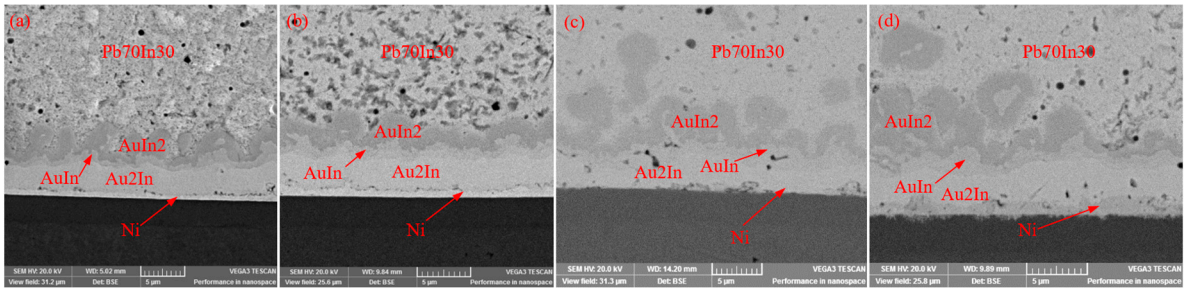


Figure 17. Bonding Interfaces on NiAu Side of DPC Substrate at Different Eutectic Temperatures: (**a**) 280 °C; (**b**) 285 °C; (**c**) 290 °C; (**d**) 295 °C.

On the DPC substrate side, the plating was NiAu. In the absence of a Pd barrier layer and with a thicker Au layer (3–4 μm), the IMC thickness increased significantly with rising temperature. A significant growth of both Au_2In and $AuIn_2$ phases was observed, which can be attributed to the high Au content in the plating layer adjacent to the eutectic solder Pb70In30. With increasing eutectic bonding temperature, the Au_2In phase continued to grow, resulting in the complete dissolution and consumption of the Au plating layer at the

interface. Concurrently, the $AuIn_2$ phase extended further into the solder bulk, and the AuIn phase also gradually thickened.

The growth thickness of IMC primarily follows Fick's law of diffusion. The IMC thickness d is proportional to the square root of the diffusion constant K and heating time t, while the diffusion constant K is an exponential function of the absolute temperature T [23], as shown in Equations (3) and (4):

$$d = K \times \sqrt{t} \tag{3}$$

$$K = K_0 exp^{(-\frac{Q}{RT})} \tag{4}$$

where K—IMC growth coefficient at a given temperature; K_0—frequency factor; Q—activation energy for IMC growth; R—ideal gas constant; and T—absolute temperature.

The IMC thickness is correlated with tensile strength [24]. When the IMC thickness is less than 0.5 μm, the solder joint may be in a cold-solder state due to the thin IMC layer, resulting in insufficient bonding strength. When the IMC thickness exceeds 4 μm, the overly thick IMC layer becomes loose, leading to increased alloy layer hardness, loss of elasticity, and consequently decreased bonding strength. Therefore, the acceptable optimal IMC thickness is 2–4 μm.

Therefore, to suppress excessive IMC growth and ensure good mechanical properties, the soldering temperature must be carefully controlled to avoid excessively high temperatures. Based on the comprehensive analysis of void area and shear strength for the HDI substrate, a eutectic temperature of 285 °C is deemed suitable.

(3) Effect of pressure on eutectic bonding results

The soldering condition of the HDI substrate at a eutectic temperature of 285 °C under different pressures is shown in Table 5 and Figure 18. As the pressure increased, the solder overflow gradually increased. At a pressure of 3 kPa, the solder overflow reached 100%; however, this caused excessive solder accumulation. The void percentage decreased with increasing pressure. At a pressure of 1.5 kPa, the void percentage was 4.75%. When the pressure increased to 3 kPa, the void percentage decreased only slightly; however, this caused excessive solder accumulation.

Table 5. Comparison of HDI Substrate Bonding under Different Pressure Conditions at a Eutectic Temperature of 285 °C.

Pressure (kPa)	Solder Overflow (% of Perimeter)	Void Percentage (% of Bonded Area)
0.5	45%	12.95%, occurrence of defective solder joints
1	85%	6.21%
1.5	94%	4.75%
3	100%, excessive solder accumulation	4.09%

During vacuum eutectic bonding, applying a force F on the HDI substrate can effectively reduce the gap between the HDI substrate and the TCV substrate, increasing the capillary filling length L. The capillary filling length L of solder in a parallel gap is shown in Figure 19 and Equation (5) [19]. From Equation (5), it can be observed that applying a force F on the HDI board can effectively reduce the gap between the HDI substrate and the TCV substrate, thereby increasing the filling length L. Insufficient or non-uniform pressure can cause gaps or defective solder joints between the HDI substrate and the TCV substrate. Excessive pressure may result in an overly thin solder layer, compromising shear strength.

It may also cause solder bridging and short circuits due to solder accumulation. During eutectic bonding, pressure is typically applied via a weight block. Through comparison, a pressure of 1.5 kPa was determined to yield ideal soldering conditions.

$$L = \frac{2\sigma cos\theta}{h\rho g} \quad (5)$$

where θ—contact angle; h—gap between substrates; ρ—density of solder; σ—surface tension of molten solder; and g—gravitational acceleration.

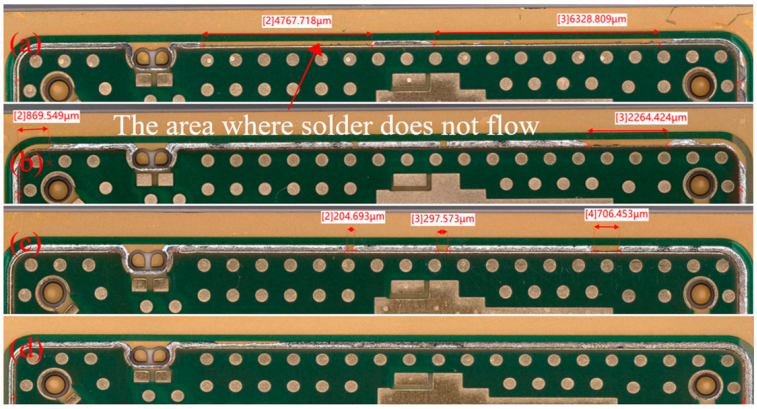


Figure 18. Solder Overflow of HDI Substrate at Eutectic Temperature of 285 °C under Different Pressures: (**a**) 0.5 kPa; (**b**) 1 kPa; (**c**) 1.5 kPa; (**d**) 3 kPa.

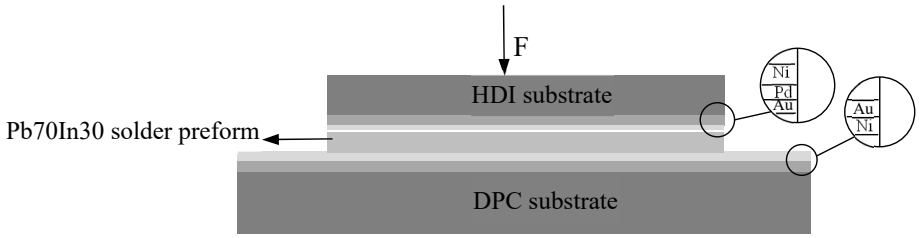


Figure 19. Schematic of Eutectic Bonding Structure.

3.3. Physical Verification

Based on the simulation optimization results, the HDI substrate was designed with the following thickness specifications: the inner two copper layers at 40 μm; the top and bottom copper layers at 30 μm and 40 μm, respectively; the top, inner, and bottom dielectric layers at 50 μm, 100 μm, and 50 μm, respectively; and the front-side solder mask layer at 25 μm. The difference in copper-fill ratio between symmetric copper layer pairs (Layer 1 & Layer 4 and Layer 2 & Layer 3) in the HDI substrate was controlled within 5%, and the cavities/slots were designed in a distributed symmetric pattern. Ten optimized HDI substrates were selected for thermal deformation testing. Warpage data were collected at 31 points along the corresponding temperature profile. The warpage variation with temperature for a single HDI substrate is shown in Figure 20. Statistical data on the warpage of 10 HDI substrates were collected, and the actual thermal deformation test results are shown in Figure 21. It can be observed from the figure that the warpage of the optimized HDI substrates is below 80 μm, meeting the requirements for subsequent stacked assembly.

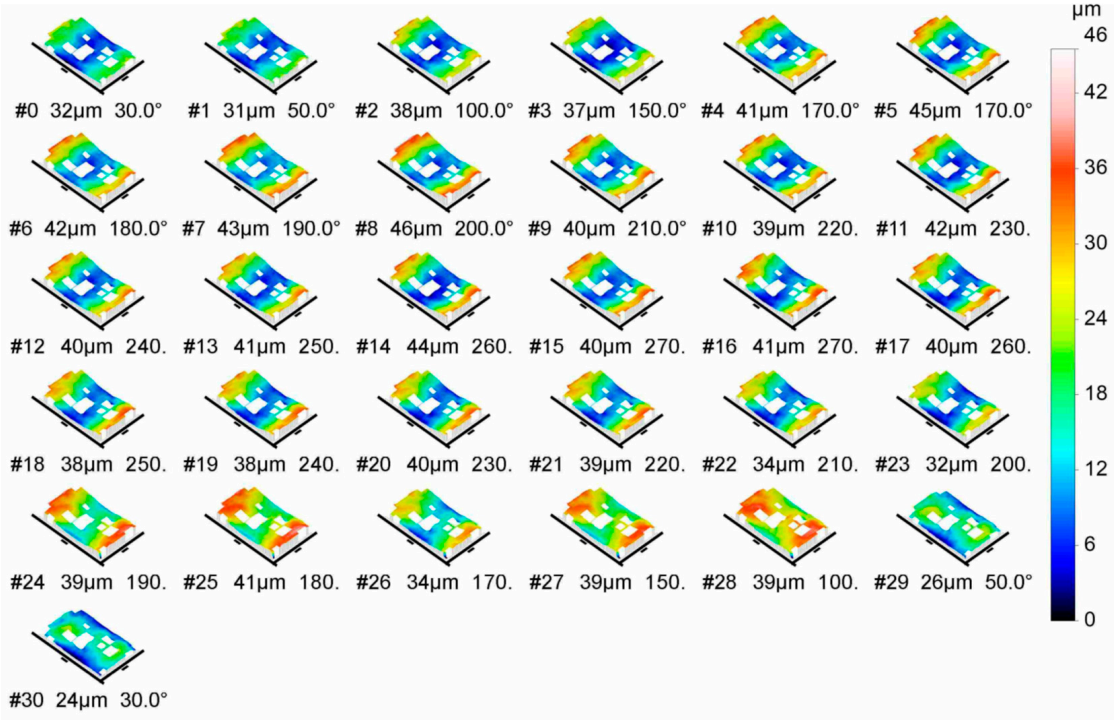


Figure 20. Thermal Deformation Test Results of a Single HDI Substrate. Note: In the figure, "#" represents the number corresponding to each test temperature value, "μm" indicates the maximum warpage of the HDI substrate at that specific test temperature, and "°" denotes the test temperature.

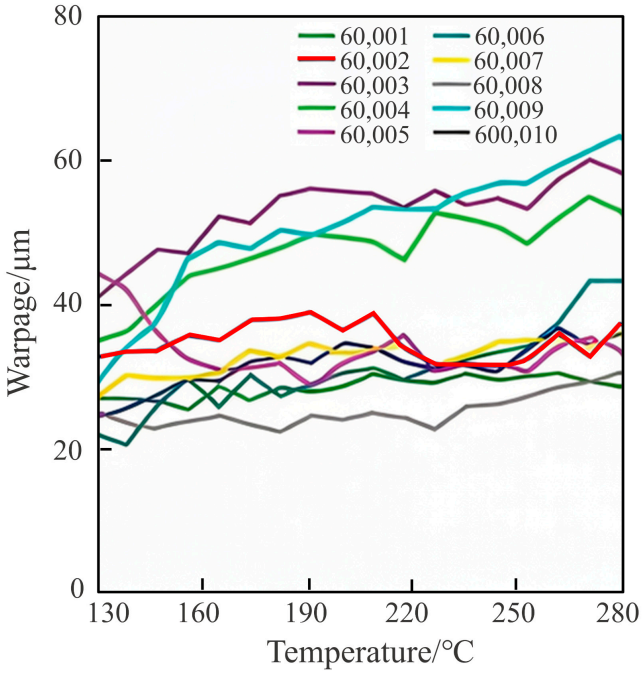


Figure 21. Statistical data of actual thermal deformation test results for 10 HDI substrates.

Based on the optimized eutectic process parameters, the N_2/H_2 mixture was selected as the reducing atmosphere, the eutectic temperature was set to 285 °C, and the pressure was set to 1.5 kPa to complete the large-area eutectic bonding between the lower HDI substrate and the DPC substrate. After ball placement, the upper HDI substrate was stacked and bonded to the lower HDI substrate. The gold-plated pads on the HDI substrate showed no contamination, the eutectic void percentage was less than 10% (Figure 22a), and

no defective or missing solder joints occurred in the inter-layer BGA stacking of the HDI substrates (Figure 22b).

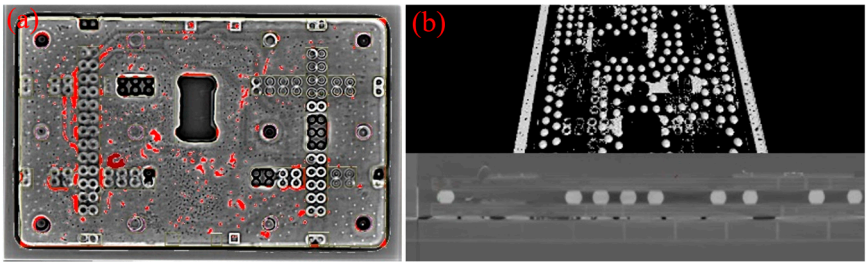


Figure 22. X-Ray Images of HDI Substrates after Stacking and Soldering: (**a**) Void Condition (Red); (**b**) Inter-Layer BGA Stacking and Soldering Condition.

4. Conclusions

In ceramic hermetic dual-stacked SiP packages, the large-area eutectic bonding of the lower HDI substrate is fundamental to product miniaturization. This study investigated thermal mismatch, solder joint contamination, and void formation during eutectic bonding of the lower HDI substrate using the Pb70In30 solder. The following process solutions are proposed, providing further guidance for the packaging process design of ceramic-packaged, dual-layer-stacked SiPs:

(1) Thermal mismatch: Through simulation optimization of copper layer thickness, dielectric layer thickness, and cavity/slot distribution, the warpage of the optimized HDI substrate was reduced to below 80 μm, satisfying the requirements for subsequent stacking assembly.

(2) Solder joint contamination: Flux pretreatment of Pb70In30 solder preforms combined with vacuum eutectic bonding in a N_2/H_2 mixture effectively removes surface oxides, prevents solder joint contamination, and meets the requirements for subsequent gold-wire bonding.

(3) Void formation: By optimizing the eutectic process parameters (eutectic temperature, 285 °C; eutectic pressure, 1.5 kPa), the void percentage was reduced to below 10%, the shear strength reached 23.66 MPa, and the solder overflow exceeded 90%, satisfying the requirements for large-area eutectic bonding.

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Conflicts of Interest: Authors Mingqi Gao, Dongyang Lei, Huijie Ye, Yanming Zhang, Ce Zeng, Hai Jiang, Qian Lu, Yueyou Yang and An Zhang are employed by China Electronics Technology Group Corporation. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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