

Article

Low-Cost Active Power Filter Using Four-Switch Three-Phase Inverter Scheme

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Abstract: Shunt active power filters (SAPFs) have been around for a long time. They improve the quality of a current drawn from the grid when feeding non-linear loads formed by old-fashioned power electronic converters such as uncontrolled and controlled rectifiers. Most SAPFs are implemented using the well-known six-switch three-phase inverter (SSTPI) topology. This paper investigates the capability of adopting the four-switch three-phase inverter (FSTPI) scheme to develop low-cost SAPFs, mainly for low-power ranges. The performance of the proposed SAPF using the FSTPI topology is compared with the conventional scheme of an SAPF formed by the six-switch three-phase inverter (SSTPI) topology. Qualitative and quantitative analyses are conducted. The performance of the proposed FSTPI-based SAPF is investigated under different loading conditions. The obtained results indicate the validity and effectiveness of the FSTPI scheme in improving the quality of currents drawn from the AC grid. The SAPF scheme investigated is also feasible and results in cost reduction when the SAPF power circuit is constructed with modern WBG devices, such as SiC-based MOSFETs, which are relatively expensive (approximately three times the price of the equivalent Si IGBTs).

Keywords: active power filter; shunt active power filter; APF; SAPF; four-switch inverter; FSTPI; PSIM; non-linear load; FFT



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1. Introduction

The concept and idea of active power filters (APFs) based on current injection into the grid to offset undesired load harmonics were proposed several decades ago [1]. However, this topic is still of considerable interest for investigation [2–13]. The main idea of APFs is to inject a current into the electric grid (AC source) at the point of common coupling (PCC) to cancel out the undesired harmonics caused by non-linear loads which are fed from the AC source. The compensating currents injected by the APF must have the same amplitude and the opposite phase to the undesired harmonic components of the non-linear load. Consequently, the resultant grid currents are sinusoidal waveforms and in-phase with the grid voltages for unity PF operation [2,3]. Mainly, the control system of the APF should guarantee a good current tracking capability and low total harmonic distortion (THD) in the grid currents. In addition to this, it should provide good DC bus voltage regulation. Therefore, successful APFs accomplish harmonic standards, such as IEEE 519, improving the power quality requirements [2]. Several efforts have been carried out to study and investigate the performance of active power filters. In Ref. [1], detection and control techniques for harmonic currents were addressed. It also introduced modeling and stability analysis methods for the multi-parallel SAPF system. In Ref. [3], a shunt hybrid active power filter for 1 kV mining applications was implemented. The control technique involved

time delay compensation and voltage distortion compensation. Refs. [4,5] presented various control techniques for APFs. In Ref. [4], a feedback-linearization-type approach to control the currents of an APF was presented. It included a DC-side voltage control loop beside the current control loop. The main feature of the proposed control method was the compensation of the time delay caused by microcontroller computation using a finite impulse response predictor.

In Ref. [5], a deadbeat-based direct power control method to generate a reference current and control of the active power filter was proposed. The THD of the steady-state grid current was reduced from 22% to 3%. In [6], an adaptive DC-link voltage control for shunt active power filters was proposed. The method was based on the model predictive current control approach. The proposed control method could regulate the DC-link voltage according to grid voltage fluctuations. In references [7–9], active power filters were controlled under unbalanced electric grid conditions. The control technique in [7] relies on the modular fundamental element detection method, which can manage the mitigation of harmonic currents under an unbalanced and/or distorted grid. In [8], a Kalman filter was employed to obtain the fundamental sequence component of the grid voltage. Meanwhile, in [9], the controller of the shunt active power filter required only current measurements without any voltage measurements. The THD of the grid currents was reduced to a satisfactory level. On the other hand, evolutionary search algorithms have been employed for the control of active power filters, as investigated in [10]. Recently, an artificial intelligence approach was employed for the control of active power filters. Ref. [11] proposed a machine learning-based controller for a shunt active power filter. It can be considered as a universal machine learning controller that can generate reference currents for an active power filter. Moreover, the sliding mode control technique was applied for the control of active power filters, as presented in [12]. On the other hand, the pioneer contributions and early works of the four-switch three-phase inverter (FSTPI) topology were addressed in references [13–18], where modulation techniques for the FSTPI scheme were proposed. The results demonstrated that the FSTPI topology would be competitive compared to the commonly used six-switch three-phase inverter (SSTPI) scheme in the low-power range. Recently, the FTPI topology was utilized to develop active power filters, as indicated in [19]. Authors in [19] adopted the fundamental positive sequence extraction method, which does not require a phase-locked loop or complex coordinate transformation. On the other hand, generation methods for reference currents for SAPFs have received great attention from researchers. Various methods have been developed to operate shunt active power filters [20–24]. All research activities aim to accomplish the existing IEEE standards of [25–27]. Thus, the current injected by APFs should result in an overall current drawn from the AC mains that satisfies the criteria of these IEEE standards.

The DC bus voltage is well-regulated using conventional or improved PI controllers, where the output of the voltage controller represents the reference signal of the grid current. References [28–30] addressed some efficient harmonic extraction algorithms and methods to generate reference grid current signals based on the extraction of the first harmonic of the load currents.

The rest of the paper is organized as follows: Section 2 summarizes the main objectives and contributions of the paper. Section 3 presents the principles and main concept of the shunt active power filter. Section 4 explains the generation methods for reference grid currents. Section 5 addresses the principle of operation of the FSTPI. Section 6 presents the investigated schemes of the SAPF, while Section 7 presents some simulation results of different operating conditions, including qualitative and quantitative assessments. Section 8 includes the conclusions and findings. Tables of abbreviations and symbols are provided as well. Finally, a list of references is provided.

2. Objective and Contribution of the Paper

2.1. Main Objective

This paper investigates the performance of a shunt active power filter (SAPF) using a four-switch three-phase inverter (FSTPI) topology to develop a high-performance SAPF with reduced cost. A comparison between the conventional six-switch three-phase inverter (SSTPI) scheme is carried out. Based on the results, the feasibility of such an SAPF scheme can be assessed.

2.2. Main Contribution

The FSTPI-based SAPF system is studied in different operating conditions, including a highly inductive nonlinear load, highly distorted load, and unbalanced nonlinear load. A comprehensive performance analysis of the investigated SAPF scheme, including qualitative and quantitative assessments, is made. In addition, the proposed SAPF scheme is compared with the conventional SSTPI-based SAPF topology to determine to which degree the proposed scheme is successful and feasible.

3. Concept of Shunt Active Power Filter

The three-phase SAPF injects currents into the electric grid that cancel out undesired harmonics caused by non-linear loads fed from the AC source [3]. The SAPF compensating currents have the same amplitude and are out of phase with the harmonic components caused by the non-linear load. Consequently, this results in a sinusoidal grid current by the power quality standards. A simplified block diagram of the shunt active power filter is illustrated in Figure 1, where the SAPF injects currents into the grid that compensate for or eliminate the effect of non-linear loads such that the net currents drawn from the AC supply are near sinusoidal waveforms with a minimum possible THD.

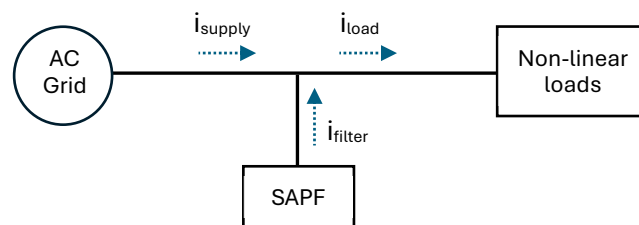


Figure 1. Block diagram of the shunt active power filter system.

Thus, Equations (1) and (2) are valid, as follows:

$$i_{supply} + i_{filter} = i_{load} \quad (1)$$

$$i_{filter} = i_{load} - i_{supply} \quad (2)$$

A circuit diagram of a typical SAPF system is shown in Figure 2, where the power circuit of the SAPF is based on the conventional SSTPI (B6) topology. The non-linear load would be equipment or an appliance that is fed from an uncontrolled rectifier. Also, it can be a DC drive, fed from a SCR phase-controlled converter. Such non-linear loads deteriorate the power quality of the AC grid in terms of the line current harmonic content, high THD of the line currents, and spikes superimposed on the grid voltage. The reference filter currents are computed using Equation (3), as follows:

$$\begin{bmatrix} i_{fa}^* \\ i_{fb}^* \\ i_{fc}^* \end{bmatrix} = \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} - \begin{bmatrix} i_{sa}^* \\ i_{sb}^* \\ i_{sc}^* \end{bmatrix} \quad (3)$$

where i_{fa}^* , i_{fb}^* , and i_{fc}^* are the reference filter currents; i_{La} , i_{Lb} , and i_{Lc} are the instantaneous values of the load currents; and i_{sa}^* , i_{sb}^* , and i_{sc}^* are the reference grid currents. The actual SAPF filter currents can be controlled using hysteresis current controllers to track (follow up) their corresponding reference values. The hysteresis current controller can be a conventional ON–OFF controller with a tolerance band or a PI controller incorporated with a PWM to operate at a fixed switching frequency (to be discussed later in Section 6).

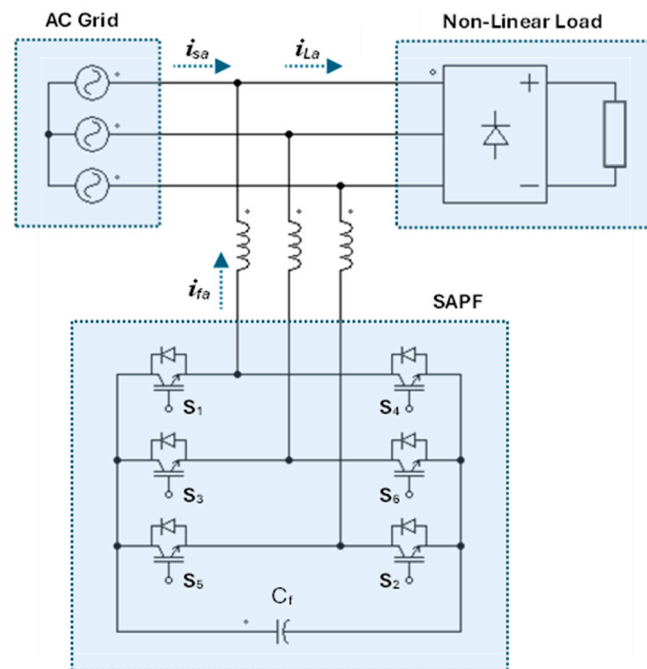


Figure 2. Circuit diagram of a typical SAPF system.

If the reference grid currents are sinusoidal signals with optimum amplitudes, the corresponding reference filter currents will be the difference between the load currents and the reference grid currents (sinusoidal signals). Hence, the instantaneous values of the filter currents that are injected into the grid result in sinusoidal grid currents with a satisfactory THD and well attenuated harmonic content that matches the existing standards [25,26].

4. Reference Grid Currents Generation Methods

The control system of the SAPF consists of the following parts (units): (1) the generation of the reference grid (supply) current; (2) the generation of the reference compensating current of the SAPF; (3) current controllers of the voltage source PWM converter; and (4) the voltage controller of the DC bus voltage of the voltage source PWM converter (when the DC bus is a DC capacitor not a DC supply). The generation of reference compensating current plays an important role that affects the filtering performance, since any reference compensating currents with an inaccurate phase or magnitude can result in degradation in the compensation process. Various methods have been proposed to generate these reference signals. Harmonic current detection techniques and harmonic current control techniques were addressed in [1], where the advantages and disadvantages of various algorithms were presented.

One main approach is based on the closed-loop control of the DC link voltage of the SAPF, as explained in [20–22]. Others generate reference signals based on the extraction of the first harmonic of the load currents, as proposed in [28–30].

4.1. Based on Closed-Loop Control of DC Link Voltage of the SAPF

The DC link side of the SAPF “capacitor voltage” is regulated using a closed-loop controller. Well-known PI controllers with a limited output are usually employed. Recently, fractional-order PI controllers can be employed as well. The output of the voltage controller is considered the reference amplitude, with the “maximum value” of the current to be drawn from the supply. To generate the three-phase sinusoidal reference signals, three-phase unity sinusoidal waveforms are employed, as illustrated in Figure 3.

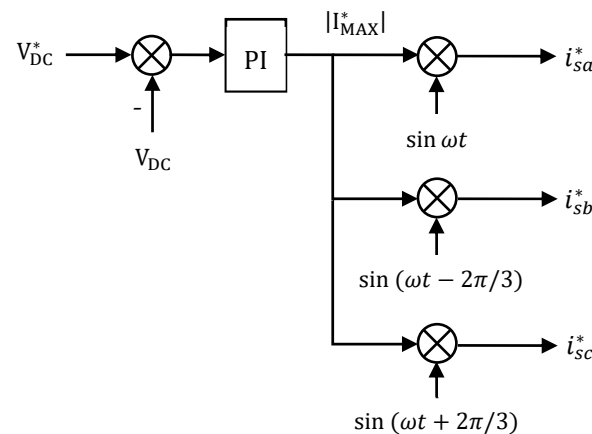


Figure 3. Generation of reference grid currents from the closed-loop control of the DC link voltage.

The method shown in Figure 3 is simple to implement. However, in the case of severe supply voltage distortion, PLLs can be utilized to generate the reference sinusoidal waveforms of the grid currents. Once the reference grid currents are calculated, they can be utilized to generate the reference filter current owing to Equation (3).

4.2. Based on Calculation of the First Harmonics of the Load Current

The reference grid current is computed based on the extraction of the fundamental component of the non-linear load current, where the reference grid currents (i_{sa}^* , i_{sb}^* , i_{sc}^*) equal the calculated fundamental components of the load current (i_{La1} , i_{Lb1} , i_{Lc1}), respectively, as shown in Figure 4. Several efficient harmonic extraction algorithms with good accuracy have been proposed, such as the methods of references [29,30].

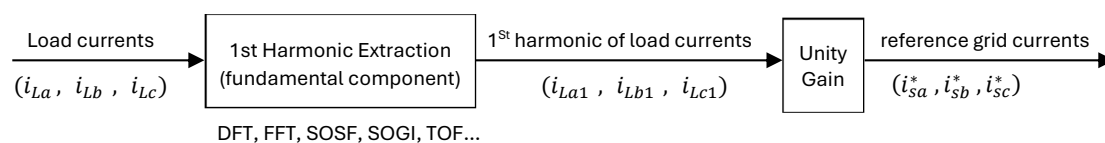


Figure 4. Generation of reference grid currents by computing the fundamental component of the load current.

Harmonic extraction techniques are carried out in the time domain or the frequency domain [31]. The well-known or commonly used frequency domain-based methods are Discrete Fourier Transform (DFT) or the Fast Fourier Transform (FFT), Second-Order Sequence Filter (SOSF), Second-Order Generalized Integrator (SOGI), and others. Time-domain-based methods such as Instantaneous Reactive Power Theory (IRPT) and Synchronous Reference Frame are also applied in SAPFs.

Recently, a method based on Trigonometric Orthogonal Function (TOF) was proposed [29].

Apart from the method employed for reference grid current generation, current controllers are used to control the operation of SAPFs. Figure 5 demonstrates two types of

current controllers that are commonly used in the control of the operation of three-phase VSI inverters and active power filters.

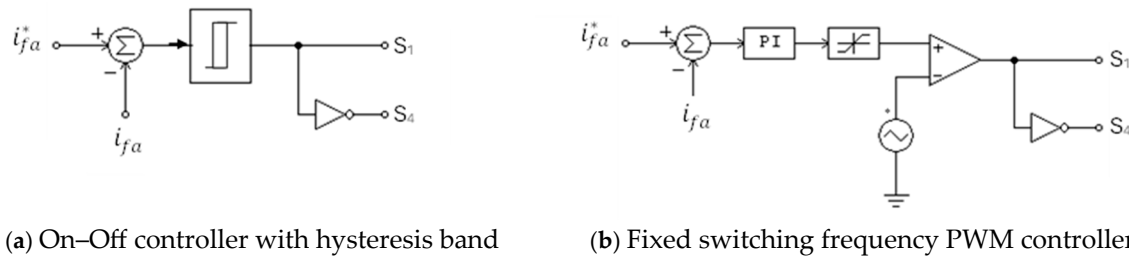


Figure 5. Possible current controllers for SAPF currents.

The first type shown in Figure 5a is an ON–OFF controller with a predefined hysteresis (tolerance) band that can be set to any desired value. With this controller, the resultant switching frequency is not constant. If the hysteresis band is set to a value of zero or a small value, the resultant switching frequency will be very high, which increases the switching losses. Sometimes, it can burn the power transistors. The second type shown in Figure 5b provides an operation of PWM controller at a fixed switching frequency based on the frequency of the carrier signal (triangular waveform). Thus, this type provides a better performance.

5. Principle of Operation of FSTPI

The FSTPI (B4) topology is composed of four power switches (transistor and antiparallel diode) forming two branches, while the third branch is formed by two identical capacitors. Figure 6 illustrates a circuit diagram of the FSTPI.

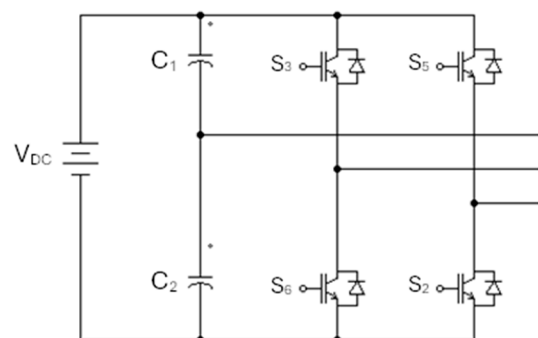


Figure 6. Power circuit of a four-switch 3-Φ inverter (FSTPI).

From the current point of view, for a balanced three-phase load, if the currents in the second and third phases (i_b and i_c) are controlled to be sinusoidal with a phase shift of 120° electrically from each other (See Figure 7), i.e., when i_b^* and i_c^* are sinusoidal, the current in the first phase (i_a), which is connected to the capacitors, will be forced to be sinusoidal owing to the Equations (4) and (5) given as follows:

$$i_a + i_b + i_c = 0 \quad (4)$$

$$i_a = -(i_b + i_c) \quad (5)$$

Thus, theoretically, the function and operation of the SAPF can be carried out successfully using the FSTPI topology. In this case, the currents i_{fb} and i_{fc} (injected from the SAPF) are controlled using hysteresis current controllers. Hence, the current in the first phase (i_{fa}) is indirectly regulated to have the same waveform as the two other phases b and c.

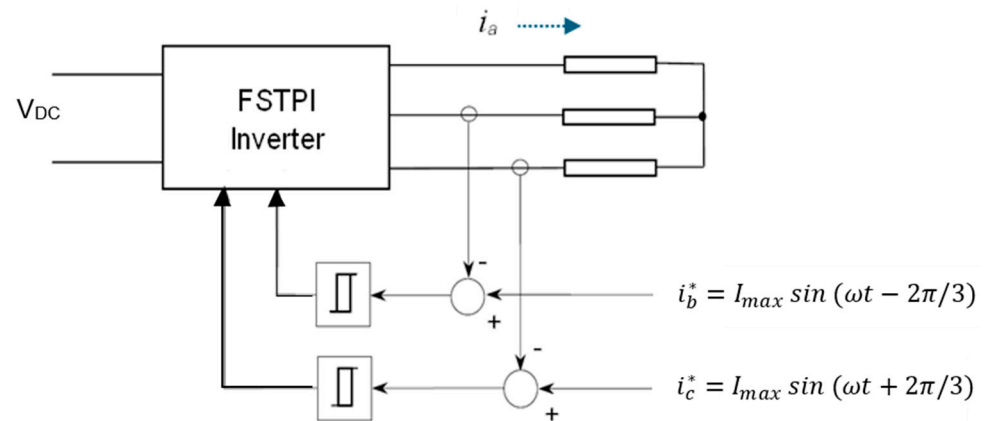


Figure 7. Simple current control of an FSTPI.

Adopting the FSTPI scheme in SAPFs results in a reduction in the number of the required isolation/driver circuits and isolated power supplies from six to four circuits. Thus, a saving of 33% in the number of power switches and the corresponding auxiliary electronic circuits is achieved. Moreover, the system will require a reduced number of Hall effect current transducers, which reduces the overall cost of the SAPF as well. The extent of savings is clear when SiC power transistors are utilized to construct the SAPF power electronic circuit (converter power circuit) due to their relatively higher prices (almost three times the price of Si-based counterparts with the same rating). The voltage space vector of the four-switch 3- Φ inverter is computed using Equation (6), as follows:

$$\bar{V}_S = \frac{2}{3} V_{DC} \left(0.5 + e^{j2\pi/3} S_3 + e^{j4\pi/3} S_5 \right) \quad (6)$$

When the previous equation is resolved in the $(\alpha-\beta)$ system of coordinates, the following components in the stationary reference frame are obtained by Equations (7) and (8):

$$v_\alpha = \frac{V_{DC}}{3} [1 - S_3 - S_5] \quad (7)$$

$$v_\beta = \frac{v_{bc}}{\sqrt{3}} = \frac{V_{DC}}{\sqrt{3}} [S_3 - S_5] \quad (8)$$

Since the inverter is composed of four switches, only four switching states are available. Applying the Park transformation to the inverter output voltage yields the following facts:

1. The inverter provides only four active vectors [17].
2. The vectors are not equal. They have different magnitudes.
3. The vectors are displaced by 90 degrees electrically from each other [18].
4. The inverter does not provide any zero/nil vectors [17,19].

6. Investigated Schemes of SAPFs with FSTPI and SSTPI Using PSIM

6.1. Hardware Modeling in PSIM

This paper utilized PSIM hardware simulation and design software to study and investigate the FSTPI-based SAPF. The power circuit of the system is illustrated in Figure 8. It is composed of the following three main parts: AC supply including grid impedance, non-linear load (3- Φ uncontrolled rectified feeding R-L load), and the SAPF formed by the FSTPI scheme, including a DC bus capacitor.

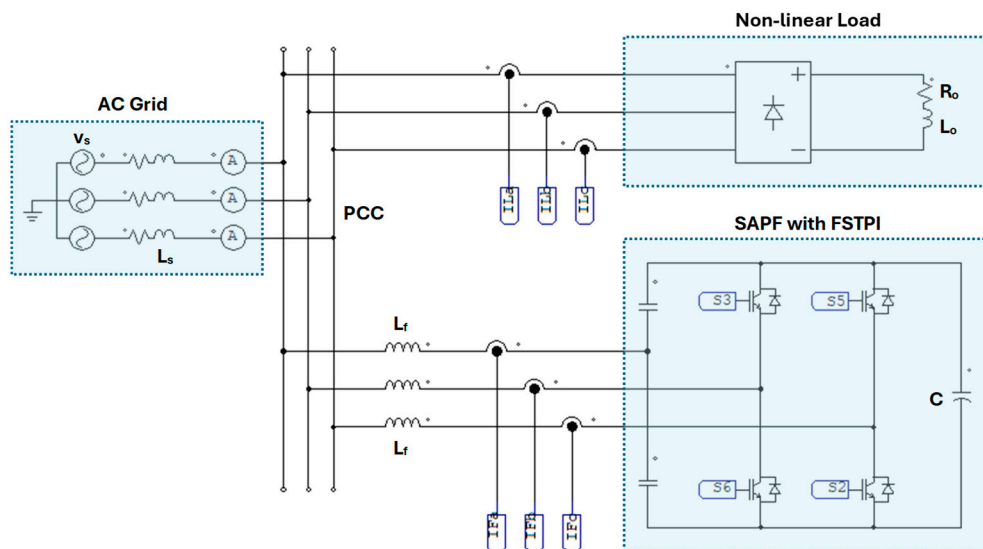


Figure 8. Power circuit of the investigated FSTPI-based SAPF in PSIM.

The closed-loop control unit of the DC link voltage of the SAPF, including the reference current generation of the AC grid, is shown in Figure 9, while the corresponding SAPF reference currents' generation and current controllers are illustrated in Figure 10. In this paper, the individual current controller is based on a PI controller and SPWM unit to generate the switching signals of the power transistors.

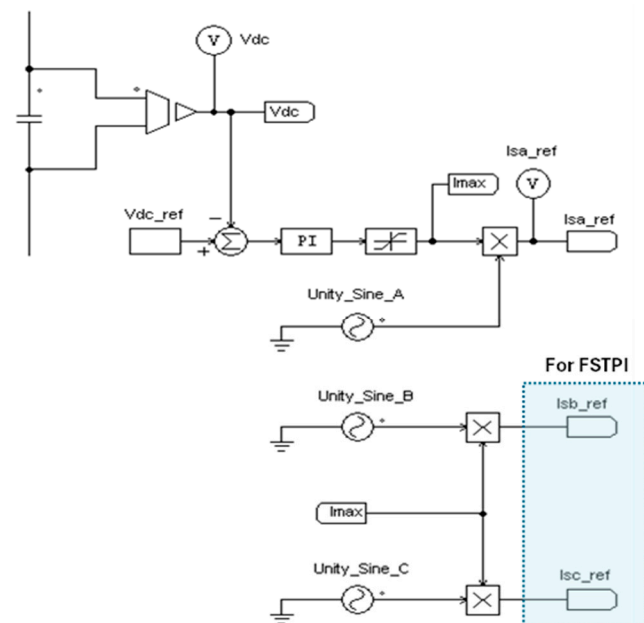


Figure 9. Closed-loop control unit of the DC link voltage developed in PSIM.

Both units of Figures 9 and 10 are designed and developed in PSIM to operate with both types of inverters, SSTPI and FSTPI, as the paper performs a comparison between both SAPF schemes. Accordingly, in the upper part of Figure 9, the signal label (I_{sa_ref}) is the reference grid current of phase A when the SSTPI scheme is utilized. Similarly in Figure 10, the signal labels (S1 and S4) represent the generated switching signals of the first arm of the SSTPI. This means that the operation of the FSTPI needs only four switching signals (S3, S6, S5, and S2), as illustrated in the lower part of Figure 10. The gains of the PI controllers are determined as explained in the next sub-section.

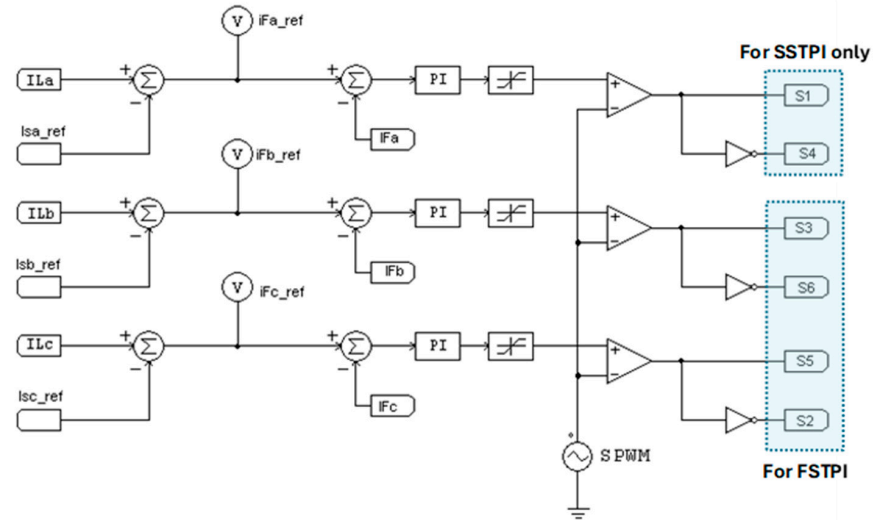


Figure 10. SAPF reference currents' generation and current controllers developed in PSIM.

6.2. Design of PI Controllers

From Figures 9 and 10, it can be indicated that the SAPF system has two control loops, a DC link voltage control loop (outer loop) and SAPF currents control loop (inner loop). A block diagram of the SAPF control system is illustrated in Figure 11. The system has the following two main controllers: a DC link voltage controller and SAPF current controllers. In the case of the FSTPI, the SAPF has two similar current controllers (to control the two phases' currents i_{Fb} and i_{Fc}), while in the case of the SSTPI, the SAPF has three similar controllers (to control the three phase currents i_{Fa} , i_{Fb} , and i_{Fc}). In general, several types of controllers can be employed to regulate both the outer and inner control loops. Conducting a comparative study of different types of controllers to determine which type is the best is outside of the scope of this paper.

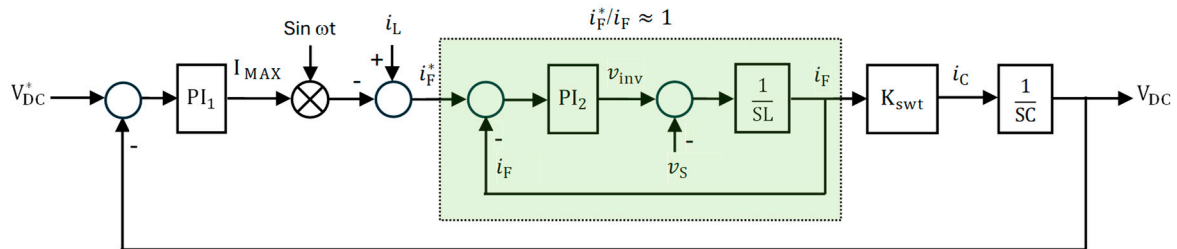


Figure 11. Voltage and current control loops of SAPF.

a. Outer control loop (voltage control loop):

As a control system, the simplified voltage control loop of the SAPF is shown in Figure 12. Since the VSI operates at a high switching frequency, the filter currents (i_{Fa} , i_{Fb} , and i_{Fc}) are almost equal to the magnitudes of their reference values (i_{Fa}^* , i_{Fb}^* , i_{Fc}^*), respectively. Therefore, it can be assumed that the transfer function of the closed-loop current controller (i_F^*/i_F) is almost unity [32]. K_{swt} represents the inverter switching function to correlate the DC link current with the filter currents.

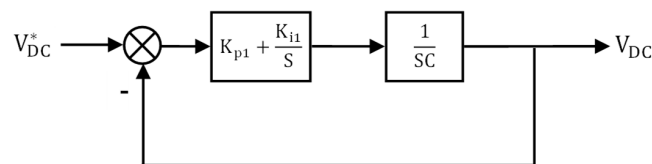


Figure 12. Simplified DC voltage control loop of SAPF.

The transfer function of the PI voltage controller is given by Equation (9), as follows:

$$G_{pi1}(S) = K_{p1} + \frac{K_{i1}}{S} \quad (9)$$

Accordingly, the closed-loop transfer function will have the following formula:

$$T_v(S) = \frac{SK_{p1} + K_{i1}}{CS^2 + SK_{p1} + K_{i1}} \quad (10)$$

The gains K_{p1} and K_{i1} can be computed by comparing the characteristic equation of $T_v(S)$ with the standard form and solving for proper values of ζ_1 and ω_{n1} .

Thus,

$$K_{p1} = 2\zeta_1\omega_{n1}C \quad (11)$$

$$K_{i1} = C\omega_{n1}^2 \quad (12)$$

Thus, choose suitable values of ζ_1 and t_s or ω_{n1} to obtain the numerical values of K_{p1} and K_{i1} . E.g., the damping ratio ζ_1 can be set to a value between 0.5 and 0.7, while the natural frequency ω_{n1} can be selected based on the rise time or the settling time.

The numerical values of K_{p1} and K_{i1} obtained based on the previous method can be considered as good initial estimates for these gains. They can be tuned either manually or by applying any evolutionary search algorithms to achieve the optimum desired response (see Appendix A for complete derivation).

b. Inner control loop (current control loop):

The inner current control loop is shown in Figure 13. The output is the maximum value of the grid current. Several types of current controllers can be utilized such that the actual grid currents track and follow their reference values. The commonly used method is an ON–OFF current controller with a hysteresis band. However, the resultant switching frequency is not constant. In this paper, a PI controller and current controller are utilized for two reasons. Firstly, to obtain a fixed switching frequency. Secondly, to be able to make a fair comparison between the FSTPI and SSTPI schemes operating at the same switching frequency and in the same operating conditions (supply voltage and loading conditions).

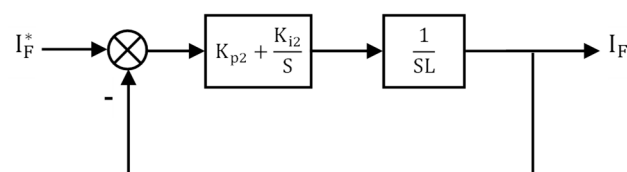


Figure 13. Simplified inner current control loop of SAPF.

Similarly, the closed-loop transfer function will have the following formula:

$$T_i(S) = \frac{SK_{p2} + K_{i2}}{LS^2 + SK_{p2} + K_{i2}} \quad (13)$$

Comparing the characteristic equation of $T_i(S)$ with the standard form and solving for proper values of ζ_2 and ω_{n2} yields the following formulas for K_{p2} and K_{i2} :

$$K_{p2} = 2\zeta_2\omega_{n2}L \quad (14)$$

$$K_{i2} = L\omega_{n2}^2 \quad (15)$$

Hence, choose suitable values of ζ_2 and t_{s2} or ω_{n2} to obtain the numerical values of K_{p2} and K_{i2} . E.g., the damping ratio (ζ) can be set to a value between 0.5 and 0.7, while

the natural frequency ω_{n2} can be selected based on the rise time or the settling time. As mentioned before for the voltage control loop, the numerical values of K_{p2} and K_{i2} obtained based on the previous approach can be considered as good initial estimates that can be tuned either manually or by applying any evolutionary search algorithms to achieve a satisfactory response. Detailed derivations of the previous equations are presented in Appendix A.

6.3. Simulation Parameters

The simulation parameters of the developed PSIM programs of the investigated SAPF scheme are summarized in Table 1. The switching technique incorporated with the current controller is SPWM operating at a switching frequency of 10.02 kHz, which yields an odd frequency ratio of 167.

Table 1. Simulation parameters.

Parameter	Value
AC supply (v_s)	3- Φ : 208 V/60 Hz
DC bus capacitor (C)	4 mF
FSTPI capacitors (C_1, C_2)	1 mF
Total inductance ($L = L_f + L_s$)	4 mH
Switching strategy	SPWM
Switching frequency (F_{SWT})	10.02 kHz
Solver time step	5 μ s
DC link voltage (V_{DC})	600 V

7. Obtained Results and Discussions

This section presents some simulation results of the SAPF driven by both the FSTPI and SSTPI under different loading conditions. The conducted study includes a quantitative analysis of the obtained results. A comparison between both schemes is made as well. The investigated nonlinear loads are as follows: (1) a three-phase diode bridge rectifier feeding a highly inductive load; (2) a three-phase diode bridge rectifier feeding a capacitive load to assess the system under a highly distorted waveform; and (3) three single-phase unbalanced non-linear loads formed by three single-phase diode bridge rectifiers loaded with unequal capacitive loads.

7.1. (Nonlinear Load): 3- Φ Diode Bridge Rectifier Feeding a Highly Inductive Load

a. SAPF with FSTPI Scheme.

The performance of the SAPF operated with the FSTPI is illustrated in Figure 14, where the nonlinear load current of the phase a (i_{La}) is depicted in Figure 14a. The corresponding injected filter current (i_{Fa}) is drawn in Figure 14b, while the resultant waveform of the supply current (i_{sa}) and its harmonic spectrum are shown in Figure 14c,d, respectively. The obtained results indicate that the SAPF driven by the FSTPI operates properly and is effective in improving the current drawn from the AC supply. The harmonic spectrum contains odd harmonics (3, 5, 7...) with negligible magnitudes compared with the fundamental component (60 Hz). The low-order harmonic (third order of 180 Hz) has a magnitude of 0.68% of the fundamental component.

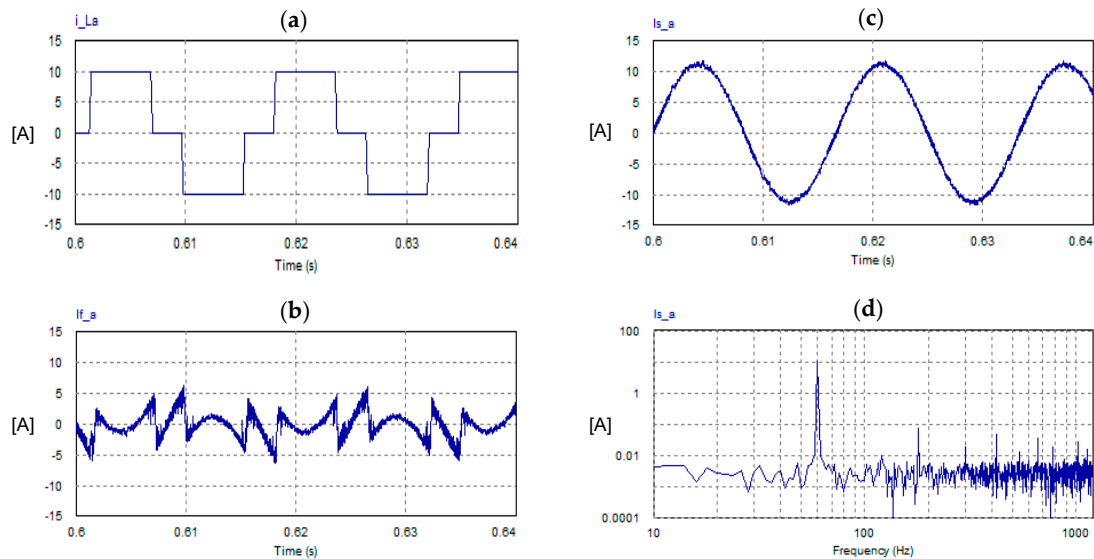


Figure 14. Performance of SAPF using FSTPI scheme: (a) nonlinear load current i_{La} ; (b) injected filter current i_{Fa} ; (c) resultant supply current i_{sa} ; and (d) harmonic spectrum of supply current i_{sa} .

b. SAPF with SSTPI Scheme.

The performance of the SAPF operated with the conventional SSTPI is illustrated in Figure 15, where the nonlinear load current of the phase a (i_{La}) is depicted in Figure 15a. The corresponding injected filter current (i_{Fa}) is drawn in Figure 15b, while the resultant waveform of the supply current (i_{sa}) and its harmonic spectrum are shown in Figure 15c,d, respectively.

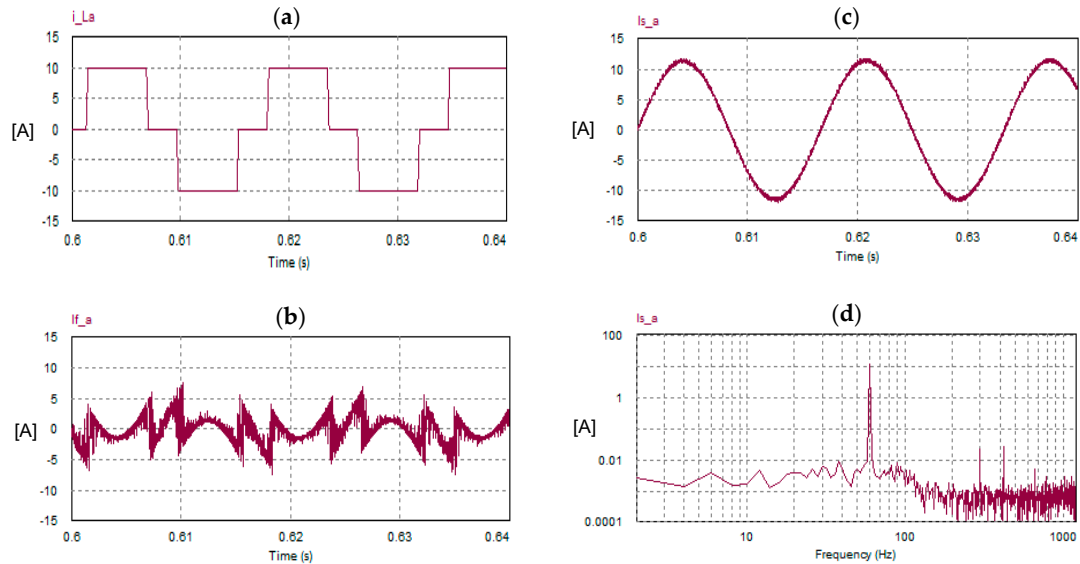


Figure 15. Performance of SAPF using SSTPI Scheme: (a) Nonlinear load current i_{La} ; (b) injected filter current i_{Fa} ; (c) resultant supply current i_{sa} ; and (d) harmonic spectrum of supply current i_{sa} .

The obtained results indicate that the SAPF driven by the FSTPI is competitive compared to the conventional SAPF scheme driven by the SSTPI. However, the SSTPI provides a relatively superior performance in terms of a lower THD and harmonic content, as explained later in the comparison part (Section 7.3).

c. Comparison with SSTPI Scheme.

Qualitative and quantitative assessments of both SAPFs are made to evaluate their performances and determine to which degree the proposed SAPF with the FSTPI scheme is successful and competitive compared to the conventional scheme.

In Figure 16, the three-phase supply currents of both schemes are depicted. The results demonstrate the sufficient quality of the current waveforms drawn from the grid under the FSTPI-based SAPF. The corresponding harmonic spectra are illustrated in Figure 17, where both schemes result in almost the same amplitude of the fundamental components. However, the AC grid currents under the SSTPI have better harmonic content compared with the FSTPI scheme.

The steady-state harmonic spectra of the DC link voltage with both schemes are illustrated in Figure 18. The results indicate the superior performance of the SSTPI in terms of lower harmonic content. In the case of the FSTPI scheme, the dominant low-order harmonic (LOH) pulsates at the grid frequency (60 Hz). Meanwhile, the dominant LOH in the case of the SSTPI scheme pulsates at six times the line frequency (360 Hz). Also, it can be observed that the harmonic spectrum of the DC link voltage with the FSTPI scheme has second, fourth, and fifth harmonics with relatively higher amplitudes compared with that of the SSTPI scheme.

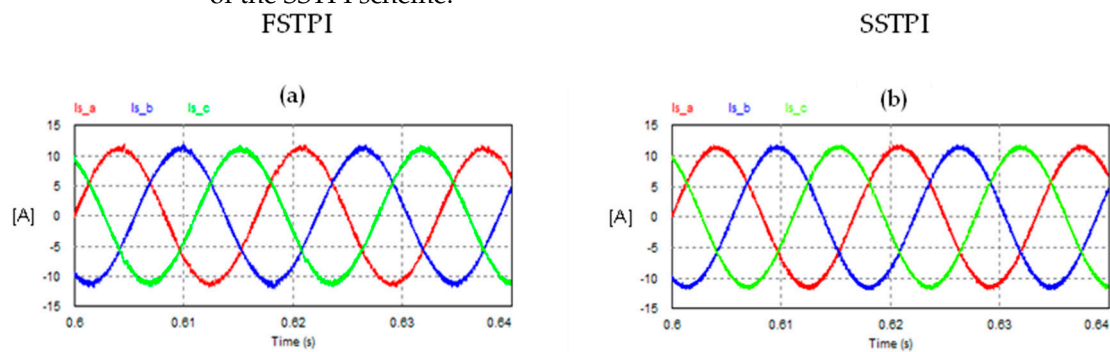


Figure 16. 3- Φ supply currents (i_{sa} , i_{sb} , and i_{sc}) with both SAPF schemes: (a) FSTPI and (b) SSTPI.

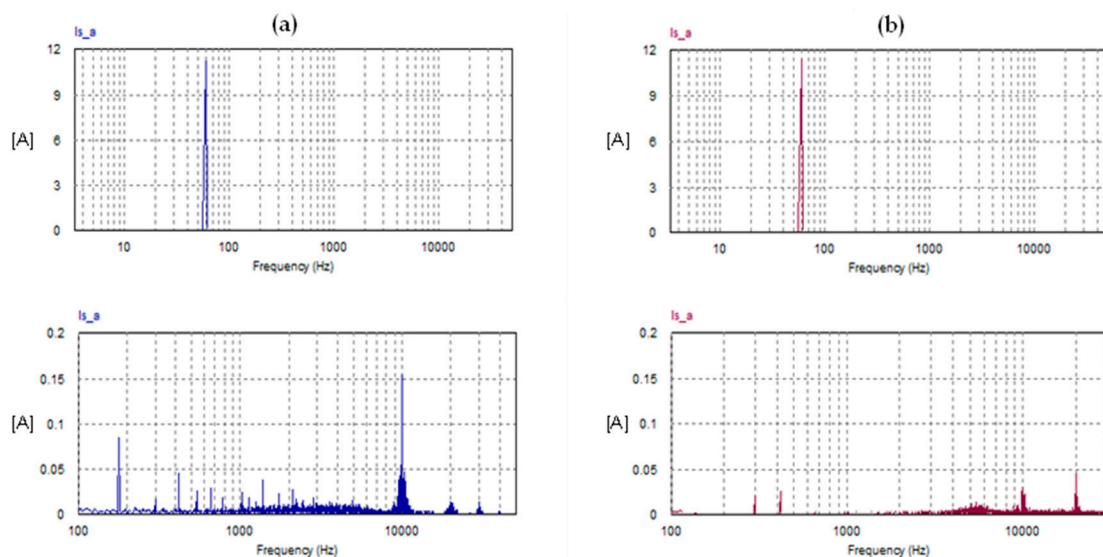


Figure 17. Harmonic spectrum of supply current i_{sa} with both SAPF schemes: (a) FSTPI and (b) SSTPI.

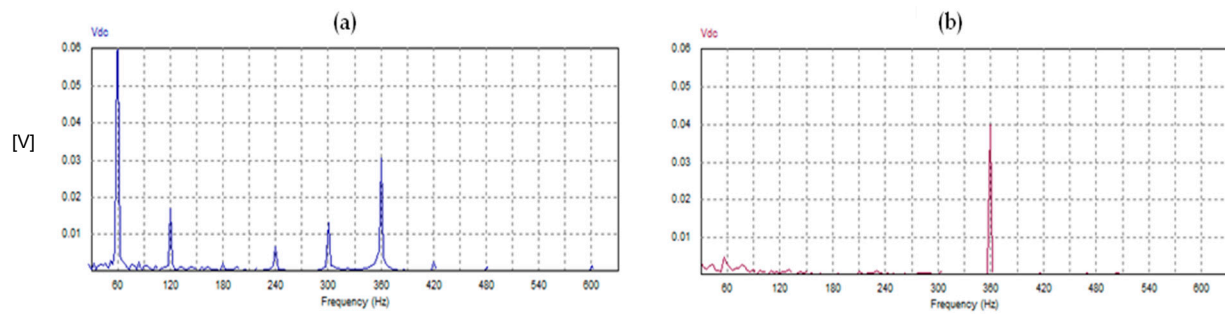


Figure 18. Harmonic spectrum of the DC bus voltage V_{DC} with both SAPF schemes: (a) FSTPI and (b) SSTPI.

Moreover, quantitative analysis is conducted to assess to which degree that the SAPF using the FSTPI scheme is successful and reliable. The comparison results are summarized in Table 2.

Table 2. Performance Assessment of both SAPF schemes.

Item	Parameter	SAPF-SSTPI	SAPF-FSTPI
Supply Current i_{sa}	THD	2.05%	3.2%
	First Harmonic	11.27	11.24 A
	Third Harmonic	0.0007 A	0.077 A
	I_5/I_1	0.18%	0.66%
	PF	0.999	0.999
DC link voltage V_{DC}	Minimum value	599.96	599.85
	Maximum value	600.06	600.13
	Dominant LOH	6	1
	First Harmonic	0.0027 V	0.064 V
	Second Harmonic	0.0007 V	0.017 V
	Third Harmonic	0.0005 V	0.0024 V
	Fourth Harmonic	9.4×10^{-5} V	0.0067 V
	Fifth Harmonic	0.0002 V	0.0131 V
	Sixth Harmonic	0.039V	0.030 V

Owing to the results obtained with the quantitative analysis, the THD of the supply currents with the FSTP scheme is 3.2%, which is good. However, it is higher than that achieved by the SSTPI by 56%. Also, it is observed that the supply current with the FSTPI scheme contains a third harmonic component with a small amplitude, which is less than approximately 1% of the fundamental component (actually, it is 0.68%). The input PF is almost unity in both schemes (0.999). Although the DC bus voltages are well-regulated (controlled to the set point) in both schemes, the harmonic contents are in favor of the SSTPI scheme. E.g., when the load suddenly increases by 40% in a step change, both voltage controllers succeed in returning the DC bus voltage to the set point (600 V). The load recovery time is almost the same (in case of the SSTPI scheme it is 0.2 s, while in the FSTPI scheme it is 0.22 s), which is relatively higher than that of SSTPI scheme by 10%. The maximum voltage dip is almost the same as well. It is 1.5 V and 1.6 V in the SSTPI and FSTPI schemes, respectively.

7.2. (Highly Distorted Current): 3- Φ Diode Bridge Rectifier Loaded with a Capacitive Load

Discontinuous load currents with spikes, such as the case of the 3- Φ diode bridge rectifier loaded with a capacitive load, result in highly distorted current waveforms to be drawn from the AC mains. This type of load is challenging for any SAPF system. Therefore, such a challenging operating condition is investigated in this paper. The investigated nonlinear load is shown in Figure 19, where R is $200\ \Omega$ and C is $1\ \text{mF}$. Waveforms of the AC supply currents and harmonic spectra (before and after compensation) are presented.

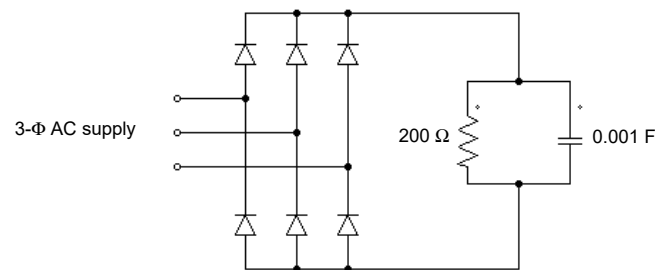


Figure 19. Highly distorted load formed by 3- Φ diode bridge feeding a capacitive load.

Figure 20 illustrates the highly distorted currents drawn from the AC mains due to the 3- Φ diode bridge rectifier loaded with a capacitive load. The corresponding harmonic spectrum of the phase current is plotted in Figure 21. The dominant low-order harmonics are odd 5th, 7th, 11th, and 13th components with considerable amplitudes (no triplen). Moreover, the computed THD of the supply current is 125%. Meanwhile, the input PF is 0.624. This type of loading condition is challenging for SAPFs.

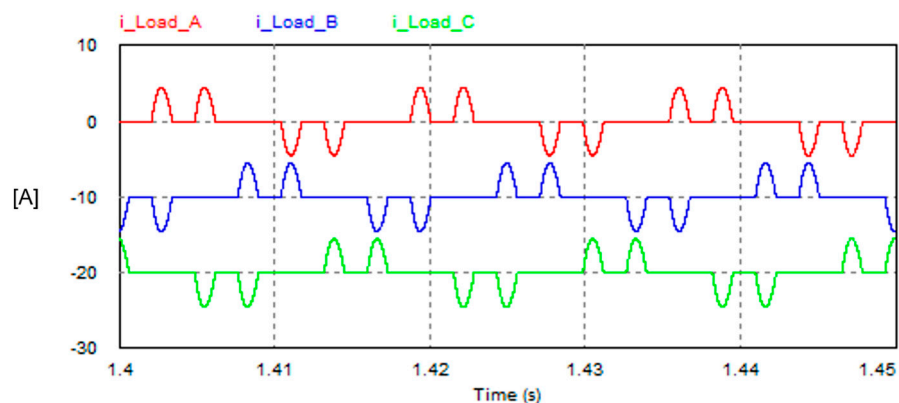


Figure 20. Highly distorted load currents due to 3- Φ diode bridge rectifier loaded with a capacitive load.

The SAPF using the FSTPI scheme succeeds in improving the waveforms of the currents drawn from the AC mains, as illustrated in Figures 22 and 23. The resultant three-phase currents drawn from the AC supply are extremely improved. The computed THD is 9%. Meanwhile, the input PF improves to 0.99. This also can be indicated from the corresponding harmonic spectrum of the supply current i_{sa} depicted in Figure 23. The harmonic spectra of the supply current i_{sa} before and after applying the SAPF are shown in Figures 21 and 23, respectively.

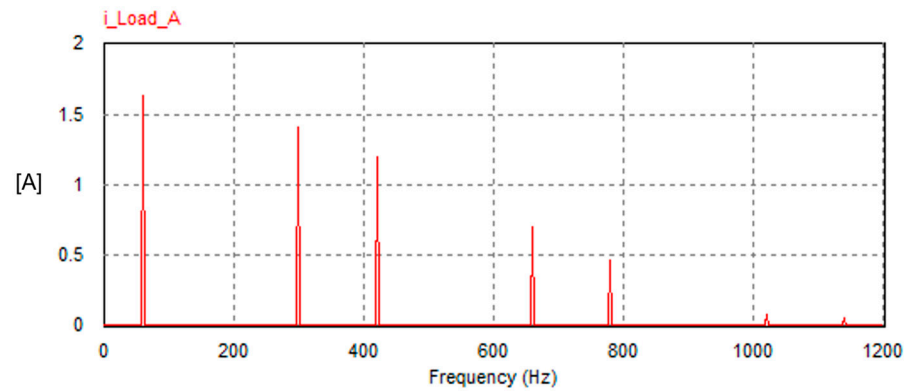


Figure 21. Harmonic spectrum of the highly distorted load current depicted in Figure 20.

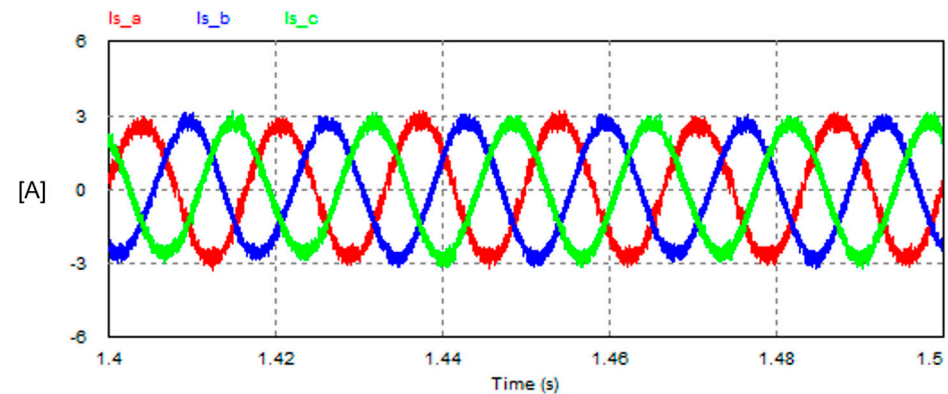


Figure 22. 3-Φ supply currents (i_{sa} , i_{sb} , and i_{sc}) with SAPF using FSTPI scheme under highly distorted load current.

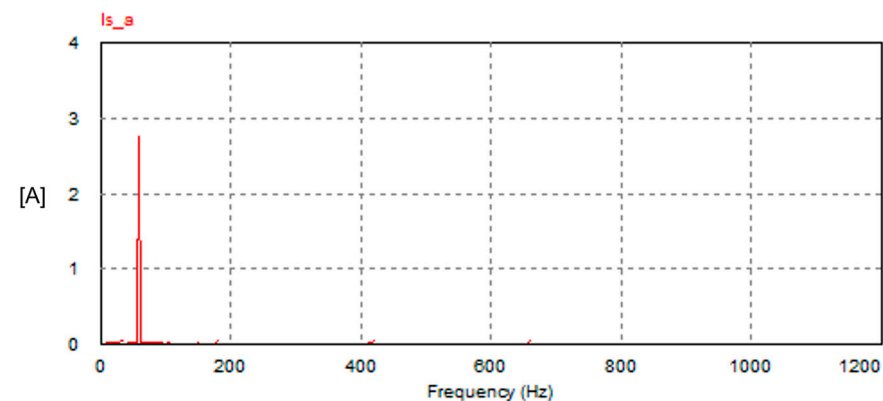


Figure 23. Harmonic spectrum of AC supply current i_{sa} with SAPF using FSTPI scheme under highly distorted load current.

The obtained results illustrated in Figures 22 and 23 indicate that the SAPF using the FSTPI scheme is efficient in compensating for the highly distorted current waveform, resulting in accepted THD levels and improved harmonic contents. The undesired dominant low order-harmonics are extremely attenuated.

7.3. (Unbalanced Non-Linear Load): Three 1-Φ Diode Bridge Rectifiers Loaded with Unequal Capacitive Loads

The operation of the SAPF with the FSTPI scheme is tested under an unbalanced load condition. The load is also a nonlinear type. Three single-phase diode rectifiers feeding an unequal capacitive load are used to produce such unbalanced loading conditions, as

illustrated in Figure 24. Practically, this case occurs in the real operation of many electronic appliances that employ old-fashioned power electronic converters (diode bridge rectifiers with smoothing capacitors). Figure 25 illustrates the currents drawn from the AC mains under unbalanced loading condition. The corresponding harmonic spectrum of the phase current i_{sa} is plotted in Figure 26. The dominant low-order harmonics are odd 3rd, 5th, 7th, 9th, 11th, and 13th components with considerable amplitudes. The computed THD of the supply current i_{as} is 153%. Meanwhile, the input PF is 0.544. Such an unbalanced nonlinear load is also challenging to the operation of SAPFs.

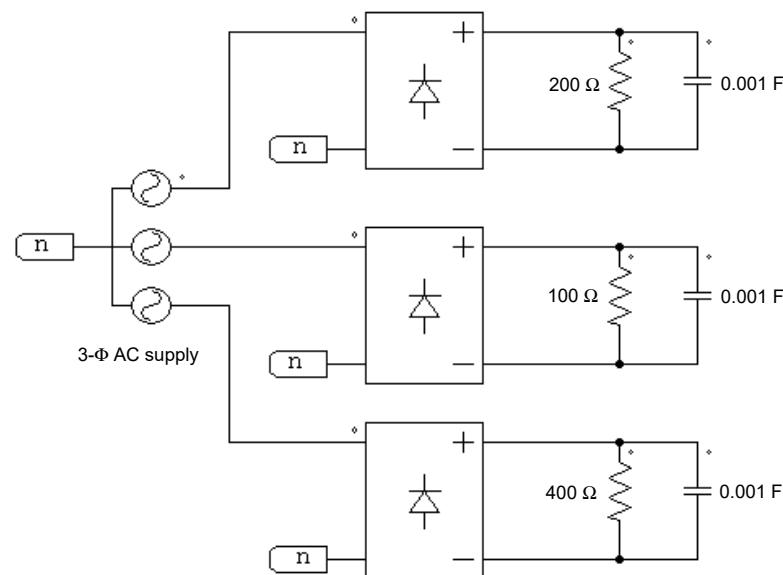


Figure 24. Unbalanced nonlinear capacitive load formed by three 1- Φ diode bridges feeding unequal capacitive loads.

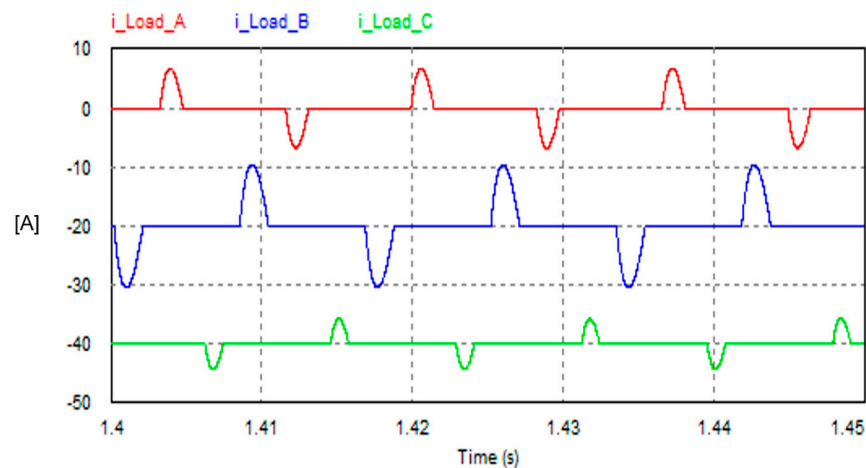


Figure 25. Unbalanced supply currents due to unbalanced nonlinear capacitive load.

The results obtained with the SAPF using the FSTPI scheme demonstrate the validity and effectiveness of the SAPF with the FSTPI scheme in alleviating unbalanced nonlinear loading conditions (see Figures 27 and 28). The resultant three-phase currents drawn from the AC supply are significantly improved. Moreover, the FSTPI-based SAPF not only improves the waveforms of the supply currents, but also improves the input PF. The resultant THD of the supply current is extremely improved to a good value (6.2%). Meanwhile, the input PF is raised to 0.99. In addition, the undesired dominant low-order harmonics of the supply current i_{sa} are extremely attenuated, as indicated in Figure 28. The

harmonic spectra of the supply current i_{sa} before and after applying the SAPF are shown in Figures 26 and 28, respectively.

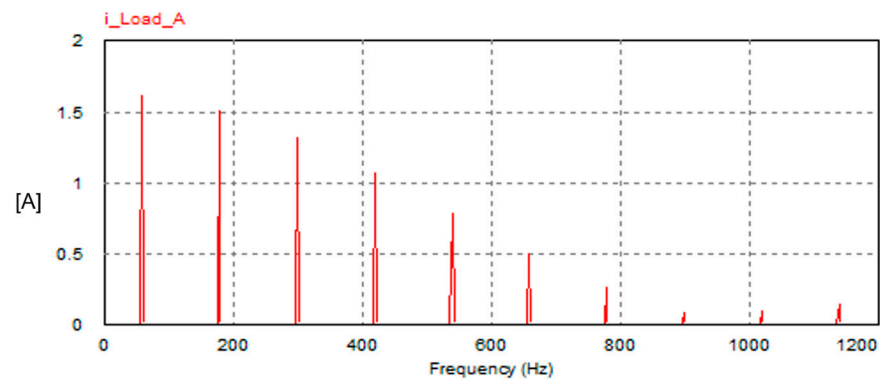


Figure 26. Harmonic spectrum of the supply current i_{sa} depicted in Figure 25.

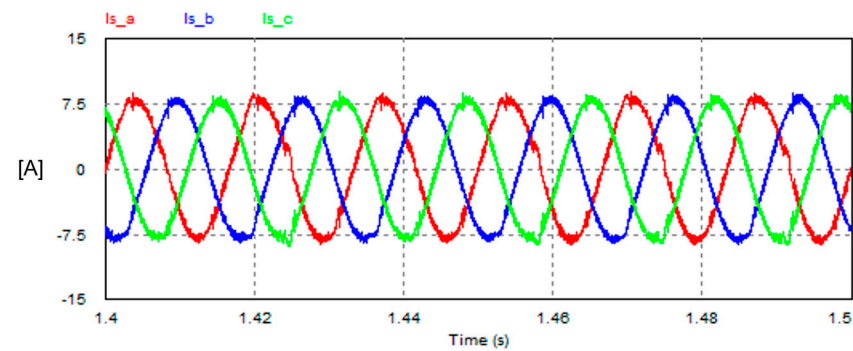


Figure 27. 3- Φ supply currents (i_{sa} , i_{sb} , and i_{sc}) with SAPF using FSTPI scheme under unbalanced nonlinear loading condition.

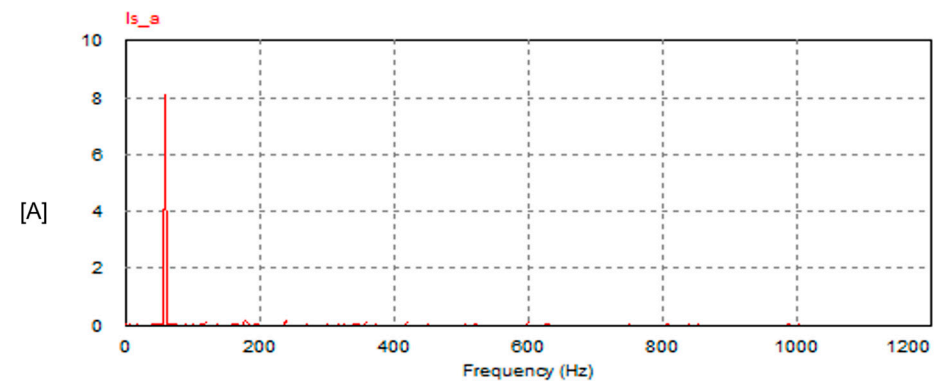


Figure 28. Harmonic spectrum of AC supply current i_{sa} with SAPF using FSTPI scheme under unbalanced nonlinear loading condition.

8. Conclusions

The paper presents a shunt active power filter (SAPF) using a four-switch three phase inverter (FSTPI) as an economic SAPF scheme. The FSTPI-based SAPF is studied under different nonlinear loading conditions, including a highly inductive load, highly distorted load, and unbalanced load. Also, the performance of the SAPF with the FSTPI topology is compared with the conventional SSTPI counterpart. Qualitative and quantitative analyses are carried out as well. The obtained results indicate the validity and effectiveness of the FSTPI scheme to be utilized in implementing SAPFs. The main findings are summarized in the following points:

1. The total harmonic distortion (THD) of the grid current with the FSTPI scheme is 3.2%, while with the SSTPI scheme, it is 2.05%. Thus, the THD with the FSTPI is higher by 56%.
2. The amplitude of the fifth-order harmonic in the supply current does not exceed 1% of the fundamental component in both schemes. In the FSTPI, the ratio (I_5/I_1) is 0.66%, while the corresponding ratio in the SSTPI is 0.18%.
3. The input power factor (PF) in both schemes is almost unity (0.99).
4. Both schemes of SAPFs produce the same average value of the DC link voltage, which is well-regulated to the desired set point (600 V) thanks to the PI voltage controllers of the outer voltage control loops. However, in the case of the FSTPI scheme, the dominant low-order harmonic of the DC link voltage pulsates at the supply frequency (60 Hz). Meanwhile in the case of the SSTPI, the dominant low-order harmonic of the DC link voltage pulsates at a rate six times the supply frequency (360 Hz).
5. The operation of the FSTPI-based SAPF is reliable and effective under highly distorted loading conditions. After compensation, the THD of the grid currents is extremely improved from 125% to 9%, meanwhile the PF is improved from 0.624 to 0.99.
6. The SAPF using the FSTPI is effective in compensating for the unbalanced nonlinear loading condition whose current waveform is highly distorted. The THD improves from 153% to 6.2%, meanwhile the PF improves from 0.544 to 0.99.
7. Compared with the SSTPI scheme, the proposed SAPF with the FSTPI scheme provides a reduction in the number of power transistors, freewheeling diodes, and auxiliary driver/isolation circuits by 33.33%. Moreover, the number of Hall effect current and voltage transducers that are needed to implement the SAPF with the FSTPI is reduced by the same amount (33%), which reduces the overall capital cost of the SAPF system.
8. The FSTPI scheme requires an additional two capacitors instead of two power semiconductor switches. Fortunately, the price of power capacitors is less than the price of power transistors, especially if their type is SiC.
9. The FSTPI scheme provides a reduction in conduction power losses of 33% for the same inverter current compared with its SSTPI counterpart.
10. Compared with the SSTPI scheme, the FSTPI suffers from an increase in switching power losses by 15.4% when both inverters operate at the same PWM switching frequency and the same inverter output voltage.
11. Although the conventional SAPF scheme with the SSTPI provides a relatively superior performance in terms of AC currents drawn from the grid with a lower THD and a lower harmonic content of the DC link voltage, the SAPF based on the FSTPI is considered to be competitive with the conventional SAPF scheme in terms of the reduced number of power semiconductor devices and transducers needed to implement the overall system.
12. The satisfactory performance achieved by the SAPFs with the FSTPI scheme makes the FSTPI scheme feasible and applicable when price reduction and fabricating economic SAPFs are of major concern.

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Conflicts of Interest: The author declares no conflicts of interest.

Nomenclature

Abbreviations

APF	Active power filter
FSTPI, B4	Four-switch three-phase inverter
FFT	Fast Fourier transform
FO-PID	Fractional-order PID
IGBT	Insulated gate bipolar transistor
LOH	Low-order harmonic
MOSFET	Metal–oxide field-effect transistor
THD	Total harmonic distortion
PCC	Point of common coupling
PF	Power factor
PLL	Phase-locked loop
PID	Proportional–integral–derivative
PWM	Pulse width modulation
SAPF	Shunt active power filter
SCR	Silicon controlled rectifier
SPWM	Sinusoidal PWM
SiC	Silicon Carbide
SSTPI, B6	Six-switch three-phase inverter
SVM	Space vector modulation
VSI	Voltage source inverter
WBG	Wide band gap

Symbols

$i_{fa}^*, i_{fb}^*, i_{fc}^*$	Reference filter currents
$i_{sa}^*, i_{sb}^*, i_{sc}^*$	Reference supply (grid) currents
i_{La}, i_{Lb}, i_{Lc}	Instantaneous values of the load currents
$i_{La1}, i_{Lb1}, i_{Lc1}$	Instantaneous values of the 1st harmonic of the nonlinear load currents
I_{MAX}^*	Peak value of the reference supply current
V_{DC}^*	Reference DC link voltage
V_{DC}	Instantaneous value of DC link voltage
$S_1, S_3, S_5, S_4, S_6, S_2$	Switching signals of the six transistors of SSTPI
S_3, S_5, S_6, S_2	Switching signals of the four transistors of FSTPI
C_1, C_2	Capacitors of the 1st branch of FSTPI
C	DC link capacitor of SAPFs
L_f	Inductance of the inductor connected to the output of the SAPF
L_s	Inductance of the AC supply (grid inductance)
v_s	AC supply voltage
K_{swt}	Switching function of the inverter
$G_{pi1}(S), G_{pi2}(S)$	Transfer functions of PI controllers of the voltage and current loops, respectively
$G_v(S)$	Open-loop gain function of the voltage control loop
$G_i(S)$	Open-loop gain function of the current control loop
$T_v(S)$	Closed-loop transfer function of the voltage control loop
$T_i(S)$	Closed-loop transfer function of the current control loop
K_{p1}, K_{p2}	Proportional gains of the voltage and current controllers, respectively
K_{i1}, K_{i2}	Integral gains the voltage and current controllers, respectively
ζ_1, ζ_2	Damping ratios of voltage and current control loops, respectively
t_{s1}, t_{s2}	Settling times of voltage and current control loops, respectively
ω_{n1}, ω_{n2}	Natural frequencies of voltage and current control loops, respectively
ω	Supply radian frequency

Appendix A

Appendix A.1. Derivation of PI Controller's Gains of DC Voltage Control Loop

The transfer function of the PI voltage controller is given by Equation (A1), as follows:

$$G_{pi1}(S) = K_{p1} + \frac{K_{i1}}{S} = \frac{SK_{p1} + K_{i1}}{S} \quad (A1)$$

The open-loop gain function is given by Equation (A2), as follows:

$$G_v(S) = \frac{G_{pi1}(S)}{SC} = \frac{SK_{p1} + K_{i1}}{S^2C} \quad (A2)$$

Thus, the closed-loop transfer function of the voltage control loop is given by Equation (A3), as follows:

$$T_v(S) = \frac{G_v(S)}{1 + G_v(S)H(S)} \quad (A3)$$

where $H(S)$ is 1 for unity feedback. Accordingly, the closed-loop transfer function will have the following formula:

$$T_v(S) = \frac{\left(\frac{SK_{p1} + K_{i1}}{CS^2}\right)}{1 + \left(\frac{SK_{p1} + K_{i1}}{CS^2}\right)} = \frac{SK_{p1} + K_{i1}}{CS^2 + SK_{p1} + K_{i1}} \quad (A4)$$

The gains K_{p1} and K_{i1} can be computed by comparing the characteristic equation of $T_v(S)$ with the standard form given by Equation (A5) and solving for proper values of ζ_1 and ω_{n1} .

The standard form of characteristic equation is given by the following:

$$(S^2 + 2\zeta_1\omega_{n1}S + \omega_{n1}^2 = 0) \quad (A5)$$

Accordingly, the following relations are yielded:

$$2\zeta_1\omega_{n1} = \frac{K_{p1}}{C} \quad (A6)$$

$$\omega_{n1}^2 = \frac{K_{i1}}{C} \quad (A7)$$

Thus,

$$K_{p1} = 2\zeta_1\omega_{n1}C \quad (A8)$$

$$K_{i1} = C\omega_{n1}^2 \quad (A9)$$

Appendix A.2. Derivation of PI Controller's Gains of Inner Current Control Loop

$$G_{pi2}(S) = K_{p2} + \frac{K_{i2}}{S} = \frac{SK_{p2} + K_{i2}}{S} \quad (A10)$$

The open-loop gain function is given by Equation (A11), as follows:

$$G_i(S) = \frac{G_{pi2}(S)}{SL} = \frac{SK_{p2} + K_{i2}}{S^2L} \quad (A11)$$

Therefore, the closed-loop transfer function of the current control loop is given by Equation (A12), as follows:

$$T_i(S) = \frac{G_i(S)}{1 + G_i(S)H(S)} \quad (A12)$$

where $H(S)$ is 1 for unity feedback. Accordingly, the closed-loop transfer function will have the following formula:

$$T_i(S) = \frac{\left(\frac{SK_{p1}+K_{i1}}{LS^2}\right)}{1 + \left(\frac{SK_{p1}+K_{i1}}{LS^2}\right)} = \frac{SK_{p1} + K_{i1}}{LS^2 + SK_{p1} + K_{i1}} \quad (A13)$$

The gains K_{p2} and K_{i2} can be determined by comparing the characteristic equation of $T_i(S)$ with the standard form given by Equation (A14) and solving for proper values of ζ_2 and ω_{n2} .

The standard form of characteristic equation is given by the following:

$$(S^2 + 2\zeta_2\omega_{n2}S + \omega_{n2}^2 = 0) \quad (A14)$$

Accordingly, the following relations are yielded:

$$2\zeta_2\omega_{n2} = \frac{K_{p2}}{L} \quad (A15)$$

$$\omega_{n2}^2 = \frac{K_{i2}}{L} \quad (A16)$$

Thus,

$$K_{p2} = 2\zeta_2\omega_{n2}L \quad (A17)$$

$$K_{i2} = L\omega_{n2}^2 \quad (A18)$$

Appendix B

Comparative Analysis of SAPFs Using FSTPI and SSTPI Schemes

Table A1. Comparison between Both SAPF schemes.

Item		SSTPI	FSTPI
Number of devices	Transistors and freewheeling diodes	6	4
	Isolation and driving circuits	6	4
	Hall effect current transducers	3	2
	Hall effect voltage transducers (for DC link voltage measurement)	1	1
	Phase-locked loop (PLL) or Hall effect voltage transducers (for unity gain signal synchronized with the AC grid voltage)	3	2
Inverter output voltage	Capacitors (DC link and one branch of the inverter power circuit)	1	3
	Normalized line–line or line–neutral (at the same DC link voltage)	1	$\frac{1}{\sqrt{3}} = 0.577$
	Normalized required DC link voltage (for the same inverter output voltage)	1	$\sqrt{3} = 1.732$

Table A1. *Cont.*

Item		SSTPI	FSTPI
Power losses	Normalized conduction losses (for the same inverter load current)	1	0.666
	Normalized switching losses (for the same inverter output voltage and current and at the same PWM switching frequency)	1	$\frac{4}{6}\sqrt{3} = 1.154$
	Normalized total power losses	1	$\frac{(0.666+1.154)}{2} = 0.91$
Power quality	Input PF	0.99	0.99
	Best achieved THD of AC grid current (at the same switching frequency, sampling time, passive filtering components)	2%	3%

Table A2. Percentage of saving/additional costs of FSTPI compared with SSTPI scheme.

Item	Description	Percentage
Saving in the devices	Transistors and freewheeling diodes	33.3%
	Isolation and driving circuits	33.3%
	Hall effect current transducers	33%
	Phase-locked loop (PLL) or Hall effect voltage transducers (for unity gain signal synchronized with the AC grid voltage)	33.3%
Additional cost of capacitors	Two capacitors of one arm (branch of no power transistors)	200%
Undesired reduction in the inverter output voltage	For the same DC link voltage	42.3%
Required additional increase in DC link voltage	For the same inverter output voltage	73.2%
Reduction (saving) in conduction power losses	For the same load current	33.3%
Increasing in switching power losses	At the same PWM switching frequency and for the same inverter output voltage and current	15.4%
Saving in overall power losses	For the same operating conditions	9%

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