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# Design and Experimental Verification of Electric Vehicle Battery Charger Using Kelvin-Connected Discrete MOSFETs and IGBTs for Energy Efficiency Improvement

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**Abstract:** This research investigates the advantages of Kelvin-connected 4-pin discrete transistors, both MOSFETs and IGBTs, in onboard battery chargers for electric vehicles. The study compares the standard 3-pin and the extended 4-pin packages based on averaged data collected from leading manufacturers. The investigation shows significant potential power loss reduction, thermal operation mitigation, and reduced gate-drive oscillation for the 4-pin package. The benefits have been quantified by analysing the operation of actual switches in an automotive battery charger based on Boost-PFC and DC-DC LLC converters. The converters' practical design demonstrates a procedure for integrating the Kelvin-connected package into the design methodology. The results have been verified experimentally.

**Keywords:** battery charger; LLC; boost PFC; Kelvin connection; IGBT; MOSFET; TO-247 package

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## 1. Introduction

Battery chargers for automotive applications are one of the main onboard sub-systems of electric vehicles. Like all other pieces of electronics, high efficiency, power density, reliability, and ease of thermal management are vital. To fulfil these needs, this study investigates 4-pin Kelvin-connected discrete MOSFETs and IGBTs, which offer advanced characteristics potentially leading to power loss and temperature reductions.

The advantages of Kelvin-connected MOSFETs have been well evaluated with analytical models based on equivalent circuits, supported by experimental verification [1–5]. In [1], the research focuses on the influence of gate-drive resistance on the drain current spike and oscillations during turn-on and turn-off. The importance of minimising parasitic inductance in the gate-drive circuit, which takes advantage of the Kelvin-connected 4-pin package's full potential, is analysed in [2]. This paper also analyses the effects of external factors, such as PCB layouts and gate-drive elements. The model in [3] includes device and circuit layout parasitics, exploring the effective transconductance during transients. The targeted maximum parasitic common source inductance criterion is 3 nH, as given in [4]. Assuming the above requirements for the package have been implemented, the Kelvin connection can also improve the reverse-recovery phenomenon associated with the body diode, as shown in [5].

Many studies have demonstrated the advantages of the Kelvin-connected 4-pin package by directly comparing it to the standard 3-pin through-hole package [6–9]. A reliability comparison between the two packages was conducted in [6] with High Electric Field (HEF) and Active Channel Gate Bias (ACGB) tests. The experimental results show that, generally, 3-pin packages are more tolerant to short circuits due to their higher source inductance and resistance. The research demonstrates a disadvantage of Kelvin-connected packages, which must be mitigated by providing over-current protection to ensure the same level of reliability. In a similar case, in [7,8], both packages' dynamic parameters were compared, and the blanking time of the desaturation protection scheme for the power

modules was studied. The parasitic inductances for the standard 3-pin package are in the range of 5–10 nH, while those for the Kelvin package are estimated to be 0.2–1 nH [8]. The comparison in [9] shows the Kelvin-connected 4-pin advantage over the exact 3-pin counterpart applied in a Boost-PFC converter. The same research also specified the optimal gate-drive resistors for the Kelvin-connected package as 18 Ω, being a trade-off between the oscillations at the gate-drive circuit, EMI, and the transistors' dynamic performance in that particular case.

The ability to use transistors in parallel is used to increase the current-handling capability. Research in this direction shows that by meeting specific requirements, Kelvin-connected devices could offer some advantages when connected in parallel [10–14]. A passive balancing method applied to Kelvin-connected SiC MOSFETs using a differential mode choke without additional active control was proposed in [10]. The undesirable effect of crosstalk was investigated further in [11], applying techniques for Gate Impedance Regulation (GIR) and Gate Voltage Regulation (GVR). The impact of an asymmetric layout on current balancing was analysed in [12]. It has been shown that current balancing strongly depends on the quality of the gate-drive circuit, particularly the prevention of gate-drive oscillations [13]. For this reason, in [14], additional resistors in the Kelvin circuit were utilised between the emitter and the gate driver, which was demonstrated with 4-pin IGBTs. The study recommends resistors in the range of 0.5–1 Ω connected in series to the driver.

Additional benefits of the Kelvin connection in both MOSFETs and IGBTs have been objects of research in several studies [15–21]. In [15], online bond wire fault monitoring was proposed, and with a similar topology [16], it offers short-circuit, overload, and gate-drive protection for high-voltage MOSFET modules. Because such overloads apply significant stress, a comprehensive study on consequent thermal–electrical degradation was undertaken in [17]. Finally, the main benefit of the Kelvin connection—improved dynamic characteristics leading to loss reduction—was shown in [18,19]. These advantages make the Kelvin-connected transistors the right choice for critical automotive applications, as proven in [20,21].

Similar studies have been dedicated to discrete Kelvin-connected IGBTs and SiC MOSFETs. According to the comparison conducted in [22–24] and the 4-pin package analysis [25], the switching loss for Kelvin-connected SiC MOSFET is 60% [23] to 80% [22] reduced compared to Si IGBTs, reducing the junction temperature by 38% [23]. Also, a comparison between the 3-pin and 4-pin IGBTs demonstrated an improved power density with the TO-247PLUS package due to the reduced number of paralleled transistors [24]. The expected switching power loss reduction by using IGBTs in a 4-pin package is up to 10% compared to the identical transistors in a 3-pin TO-247 package [25]. Further power density and efficiency improvements were reported due to IGBTs with TRENCHSTOP technology [26], giving up to 15% more output current, and these IGBTs are also offered in the TO-247PLUS package. The measurement techniques and protection abilities of Kelvin-connected IGBTs were reported in [27–30] for discrete packages and modules.

Power density and efficiency are the central requirements for automotive applications, including onboard battery chargers. One of the topologies offering high efficiency is the LLC DC-DC converter, widely used in battery chargers [31–41]. The reported efficiency in [31] is 94.6% at 2.7 kW, operating with a combination of Pulse Frequency Modulation (PFM) and Pulse Width Modulation (PWM) for light-load operation. The topology is applicable for low-voltage (LV) [31,34–36,39,41] and high-voltage (HV) [32,37,38] battery chargers. A similar efficiency of 94.3% was reported in [32] for a train application charger rated at 25 kW. The switching frequency using SiC MOSFETs can reach 1 MHz, achieving 95.8% efficiency over the battery voltage range, as experimentally shown for an 11 kW charger in [33]. In [35], a frequency range between 91 kHz and 110 kHz was applied, giving 96.9% efficiency with a five-level LLC converter. Similar multi-level techniques have been demonstrated with a series–parallel connection of two transformers [37], reducing the size and the core power loss and improving heat dissipation. The same benefits are achievable with an interleaved LLC topology, as shown in [38], giving 95.65% peak efficiency for a

converter with 1.5 kW maximum power. A three-phase topology was described in [39]. Optimal transformer design techniques were presented in [40], and the low-voltage output (28 V) with a relatively high output current (50 A) solution was suggested in [41].

The Power Factor Correction (PFC) converter is mandatory for offline chargers [42–57]. The DC-DC topologies used are Boost, semi-bridgeless, and bridgeless. The review in [42] presents their advantages and disadvantages. Many studies report the superior efficiency of bridgeless converters [43–47] based on the Totem-pole topology with GaN HEMTs. However, the circuit is distinguished by increased complexity and price due to the expensive GAN transistors. Therefore, the DC-DC Boost-PFC converter is still preferred for many applications, offering a good quality/price ratio [48–57].

Although PFC-Boost is a well-known topology, its development and improvement are still in progress. A modification of the PFC-Boost feedback circuit to reduce the compensation capacitor, potentially leading to improved reliability and reduced cost, was suggested in [48]. Further, an overall power factor increase can be achieved by applying variable inductances, for example, ranging from 0.193 mH to 0.951 mH [49]. The potential of the Boost-PFC converter to operate with low Electromagnetic Interference (EMI) was shown in [50], and the reduction in the Total Harmonic Distortion (THD) in the supply current to within industrial standards was shown in [51].

The interleaved Buck–Boost and PFC-Boost topologies [52–59] offer additional benefits, like reduced current and, thermal stress on the power switches, more uniform power loss distribution, and improved reliability. To deploy the full potential of the interleaved circuit, some essential issues must be resolved: equalising current sharing [52]; applying soft commutation [53]; increasing the output voltage range with Buck–Boost operation [54,55]; and improving the light-load operation with a coupled inductor [56]. Nevertheless, an interleaved Boost-PFC converter remains a good choice for an onboard battery charger, as demonstrated in [57]. The general utilisation of Buck–Boost converters is a part of the charging system of the electric drivetrain, as shown in [58,59]

The literature review leads to the following conclusions:

- The advantages of the 4-pin discrete Kelvin-connected MOSFETs [1–20] and IGBT [21–30] are well demonstrated with models and simulations and supported with experiments. The switches were studied individually and are not associated with a specific converter topology. Therefore, their potential contribution to power loss and temperature reduction in a particular topology requires additional study.
- Most battery charger converters are based on a PFC-Boost circuit [42–57], offering a good quality/price ratio and a subsequent LLC [31–41] stage, which is highly efficient due to the ZVS operation. Published results suggest that further improvement could be achieved with Kelvin-connected transistors, but this requires further analytical and experimental investigation. However, no complete study has demonstrated the application of Kelvin-connected discrete IGBTs and MOSFETs in automotive battery chargers.

Based on these conclusions, this research aims to fill the knowledge gap by showing approaches for integrating Kelvin-connected transistors into the Boost-PFC and LLC DC-DC stages in an automotive battery charger, supported by a comparison between the standard 3-pin and Kelvin-connected 4-pin packages. The results quantify the potential benefits by numerically estimating the power loss reduction, temperature decrease, and efficiency improvement. In this sense, the novelty is finding alternative approaches to improving converters based on 4-pin Kelvin-connected TO 247 package transistors, enhancing the battery charger.

The rest of this paper is structured as follows: Section 2 introduces the proposed battery charger architecture and develops the primary mathematical approach to describe the main difference between the two packages; in Sections 3 and 4, the design of the LLC and PFC-Boost converters are presented, respectively; Section 5 introduces the experimental verification, and the final conclusions are given in Section 6.

## 2. The Architecture of the Proposed Battery Charger

This part presents the topology of the proposed charger based on discrete Kelvin-connected IGBTs and MOSFETs. Based on 4-lead TO-247PLUS transistors, the potential for power loss reduction, leading to efficiency improvement, is studied analytically, supported by datasheet examples for several off-the-shelf devices.

### *2.1. The Central Topology of the Proposed Charger*

Figure 1 shows the primary circuit of the explored battery charger. This research focuses on two sub-systems: the Boost-PFC DC-DC converter and the LLC DC-DC converter, which operates as a battery charger. As the suggested Kelvin connection benefits apply to the converters' power parts, control systems and feedback networks are not considered.

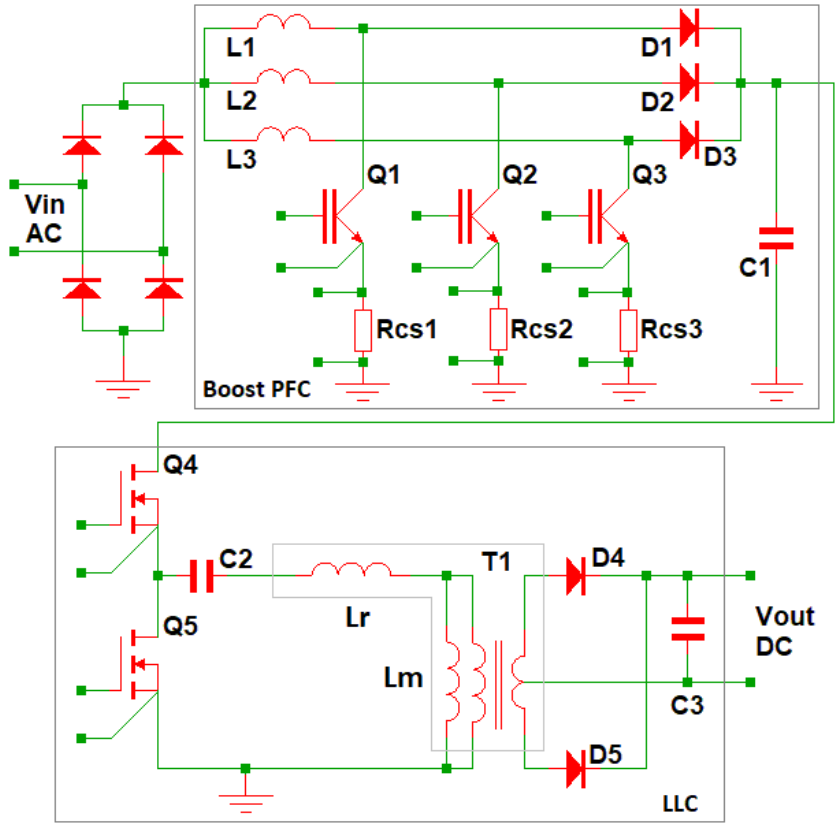



**Figure 1.** The central topology of the suggested battery charger with Kelvin-connected transistors.

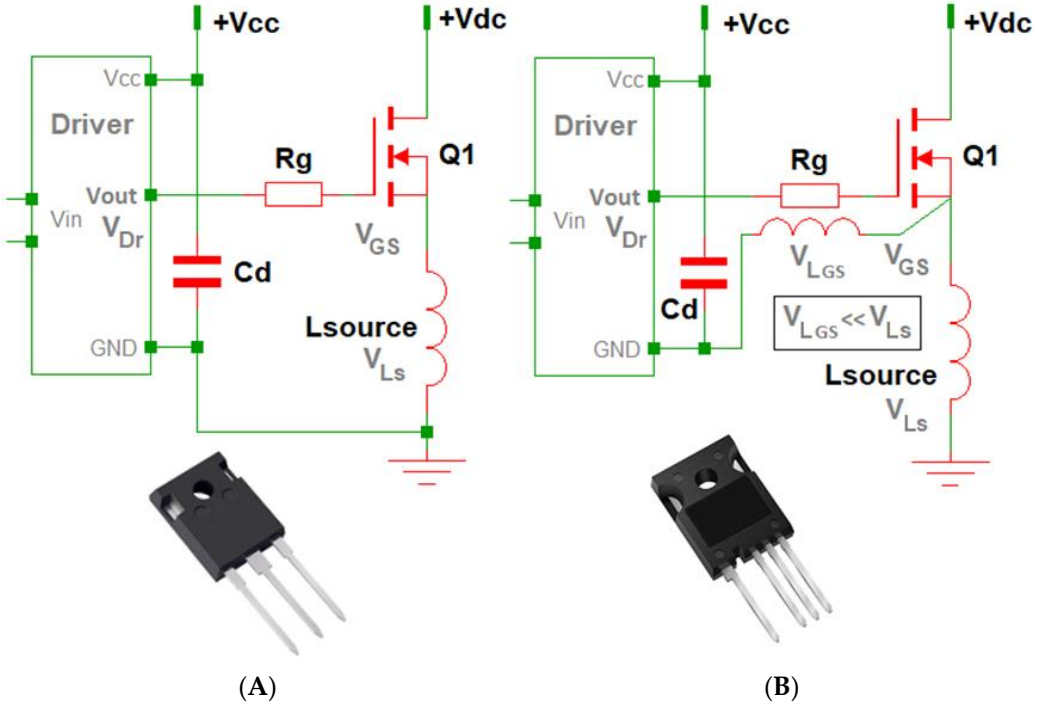
The proposed charger comprises the following elements:

- Single-phase input rectifier (not part of this research).
- Boost-PFC converter with three channels. Channel 1: Kelvin-connected IGBT Q1, inductor L1, ultra-fast diode D1, and current sense resistor Rcs1. Channel 2: Q2, L2, D2, Rcs2. Channel 3: Q3, L3, D3, and Rcs3. The Boost capacitor C1 is common for all three parallel channels.
- LLC DC-DC half-bridge converter with Kelvin-connected MOSFETs Q4 and Q5, resonant circuit capacitor C2, transformer with integrated resonant inductor T1, output rectifier ultra-fast diodes D4 and D5, and output filter capacitor C3. The transformer integrates the resonant inductance $L_r$ and magnetised inductance $L_m$.

### *2.2. Investigation of the Application of Kelvin-Connected Discrete MOSFETs and IGBTs in the Suggested Battery Charger*

The primary circuits of the standard 3-pin and Kelvin 4-pin TO-247 packages are shown in Figure 2A and Figure 2B, respectively. The main elements are the driver, the

gate-drive resistor (Rg), the gate-drive capacitor (Cd), and the parasitic source inductance (Lsource). The same circuit topology and analysis applies to the IGBTs; therefore, they are not presented separately.




(**A**) (**B**)

**Figure 2.** Primary circuits of TO-247 package with 3-pins (**A**) and Kelvin source 4-pins (**B**).

As previously explained, the first package includes the parasitic source inductance, $L_{source}$, as a part of the gate-drive loop, the driver $V_{out}$, $R_g$, $Q1$ gate-source junction, $L_{source}$, and ground GND. The Kelvin source package isolates $L_{source}$ from the gate-drive loop by doubling the source pins. The configuration has the potential to reduce the switching losses by lowering the ON and OFF times and, respectively, the accumulated energies $E_{ON}$ and $E_{OFF}$. This package advantage is first studied analytically based on the main circuit equations and supported numerically with statistical data and specific examples [60–62].

In a steady state, the $Q1$ gate-source voltage ($V_{GS}$) can be related to the voltage difference between the gate driver output voltage ($V_{Dr}$) and the voltage drop ($V_{Ls}$) over the $L_{source}$ as follows:

$$V_{GS} = V_{Dr} - V_{Ls}, \tag{1}$$

expressing $V_{Ls}$ with

$$V_{Ls} = L_{source}\frac{di}{dt}, \tag{2}$$

which gives the following equation:

$$V_{GS} = V_{Dr} - L_{source}\frac{di}{dt} \tag{3}$$

From the last equation, the $L_{source}$ influence on the ON ($V_{GS.ON}$) and OFF ($V_{GS.OFF}$) gate-source voltages can be expressed as

$$V_{GS.ON} = V_{Dr.ON} - R_G \times I_{G.ON} - L_{source}\frac{di}{dt} \tag{4}$$

$$V_{GS.OFF} = V_{Dr.OFF} - R_G \times I_{G.OFF} + L_{source}\frac{di}{dt} \tag{5}$$

where $I_{G.ON}$ and $I_{G.OFF}$ are, respectively, ON and OFF gate currents through the gate-drive resistance $R_G$, and $V_{Dr.ON}$ and $V_{GS.OFF}$ are ON and OFF gate-drive voltages.

Based on the obtained data [4,8] and the datasheets provided by the manufacturers (Appendix A Tables A1 and A2), a maximum parasitic inductance of 3 nH is accepted in this design. Following the manufacturers' recommendations, a PCB parasitic inductance of 30 nH is included in the design procedure in Section 3.

The switching-ON ($t_{on}$) and -OFF ($t_{off}$) times can be distinct for both packages, depending on $L_{source}$ and the transistor transconductance $g_{fs}$, taken to be constant. Therefore, for the 3-pin package, these times are calculated from

$$t_{on} = \left(R_g \times C_{iss} \quad + L_{source} \times g_{fs}\right) \times ln\left(\frac{V_{g.on} - V_{gs.th}}{V_{g.on} - V_{gs.Miller}}\right) + C_{rss} \times R_g \times \left(\frac{V_{ds} - V_{gs.Miller}}{V_{g.on} - V_{gs.Miller}}\right) \tag{6}$$

$$t_{off} = \left(R_g \times C_{iss} \quad + L_{source} \times g_{fs}\right) \times ln\left(\frac{V_{gs.Miller} - V_{g.off}}{V_{gs.th} - V_{g.off}}\right) + C_{rss} \times R_g \times \left(\frac{V_{ds} - V_{gs.Miller}}{V_{gs.Miller}}\right) \tag{7}$$

where $C_{iss}$ is the input capacitance; $C_{rss}$ is the reverse capacitance; $V_{g.on}$ is the gate ON voltage; $V_{gs.th}$ is gate-source threshold voltage; $V_{gs.Miller}$ is the Miller plateau voltage; $V_{ds}$ is the drain-source voltage; and $V_{g.off}$ is gate OFF voltage.

The transconductance $g_{fs}$ is calculated from the ratio $I_D$ between the drain current and the $V_{GS}$:

$$g_{fs} = \frac{I_D}{V_{GS}} \tag{8}$$

Equations (6) and (7) expressed for the Kelvin source 4-pin package are written as

$$t_{on} = \left(R_g \times C_{iss}\right) \times ln\left(\frac{V_{g.on} - V_{gs.th}}{V_{g.on} - V_{gs.Miller}}\right) + C_{rss} \times R_g \times \left(\frac{V_{ds} - V_{gs.Miller}}{V_{g.on} - V_{gs.Miller}}\right) \tag{9}$$

$$t_{off} = \left(R_g \times C_{iss}\right) \times ln\left(\frac{V_{gs.Miller} - V_{g.off}}{V_{gs.th} - V_{g.off}}\right) + C_{rss} \times R_g \times \left(\frac{V_{ds} - V_{gs.Miller}}{V_{gs.Miller}}\right) \tag{10}$$

Based on the above Equations (6)–(10), the $P_{ON}$ and $P_{OFF}$ switching power losses are calculated, respectively, from the equations

$$P_{ON} = \frac{I_{avg} \times V_{ds}}{2} \times t_{on} \times F_{sw} \tag{11}$$

$$P_{OFF} = \frac{I_{avg} \times V_{ds}}{2} \times t_{off} \times F_{sw} \tag{12}$$

where $I_{avg}$ is the average drain current; $F_{sw}$ is the switching frequency. The total switching power loss $P_{sw.loss}$ is the sum of $P_{ON}$ and $P_{OFF}$.

The turn-on energy $E_{ON}$ is determined by the gate-to-source charge $Q_{gs}$, gate-to-drain charge $Q_{gd}$, and gate charge $Q_g$, which are specified in the transistors' datasheets for a given gate-to-source voltage $V_{GS}$, drain-to-source voltage $V_{DS}$, and drain current $I_D$ as follows:

$$E_{ON} = \frac{Q_{gs} V_{gs.Miller} + \left(Q_g + Q_{gs} + Q_{gd}\right) \times \left(V_{GS} - V_{gs.Miller}\right)}{2} \tag{13}$$

$E_{OFF}$ determines the loss in the gate discharge of the gate energy $E_G = Q_G \times V_{GS}$ from $V_{GS}$ to zero according to

$$E_{OFF} = E_G - E_{ON} \tag{14}$$

In zero-voltage switching (ZVS) operation, required for the LLC converter, the gate charge $Q_{Gzvs}$ is expressed as (assumes charges are linearly related to voltage, i.e., constant capacitances)

$$Q_{Gzvs} = \frac{V_{GS}}{V_{GS} - V_{gs.Miller}}(Q_G - (Q_{GS} + Q_{GD})) \tag{15}$$

The ZVS On $E_{ONzvs}$ and ZVS Off $E_{OFFzvs}$ energies are

$$E_{ONzvs} = \frac{Q_{Gzvs} \times V_{GS}}{2} = \frac{\frac{V_{GS}^2}{V_{GS} - V_{gs.Miller}}(Q_G - (Q_{GS} + Q_{GD}))}{2} \tag{16}$$

$$E_{OFFzvs} = \frac{\left(V_{GS}^2 + V_{gs.Miller}^2\right)(Q_G - Q_{GD}) - (V_{GS} \times Q_{GS})\left(V_{GS} + V_{gs.Miller}\right)}{2\left(V_{GS} - V_{gs.Miller}\right)} \tag{17}$$

And, finally, the total ZVS energy is expressed as

$$E_{zvs} = \frac{\left(2 \times V_{GS}^2 + V_{gs.Miller}^2\right)(Q_G - Q_{GD}) - (V_{GS} \times Q_{GS})\left(2 \times V_{GS} + V_{gs.Miller}\right)}{2\left(V_{GS} - V_{gs.Miller}\right)} \tag{18}$$

The above equations are the basis for the 3-pin and 4-pin energy estimations. While leading manufacturers offer such comparisons based only on their products, this research aims at a broader range of data. Figures 3–6 show the graphical representation of statistical data collected for multiple 4-pin MOSFETs (Figures 3 and 4) and 4-pin IGBTs (Figures 5 and 6) for the Kelvin-connected transistors, respectively, given in Appendix A Tables A1 and A2. The above-presented equations are applied to the energies $E_{ON}$ and $E_{OFF}$ (Equations (13) and (14)) and the total power loss calculation (Equations (9)–(12)).

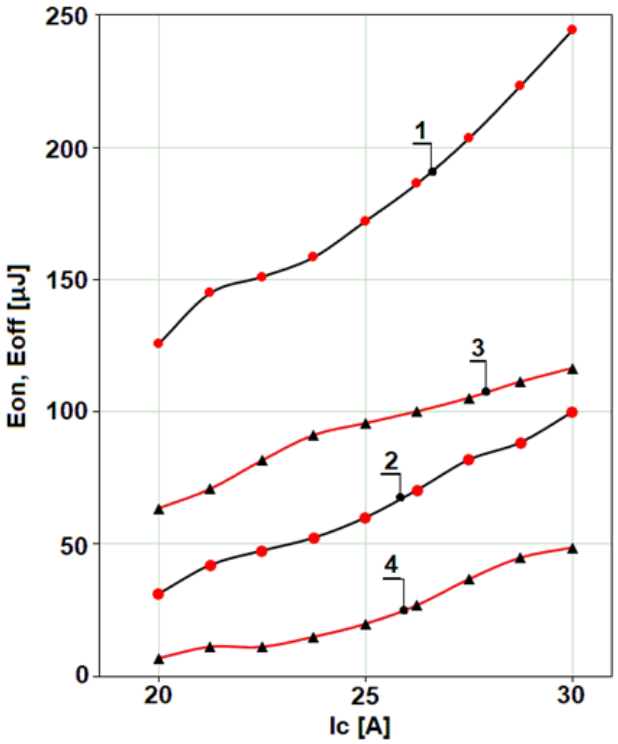



**Figure 3.** Eon (1, 3) and $E_{off}$ (2, 4) energies calculated for MOSFETs TO-247 3-pin (1, 2) and TO-247 4-pin (3, 4) packages.

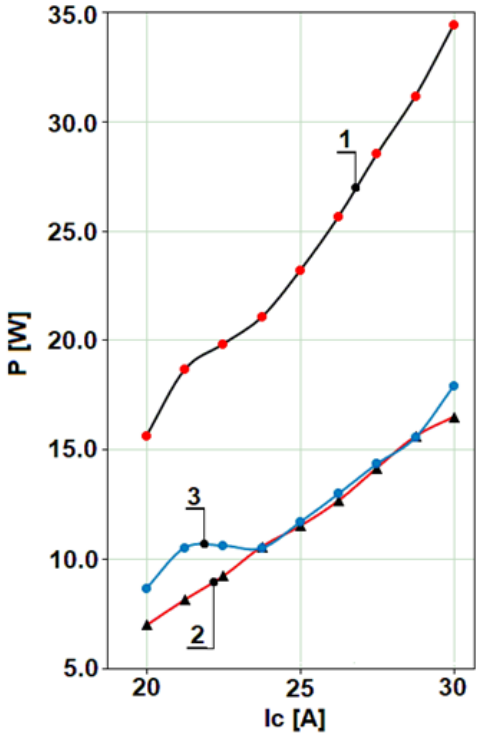



**Figure 4.** Power losses calculated for MOSFETs TO-247 3-pin (1) and TO-247 4-pin (2) packages. Difference between the two packages' power losses (3).

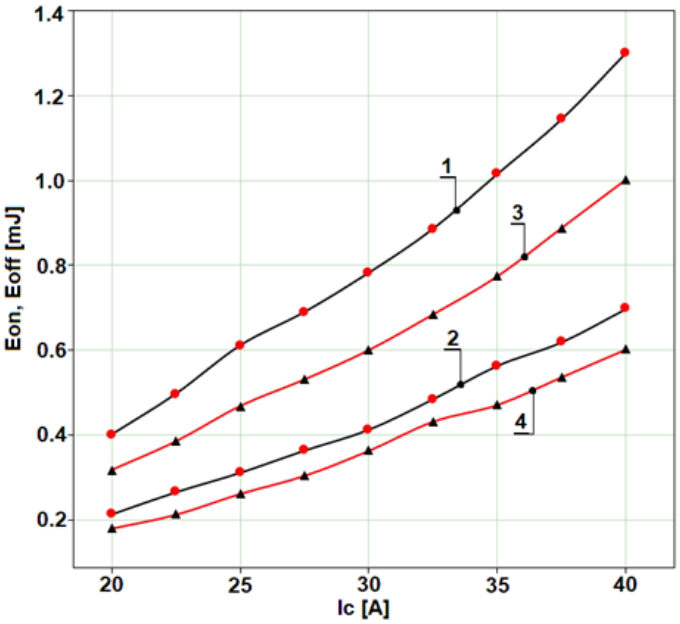



**Figure 5.** Eon (1, 3) and Eoff (2, 4) energies calculated for IGBTs TO-247 3-pin (1, 2) and TO-247 4-pin (3, 4) packages.

Generally, for Kelvin-connected MOSFETs, the average reduction in $E_{ON}$ is 47.9%, and that for $E_{OFF}$ is 65.2%, calculated for the current range of 20–30 A. For the same range, the power loss reduction varies between 8.6 W and 17.9 W (Figure 4, diagram 3), which gives a 12.5 W reduction. The results were calculated for both packages at a switching frequency of 100 kHz.

It must be clarified that the numerical comparison was conducted with hard-switching to demonstrate the benefits of 4-pin packages. In the ZVS operation, the expected loss for the LLC converter will be lower than that depicted in Table 1. In this case, the Kelvin-connected 4-pin package could benefit the LLC topology, as analysed in [1–30], through reduced gate-drive oscillations, improved efficiency due to the reduced timing, and consequently, a stable ZVS operation with reduced $E_{rr}$, leading to lower body diode loss. These assumptions have been verified experimentally, as described in Section 5.

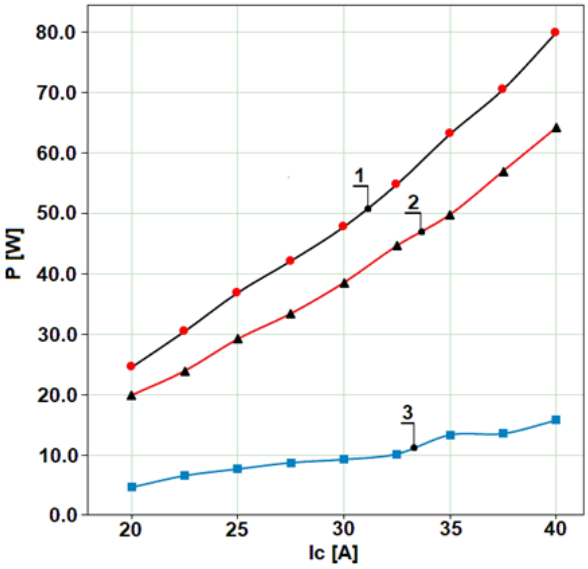



**Figure 6.** Power losses calculated for IGBTs TO-247 3-pin (1) and TO-247 4-pin (2) package. Difference between the power losses (3).

Similarly, the results for Kelvin-connected IGBTs' $E_{ON}$ show an average reduction of 22.8%, and the $E_{OFF}$ reduction is 14.8%, calculated for the range of 20–40 A. The power loss reduction ranges between 4.6 W and 15.7 W, giving a 10 W average result. These results are calculated with a 40 kHz switching frequency, typical for an interleaved PFC-Boost converter.

The statistical results can be supported by concrete data for specific transistors; the main datasheet parameters of the two packages are compared in Table 1. The data presented for $t_{d(on)}$ delay on, $t_r$ rise, $t_{d(off)}$ delay off, $t_f$ fall, and $t_{rr}$ reverse-recovery times determine the energy values $E_{on}$, $E_{off}$, total energy $E_{tot}$, and reverse-recovery energy $E_{rr}$. The comparison is visualised graphically in Figure 7 for MOSFETs and in Figure 8 for IGBTs. For the transistors considered, the total energy is reduced for the 4-pin Kelvin-connected package MOSFET by 78.2% and, for an IGBT in the same package, by 25%.

The results indicate that the lower energy loss for the Kelvin-connected package also reduces the junction temperature. Table 2 shows the thermal parameters for a model based on an equivalent circuit for junction temperature estimation under steady-state conditions (Equations (20)–(23)). Table 3 shows the power loss and junction temperature comparison calculated for certain conditions. The applied thermal model shows a 4-pin MOSFET $T_j$ reduction of 22.1% and 4-pin KE IGBT $T_j$ reduction of 17.8%. The total power loss $P_{tot}$ is calculated as a sum of the switching $P_{ON}$ (Equation (11)) and $P_{OFF}$ (Equation (12)) loss, and the conduction loss is

$$P_{cond} = I_D^2 \times R_{on} \tag{19}$$

where $I_D$ is the average drain current, and $R_{on}$ is the drain-to-source on-state resistance.

**Table 1.** Comparison between the main parameters of 3-pin and 4-pin MOSFETs and IGBTs.

| | MOSFET | | IGBTs | |
|---|---|---|---|---|
| | **IMW65R015M2H TO-247 3-pin** | **IMZA65R015M2H TO-247 4-pin** | **STGW80H65DFB TO-247 3-pin** | **STGW80H65DFB-4 TO-247 4-pin** |
| | Times (ns) | | | |
| $t_{d(on)}$ | 34 | 11.6 | 84 | 75 |
| $t_r$ | 21 | 14.7 | 52 | 35 |
| $t_{d(off)}$ | 22 | 22 | 280 | 336 |
| $t_f$ | 8 | 6.4 | 31 | 23 |
| $t_{rr}$ | 40.5 | 21.5 | 85 | 112 |
| | Energies (µJ) | | | |
| $E_{on}$ | 825 | 84 | 2100 | 1000 |
| $E_{off}$ | 191 | 138 | 1500 | 1700 |
| $E_{tot}$ | 1016 | 222 | 3600 | 2700 |
| $E_{rr}$ | 88.4 | 61.6 | 257 | 170 |

**Table 2.** Thermal model equivalent circuit and base equations.

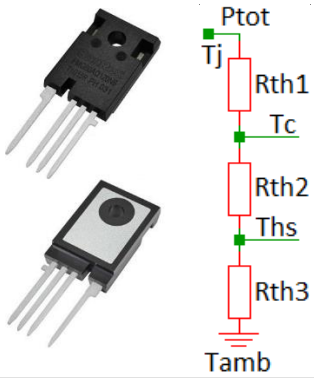
| Package | Equivalent Circuit | Equation | |
|---|---|---|---|
|   | $P_{tot}$—total power at the junction | | |
| | $T_j$—junction temperature | $T_j = (P_{tot} \times R_{th1}) + T_c$ | (20) |
| | $R_{th1}$—junction-to-case thermal resistance | | |
| | $T_c$—case temperature | | |
| | $R_{th2}$—case-to-heat-sink th. resistance | $T_c = (P_{tot} \times R_{th2}) + T_{hs}$ | (21) |
| | $T_{hs}$—heat sink temperature | | |
| | $R_{th3}$—heat-sink-to-ambient th. resistance | | |
| | $T_{amb}$—ambient temperature | $T_{hs} = (P_{tot} \times R_{th3}) + T_{amb}$ | (22) |
| | Total thermal balance | $T_j = (P_{tot} \times (R_{th1} + R_{th2} + R_{th3})) + T_{amb}$ | (23) |

**Table 3.** Comparison of the power losses and temperatures of 3-pin and 4-pin MOSFETs and IGBTs.

| | MOSFET | | IGBTs | |
|---|---|---|---|---|
| | **IMW65R015M2H TO-247 3-pin** | **IMZA65R015M2H TO-247 4-pin** | **STGW80H65DFB TO-247 3-pin** | **STGW80H65DFB-4 TO-247 4-pin** |
| | Datasheet data | | | |
| $R_{th1}$ (°C/W) (datasheet) | 0.44 | | 0.32 | |
| $R_{th2}$ (°C/W) (estimated) | 1 | | 1 | |
| $R_{th3}$ (°C/W) (heat sink selected) | 1.5 | | 1.5 | |
| | Calculated results according to Table 2 | | | |
| $P_{tot}$ (W) | 27.5 | 18.4 | 36.4 | 27.4 |
| $T_j$ (°C) | 120.9 | 94.2 | 142.8 | 117.4 |
| $T_{hs}$ (°C) | 81.2 | 67.6 | 94.7 | 81.2 |

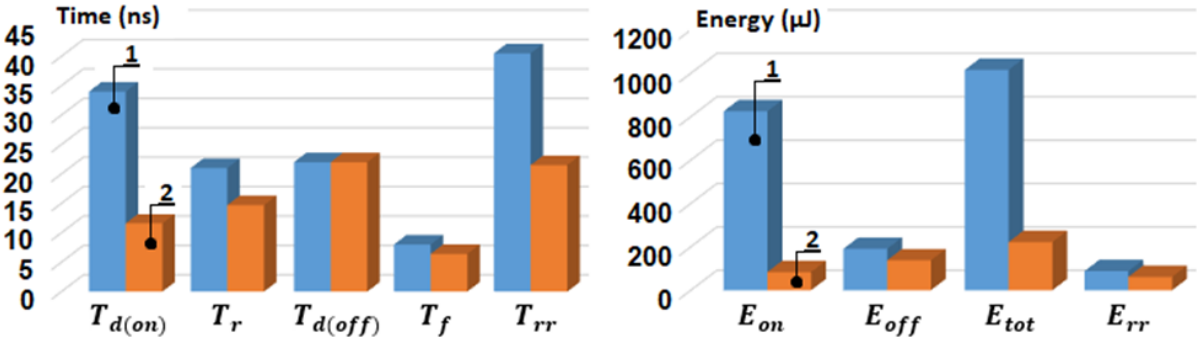



**Figure 7.** Comparison between 3-pin (1—IMW65R015M2H) and 4-pin Kelvin-connected (2—IMZA65R015M2H) packages for the MOSFETs. The data are presented in Table 1.

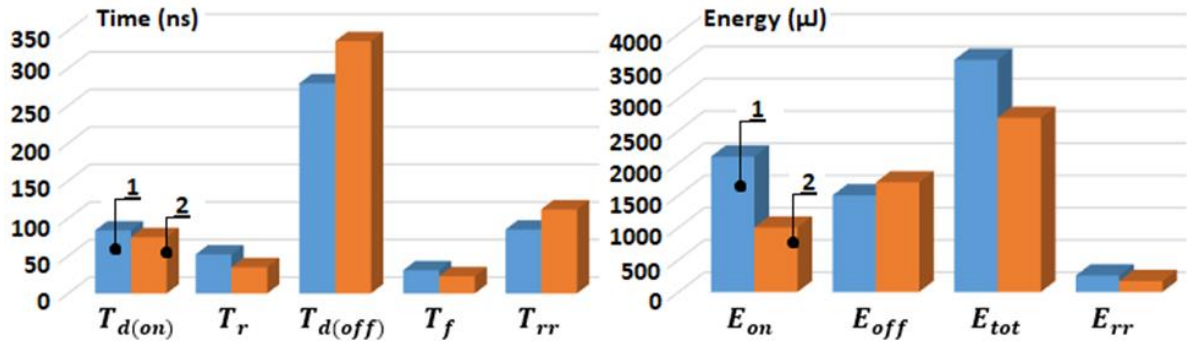



**Figure 8.** Comparison between 3-pin (1—STGW80H65DFB) and 4-pin Kelvin-connected (2—STGW80H65DFB-4) packages for the IGBTs. The data are presented in Table 1.

## 3. Design of LLC Converter

The half-bridge LLC converter (Figure 1) design procedure is based on First Harmonic Analysis (FHA), conducted according to the equivalent circuit in Figure 9 [31–41]. The components of the circuit are as follows: $C_r$ is the resonant capacitor; $L_r$ is the resonant inductor; $L_m$ is the magnetising inductance; $C_p$ is the parasitic capacitance referred from the transformer's primary side and the PCB layout; and $R_{ac}$ is the reflected load resistance.

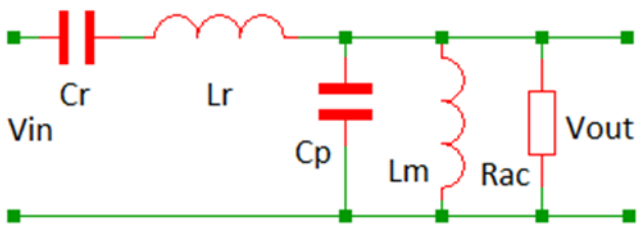



**Figure 9.** Substitute resonance circuit for LLC converter design with FHA.

### *3.1. Methodology for LLC Converter Design Based on FHA*

The methodology for LLC converter design consists of using the main equations to calculate values for the resonant tank and transformer and determine the parameters of the primary-side MOSFETs and secondary-side rectifiers.

In Figure 9, $C_P$ represents the sum of the parasitic drain–source capacitance $C_{DS}$ and parasitic capacitance of the transformer's primary side, which are usually neglected in conventional design procedures. However, to describe the minimum dead time, $C_P$ should not be neglected, especially when high-voltage, high-power MOSFET transistors are used.

The LLC design methodology is given in Table 4, presenting the main equations applied to the converter design in Section 3.2. The gain G calculated (Equation (32)) versus

the normalised frequency $Fx$ (Equation (26)) is depicted graphically in Figure 10. $G_{min}$ and $G_{max}$ are depicted in Figure 11. The gain range determines the switching frequency range. As a product of this, the ZVS region on the primary side is specified, as shown in the exact figure.

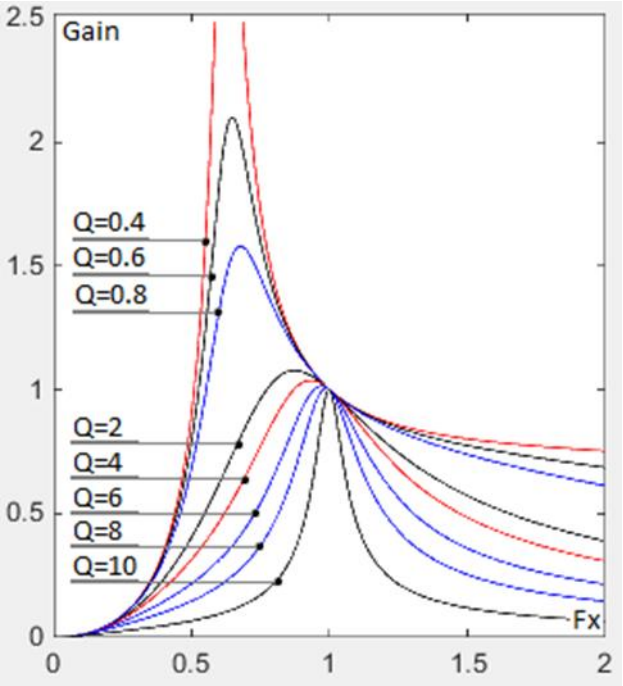



**Figure 10.** A typical gain vs. normalised frequency diagram with different quality factors $Q$.

**Table 4.** A design procedure of the LLC DC-DC converter.

| Description | Equation | Number |
|---|---|---|
| Gain (***G***) | $G(Q,m,F_x) = \left\lvert \frac{V_o}{V_{in}} \right\rvert = \frac{F_x^2(m-1)}{\sqrt{(m.F_x^2-1)^2 + F_x^2.(F_x^2-1)^2.(m-1)^2.Q^2}}$ | (24) |
| Quality factor ($Q$) | $Q = \frac{\sqrt{L_r/C_r}}{R_{ac}}$ | (25) |
| Normalised frequency ( $\boldsymbol{F_x}$) | $F_x = \frac{F_{sw}}{F_r}$ | (26) |
| Resonant factor (***m***) | $m = \frac{L_p}{L_r} = \frac{L_r + L_m}{L_r}$ where $L_p$ is the primary inductance, and $L_r$ is the resonant inductance | (27) |
| Reflected load resistance ($\boldsymbol{R}_0$) | $R_{ac} = \frac{8}{\pi^2}.\frac{N_{pri}^2}{N_{sec}^2}.R_0$ | (28) |
| Resonant capacitor $\boldsymbol{C_r}$ | $C_r = \frac{1}{2\pi Q \times F_r \times R_{ac}}$ | (29) |
| Resonant inductance $\boldsymbol{L_r}$ | $L_r = \frac{1}{(2\pi F_r)^2 \times C_r}$ | (30) |
| Transient function $\boldsymbol{G}(\mathrm{j}\omega)$ | $G(\mathrm{j}\omega) = \frac{V_{out}(\mathrm{j}\omega)}{V_{in}(\mathrm{j}\omega)}$ | (31) |
| Gain ($\boldsymbol{G}$) including $\boldsymbol{C_p}$ | $G(\mathrm{j}\omega) = \frac{\mathrm{j}\omega^2}{\mathrm{j}\omega^4 \frac{L_m C_p}{m} + \mathrm{j}\omega^3 \frac{L_m}{m.R_{ac}} + \mathrm{j}\omega^2\left(\frac{C_p L_m k_r^2}{m} + \frac{1}{m} + 1\right) + \mathrm{j}\omega \frac{L_m k_r^2}{m R_{ac}} + \frac{k_r^2}{m}}$ where $\omega = 2\pi f$; $k_r = 1/\sqrt{L_r.C_r}$ | (32) |

**Table 4.** *Cont.*

| Description | Equation | Number |
|---|---|---|
| ZVS condition | $\frac{(L_m + L_r).I_{mpk}^2}{2} \geq \frac{(2.C_p).V_{in}^2}{2}$ | (33) |
| Required minimum gain $(G_{min})$ | $G_{min} = \frac{N_{tr}.(V_{out\ min} + V_f)}{V_{in\ max}/2}$ | (34) |
| Required maximum gain $(G_{max})$ | $G_{max} = \frac{N_{tr}.(V_{out\ max} + V_f)}{V_{in\ min}/2}$ where $V_f$ is the voltage drop over the diodes $Dr1$ and $Dr2$ | (35) |
| Input LLC power $(P_{in_llc})$ | $P_{in_llc} = \frac{P_{out}}{\eta_{llc}}$ | (36) |
| Minimum input voltage $(V_{in_min})$ | $V_{in_min} = \sqrt{V_{out_pfc}^2 - \frac{2P_{in_llc} \times t_{hold_up}}{C_{out}}}$ | (37) |
| Primary-side turns $(N_{pri_min})$ | $N_{pri_min} = \frac{N_{tr}\left(V_{out} + V_f\right)}{2f_{SWmin} \times G \times \Delta B \times A_e}$ | (38) |
| Transformer turns ratio $(N_{tr})$ | $N_{tr} = \frac{N_{pri}}{N_{sec}}$ | (39) |
| RMS primary side $\left(I_{Cr(RMS)}\right)$ | $I_{Cr(RMS)} = \frac{1}{\eta}\sqrt{\left(\frac{\pi I_{out}}{2\sqrt{2}N_{tr}}\right)^2 + \left(\frac{N_{tr}\left(V_{out} + V_f\right)}{4\sqrt{2}f_r G\left(L_p - L_r\right)}\right)^2}$ | (40) |
| RMS current through each MOSFET $(I_{d_rms})$ | $I_{d_rms} = \frac{\pi}{4} \times I_{out}$ | (41) |

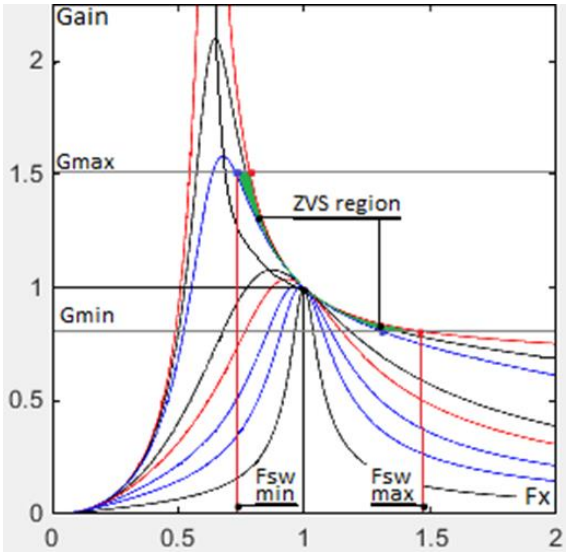



**Figure 11.** Quality factor, normalised switching frequency range and zero-voltage switching (ZVS) regions.

### *3.2. LLC DC-DC Converter Design Case Study*

The foregoing LLC design methodology (Equations (24)–(41)) is for the converter design as a part of the overall battery charger (Figure 1). The transistor's power loss is considered with ZVS conditions (Equations (15)–(18)) calculated for a Kelvin-connected 4-pin MOSFET. The LLC DC-DC converter design specification and results are presented in Table 5. Figure 12 shows the gain vs. the switching frequency for different resonant factors $m$ (Equation (27)).

**Table 5.** LLC input data and design results.

| **Design Specification** | | | |
|---|---|---|---|
| **Input Parameters** | | **Output Parameters** | |
| Minimum voltage | 350 V | Minimum voltage | 200 V |
| Nominal voltage | 400 V | Nominal voltage | 300 V |
| Maximum voltage | 420 V | Maximum voltage | 400 V |
| Estimated efficiency | 0.96 | Output power | 3600 W |
| Minimum switching frequency | 75 kHz | Nominal output current | 12 A |
| Resonant frequency | 100 kHz | | |
| Maximum switching frequency | 150 kHz | | |
| Design parameters | | | |
| Input power | 3750 W | Magnetising inductance | 25.2 µH |
| Transformer turns ratio | 0.5 | Resonant inductance | 6.4 µH |
| Minimum gain | 0.64 | Resonant capacitance | 400 nF |
| Maximum gain | 1.93 | Nominal resistance | 5.1 Ω |
| Quality factor | 0.88 | Peak primary-side current | 26.6 A |
| Resonant current | 31.4 A | Maximum output current | 12.5 A |
| Magnetising current at minimum switching frequency | 11.4 A | Secondary half-wave current | 8.8 A |
| Magnetising current at nominal switching frequency | 8.5 A | Energy accumulated in parasitic capacitors *Cds* in both transistors | 88 µJ |
| Magnetising current at maximum switching frequency | 5.6 A | Dead time | 33.3 ns |
| Selected semiconductors | | | |
| Primary-side transistors: IMZA65R015M2H (CoolSiC™ 4-pin Kelvin-connected MOSFET) | | | |
| Secondary-side rectifiers: VS-E5PH7506LHN3 | | | |

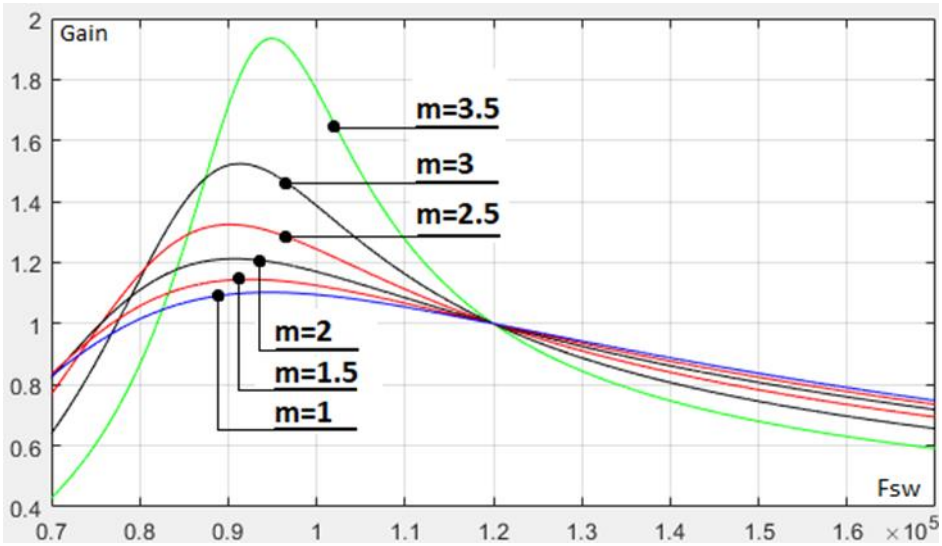



**Figure 12.** Gain vs. switching frequency with different resonant factors *m*.

The transistor's power loss under ZVS conditions (Equations (15)–(18)) at 3.6 kW output was evaluated for the selected Kelvin-connected 4-pin MOSFET. The results are as follows: $Q_{Gzvs} = 110$ nC, $E_{ONzvs} = 825$ nJ, $E_{OFFzvs} = 1032$ nJ, and $E_{zvs} = 1.857$ µJ. The

switching loss at a maximum operating frequency of 150 kHz will be 0.279 W. The conducting loss is calculated at 12.74 W (Equation (19)), rounding the total loss to 13 W. Applying the equivalent model (Equations (20)–(23)), the expected temperature allocation will be $T_j = 78.2$ W and $T_{hs} = 59.5$ W with the suggested 1.5 C/W heat sink thermal resistance.

## 4. The Design of the PFC-Boost Converter

The interleaved PFC-Boost topology chosen (Figure 1) aims to distribute the losses amongst the three channels, reducing the stress on individual devices. The converter is based on 4-pin Kelvin-connected IGBTs.

### *4.1. Methodology for PFC-Boost Design*

The input PFC power $P_{in_pfc}$ is determined from the required output PFC power $P_{out_pfc}$, considering the input LLC power calculated in (Equation (36)) $P_{out_pfc} = P_{in_LLC}$:

$$P_{in_pfc} = \frac{P_{out_pfc}}{\eta_{pfc}} \tag{42}$$

where $\eta_{pfc}$ is the estimated PFC-Boost converter efficiency.

The total output current $I_{out_pfc}$ is

$$I_{out_pfc} = \frac{P_{out_pfc}}{V_{out_pfc}} \tag{43}$$

where $V_{out_pfc}$ is the output PFC-Boost voltage.

The current through each PFC-Boost channel, considering the number of channels, $N_{ch}$, is given by

$$I_{pfc_ch} = \frac{P_{out_pfc}}{V_{out_pfc} \times N_{ch}} \tag{44}$$

The duty cycle $D_{pfc}$ at the maximum output voltage $V_{out_pfc}$ is calculated from the maximum input voltage $V_{in_max}$:

$$D_{pfc} = \frac{V_{out_pfc} - \sqrt{2}V_{in_max}}{V_{out_pfc}} \tag{45}$$

The current ripple $\Delta I_{boost}$ in the Boost inductor at the minimum input voltage, i.e., the worst-case conditions, depends on the duty cycle and the switching frequency as follows:

$$\Delta I_{boost} = D_{pfc} \times \frac{V_{out_pfc} - \sqrt{2}V_{in_min}}{V_{out_pfc}} \times \frac{1}{F_{sw}} \tag{46}$$

The average inductor current $I_{avg_pfc}$ is calculated at the minimum input voltage $V_{in_min}$ as follows:

$$I_{avg_pfc} = \frac{\sqrt{2}V_{out_pfc}}{V_{in_min} \times \eta_{pfc}} \tag{47}$$

The inductance of each PFC inductor $L_{pfc}$ must be calculated at a specified ripple factor $K_{rf}$ and switching frequency $F_{sw}$:

$$L_{pfc} = \frac{\sqrt{2}V_{in_min}}{K_{rf} \times I_{avg_pfc}} \times \frac{V_{out_pfc} - \sqrt{2}V_{in_min}}{V_{out_pfc}} \times \frac{1}{F_{sw}} \tag{48}$$

The peak inductor current $I_{Lpk}$ applies to an inductor selection with no core saturation, calculated from

$$I_{Lpk} = I_{avg_pfc} \times \left(1 + \frac{K_{rf}}{2}\right) \tag{49}$$

For a maximum output voltage ripple $V_{pfc_ripp}$, the minimum capacitance of the output capacitor $C_{out}$ is given by

$$C_{out} > \frac{I_{out_pfc}}{2\pi F_{in} V_{pfc_ripp}} \quad (50)$$

where $F_{in}$ is the input line frequency.

### *4.2. PFC-Boost Converter Design Case Study*

The interleaved PFC-Boost converter is designed to match the LLC converter (Section 3.2), supplying the necessary input power of 3750 W, 400 V. The design results (Equations (42)–(50)) are given in Table 6.

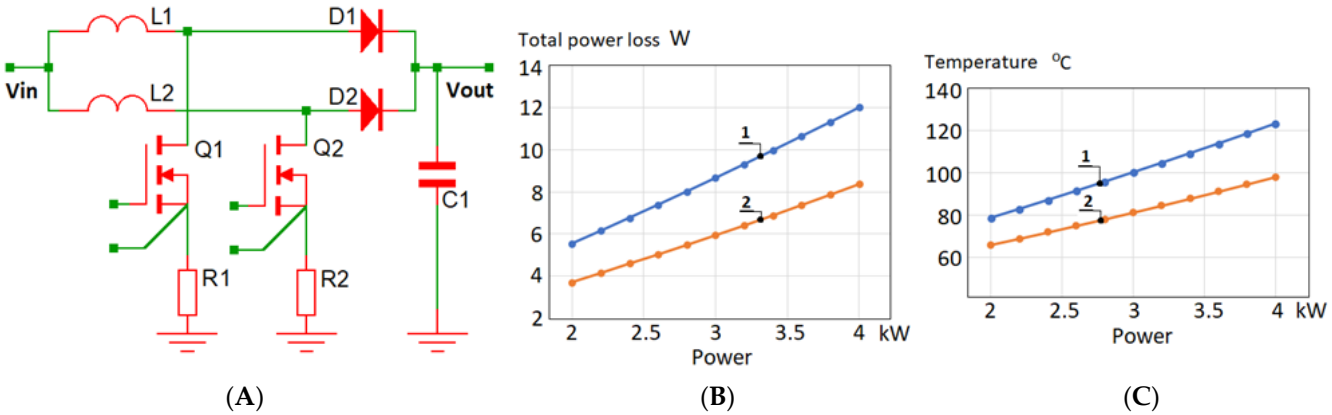
**Table 6.** Interleaved PFC design results.

| **Design Specification** | | | |
|---|---|---|---|
| **Input Parameters** | | **Output Parameters** | |
| Minimum AC voltage | 180 V | Nominal output DC voltage | 400 V |
| Maximum AC voltage | 264 V | Minimum output DC voltage | 350 V |
| Line frequency | 50 Hz | Output power | 3750 W |
| Number of channels | 3 | Output voltage ripples | 0.05% |
| Switching frequency | 40 kHz | | |
| Efficiency (estimated) | 92% | | |
| Design parameters | | | |
| Input power | 4076.1 W | Duty cycle | 0.399 |
| Nominal output DC current | 9.4 A | Inductor | 130 µH |
| Current per channel | 3.1 A | Inductor peak current at line brownout 160 V | 21.3 A |
| Power per channel | 1250 W | Output capacitor | 1500 µF |
| Maximum switch current | 5.2 A | | |
| Selected semiconductors | | | |
| IGBT: STGW80H65DFB-4 | | | |
| Fast-recovery diode: VS-E5PH7506LHN3 | | | |

Applying the analytical power loss model (Equations (1)–(14) and (19)) and the thermal model (Equations (20)–(23)), the results for the selected 4-pin Kelvin-connected IGBT are a conduction loss of 0.24 W, a switching loss of 22 W, a total loss of 22.24 W, a junction temperature of 102.73 °C, and a heat sink temperature of 95.61 °C. As a comparison, the same IGBT with a standard 3-pin connection, based on the data in Table 1, shows a total loss of 31.24 W in the same application, leading to a junction temperature of 128.1 °C and a heat sink temperature of 118.1 °C. The total power loss dissipated from the three interleaved IGBTs is 93.7 W for the 3-pin package and 66.7 W for the Kelvin-connected package. Although both packages show satisfactory results, the power loss reduction of 27 W, or 28.8%, shows that 4-pin discrete IGBTs could be preferred for this application.

Further significant power loss reduction could be achieved by applying CoolSiC 4-pin Kelvin-connected MOSFETs. Using the data in Table 1, the standard 3-pin package shows a power loss of 11.1 W and a junction temperature of 72.6 °C, while the 4-pin package dissipates 7.46 W and has a temperature of 61.9 °C. The results show that this approach would allow the interleaved Boost-PFC converter to be completed with only two transistors and a reduced heat sink size for power density improvement. In this case, the Boost PFC was reconstructed with two interleaved MOSFETS (Figure 13A). The comparison of 3-pin

(diagram 1) and 4-pin (diagram 2) power losses (Figure 13B) and temperatures (Figure 13C) was conducted with a switching frequency of 66 kHz, according to the ASIC utilised, and a heat sink of 5.5 C/W, leading to power density improvement.



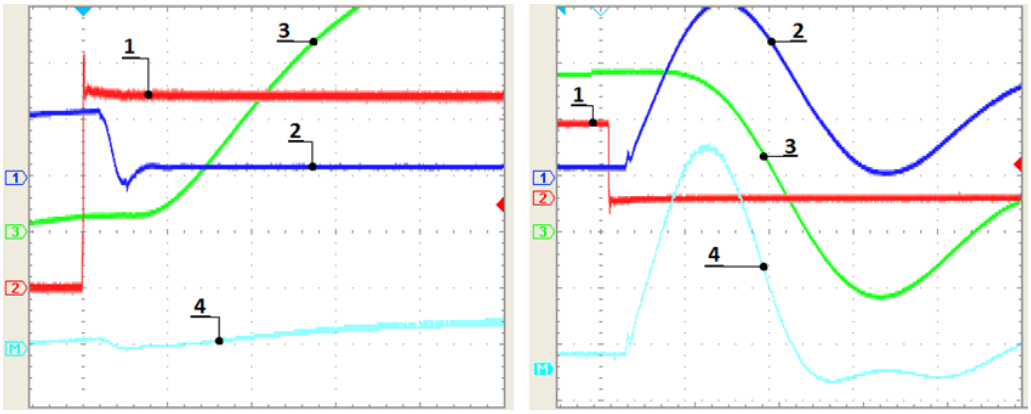

(**A**) (**B**) (**C**)

**Figure 13.** (**A**) Boost-PFC converter based on two interleaved SiC MOSFETs; (**B**) comparison between power losses; (**C**) temperature comparison between (1) 3-pin and (2) 4-pin packages.

## 5. Experimental Setup

The experimental verification started with testing both packages, 3-pin and 4-pin TO-247, as individual switches, as shown in Figure 2, under the same conditions. The experiments were conducted with standard laboratory equipment, such as a Keysight DSOX1204G oscilloscope, an HMC8015 Rohde & Schwarz power analyser, a power supply, and digital multimeters. The experiments were conducted with both Boost-PFC and LLC converters and the entire battery charger (Figure 1). The measurements were taken for input/output power, efficiency, power loss, transistor junctions, gate driver control signals, and transistor temperature. The converters were tested under nominal and worst-case conditions, applying maximum power at minimum input voltage.

Oscillograms for the 3-pin results are depicted for switch-on (Figure 14A) and switch-off (Figure 14B) as follows: Trace 1 shows the PWM; 2 is the collector–emitter voltage; 3 is the collector current; and 4 is the result of using the mathematical function for power calculation, multiplying the current and voltage, embedded in the oscilloscope. The experiments were conducted with IGBT STGW80H65DFB-4 at a switching frequency of 40 kHz, according to the Boost PFC specified in Table 6.




(**A**) (**B**)

**Figure 14.** Experimental characteristics of 4-pin IGBT TO-247 package. (**A**) Turn-on and (**B**) turn-off processes. 1—PWM; 2—collector current; 3—collector–emitter voltage; 4—power calculation.

A comparison of the oscillations in the gate-drive circuit is shown in Figure 15. The voltage over $V_{Ls}$ (Figure 2A) during the 3-pin package switched-on process is shown in Figure 15A, and the voltage over $V_{Lgs}$ (Figure 2B) for the 4-pin package is given in Figure 15B. It must be clarified that the result strongly depends on the board layout.

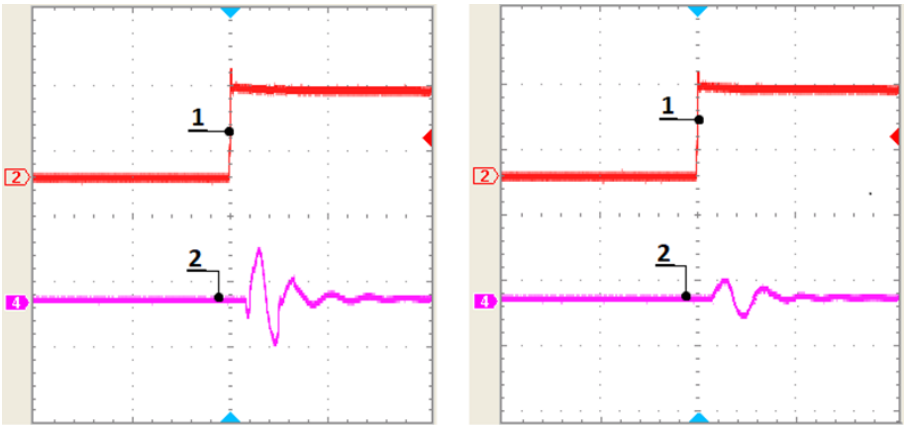



**Figure 15.** Oscillations of the source inductances of (**A**) 3-pin and (**B**) 4-pin IGBT TO-247 packages. 1—PWM; 2—voltages over the straight inductances $V_{Ls}$ and $V_{Lgs}$ (Figure 2).

As a continuation of the previous experiment, the voltage applied to the gate is depicted in Figure 16 with diagram 4. The measurement shows the minimal impact of the Miller plateau for the 4-pin package.

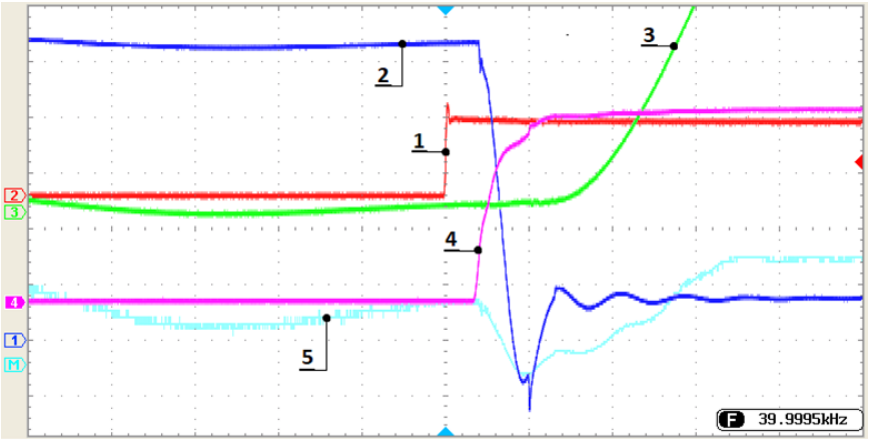



**Figure 16.** Gate-drive characteristics of 4-pin IGBT TO-247 package. 1—PWM; 2—collector–emitter voltage; 3—collector current; 4—gate–emitter voltage; 5—math function for power calculation.

The automotive battery charger has been prototyped and experimentally tested to support the analytical data and the design procedures. Both converter stages were initially tested in general, depicting their operation over the entire charger power range. Eventually, the integrated 4-pin Kelvin-connected operation was tested.

The PFC-Boost converter was tested according to the design described in Section 4.2. The results are presented as follows:

- Figure 17 shows a single channel of the interleaved PFC-Boost converter implemented with three IGBTs, as suggested in the initial design (Table 6). The gate PWM (1) controls the switch with the collector-to-emitter voltage (2) and the collector current (3). The diode conducts the current in the OFF switch state (4).

- Figure 18 shows the input PFC-Boost rectified DC voltage (1) without filtering. The PFC operates by varying the PWM (3) signal according to the input voltage variation and the collector-to-emitter voltage (2), leading to a stable output DC current (4).
- Figure 19 shows the converter operating with the PFC at a nominal load (Figure 19A) and during the charger's stand-by without the PFC (Figure 19B). The result demonstrates the ability of the converter to correct the power factor in the entire power range.

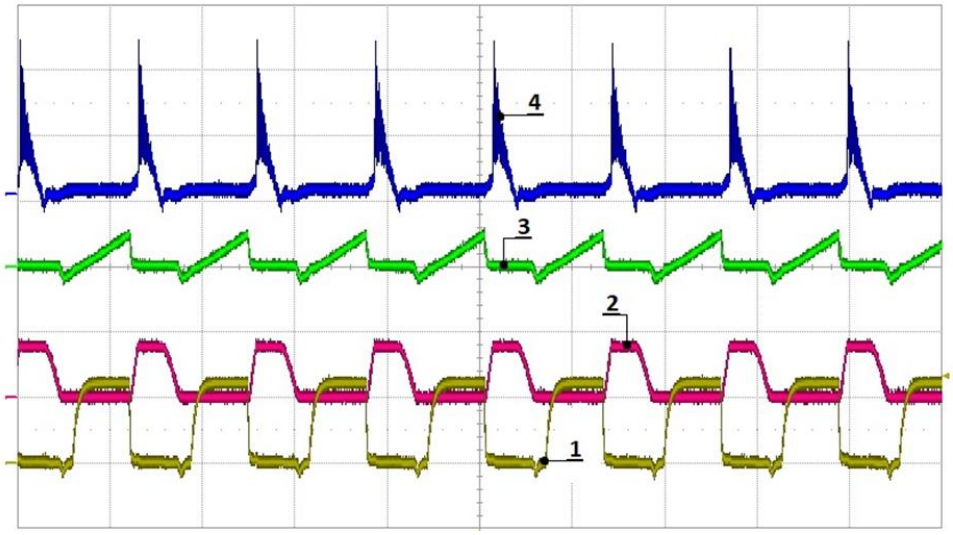



**Figure 17.** Operation of PFC-Boost converter (single channel). (1) Gate PWM; (2) collector–emitter of IGBT transistor; (3) IGBT collector current; (4) diode current.

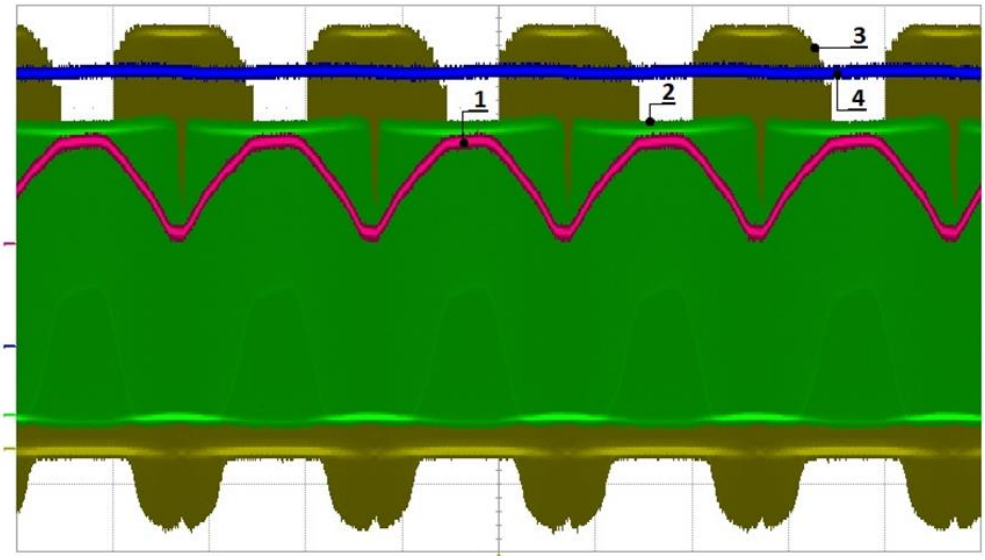


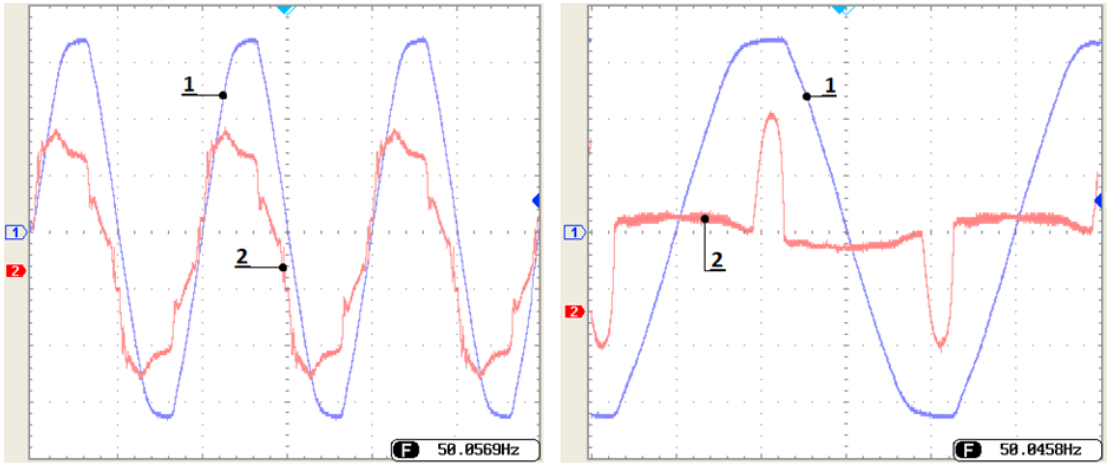

**Figure 18.** Input PFC-Boost converter (single channel). (1) Input DC voltage; (2) collector–emitter voltage; (3) gate PWM; (4) output DC current.

The LLC converter was tested first to show the ZVS operation with 4-pin Kelvin-connected transistors, according to Figure 1 and the design in the case study in Section 3.2, Table 5. The oscillograms present the following results:

- Figure 20A shows the ZVS operation in which the voltage at the middle point of the half-bridge (3) switches in the dead time between the two transistors' PWM (1, 2). The current through the resonant capacitor and transformer (4) is depicted under the resonant frequency under output power control. Figure 20B shows the magnetising

current (3) on the primary side. Both oscillograms depict the accurate operation of the LLC converter completed with 4-pin Kelvin-connected MOSFETs.

- Figure 21A shows the ZVS in greater resolution, depicting the voltage switching at the zero point (3) between the drain-to-source voltages over the two MOSFETs (1, 2) in the half-bridge. The output DC current is shown in diagram 4. Figure 21B shows the output voltage (1) and current (2) in better resolution as part of the switching process. The output ripples are according to those accepted in the design procedure.




(**A**) (**B**)

**Figure 19.** Input battery charger voltage (1) and current (2). Operation with PFC (**A**) and without PFC (**B**).

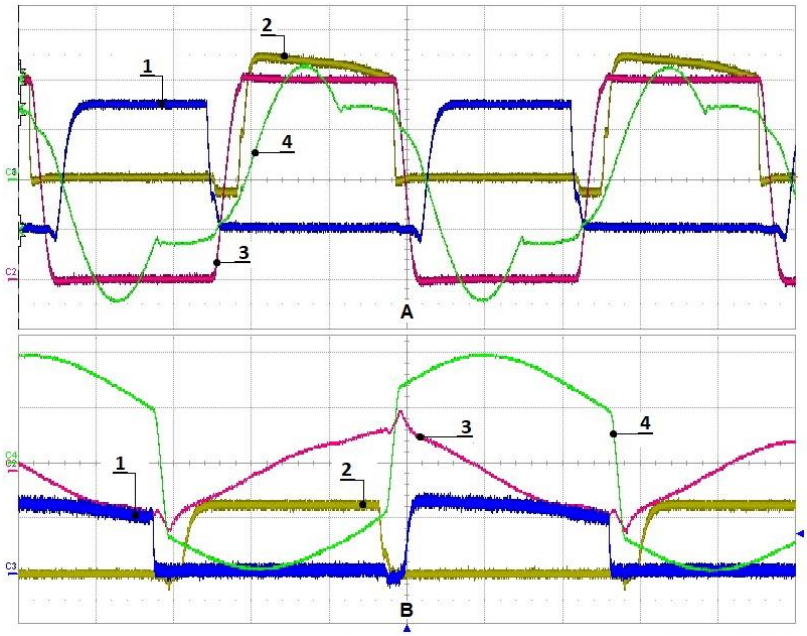



**Figure 20.** LLC primary-side operation. (**A**) Below resonant frequency. (1) High-side MOSFET gate driver; (2) low-side MOSFET gate driver; (3) middle-point ZVS; (4) current through the resonant capacitor. (**B**) (1) High-side MOSFET gate driver; (2) low-side MOSFET gate driver; (3) magnetising current; (4) current through the resonant capacitor.

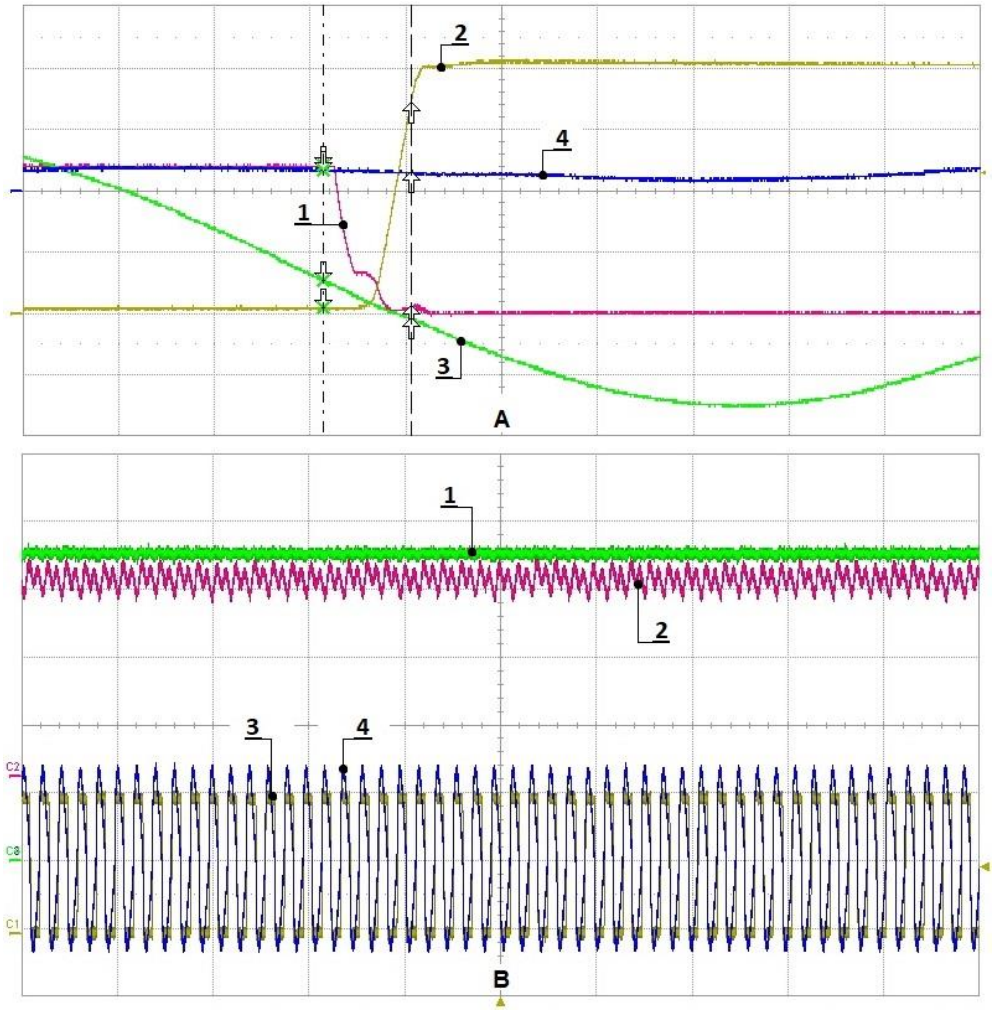



**Figure 21.** LLC output voltage and current. (**A**) (1) Low-side gate drain-to-source voltage; (2) high-side drain-to-source voltage; (3) voltage over the resonant capacitor, ZVS; (4) secondary-side output current. (**B**) (1) Output voltage; (2) responses in the output current; (3) primary-side MOSFET switching; (4) primary-side voltage at the middle point at the resonant frequency.

The energy efficiency of the Boost-PFC converter has been experimentally verified. Figure 22A compares the total transistors' power loss, calculated from the measurement results over the entire power range. Diagram 1 shows the total loss of the three interleaved 4-pin Kelvin-connected IGBTs, and diagram 2 depicts the power loss of their 3-pin counterparts. The difference is shown in Figure 22B. As measured experimentally, the power loss reduction at the nominal rated power of 3750 W is 26.63 W or 8.9 W per transistor in this design. This contributes to a total efficiency improvement of 98% to 98.71% (Figure 23A) or 0.71% (Figure 23B) estimated for the interleaved transistors (Q1, Q2, and Q3, Figure 1).

Temperature rises were investigated using thermal imaging to confirm the power loss reductions. Images from both packages are compared in Figure 24: (A) 4-pin, showing 85.6 °C on the transistor cage, and (B) 3-pin, reaching 101.2 °C. The Kelvin-connected package connected to a heat sink for the presented experiments is shown in Figure 24C.

Figure 25 depicts a thermal image of the entire Boost-PFC power stage with three 4-pin TO-247 IGBTs. The final prototype is completed with heat sinks with a reduced surface, as suggested in the design above. The maximum temperature of the heat sink reaches 114.4 °C.

The LLC converter's 4-pin MOSFET transistors' thermal operation, according to the design in Section 3, is shown in Figure 26. The measured heat sink temperature is 53.5 °C versus the calculated temperature of 59.5 °C (Table 5).

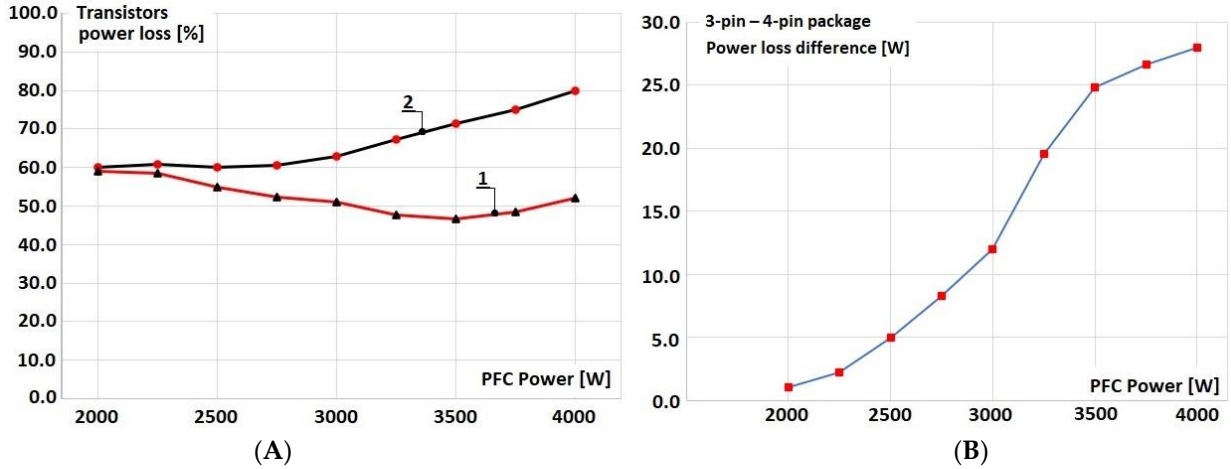



**Figure 22.** A comparison between the two packages. (**A**) The power loss of 4-pin (1) and 3-pin (2); (**B**) the power difference between the two packages, diagrams 1 and 2.

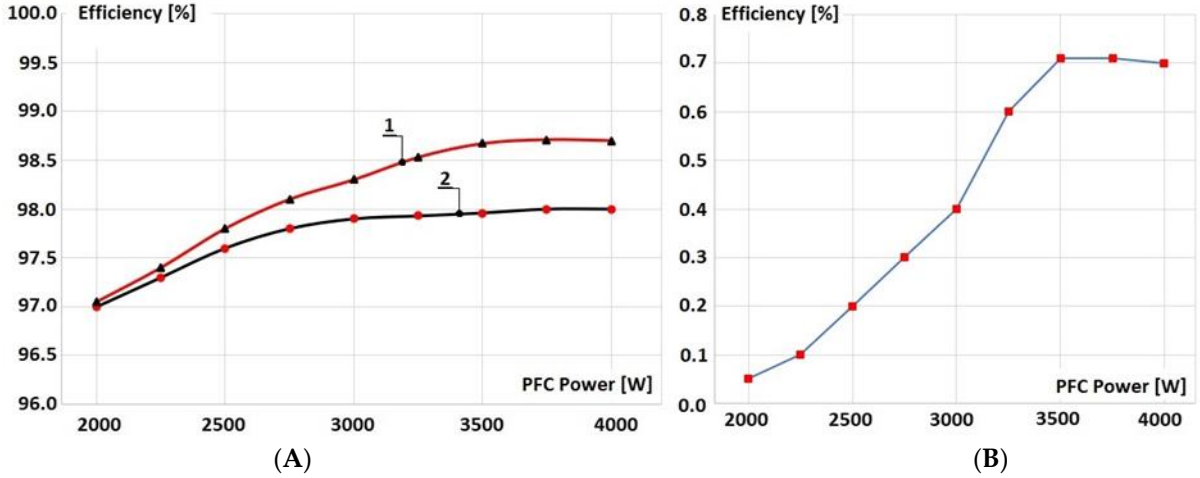



**Figure 23.** The efficiency of the Boost PFC, estimated for the transistors Q1, Q2, and Q3, Figure 1: (**A**) 4-pin (2) and 3-pin (1); (**B**) the efficiency difference between diagrams 1 and 2.

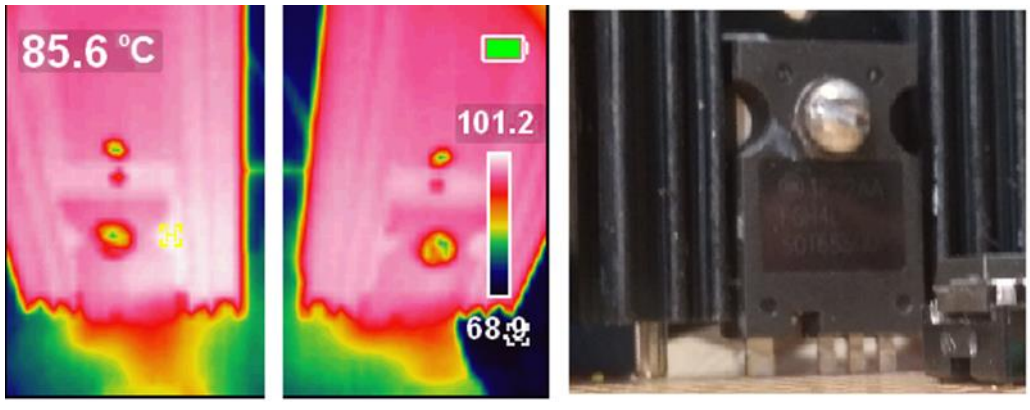



**Figure 24.** Thermal images of TO-247 (**A**) 4-pin Kelvin-connected and (**B**) 3-pin IGBTs; (**C**) 4-pin Kelvin-connected TO-247 package connected to a heat sink.

The data obtained from the design and experimental measurements are summarised in Table 7. The results mismatch between the two studies is due to the 30% design safety margins applied to the datasheet parameters.

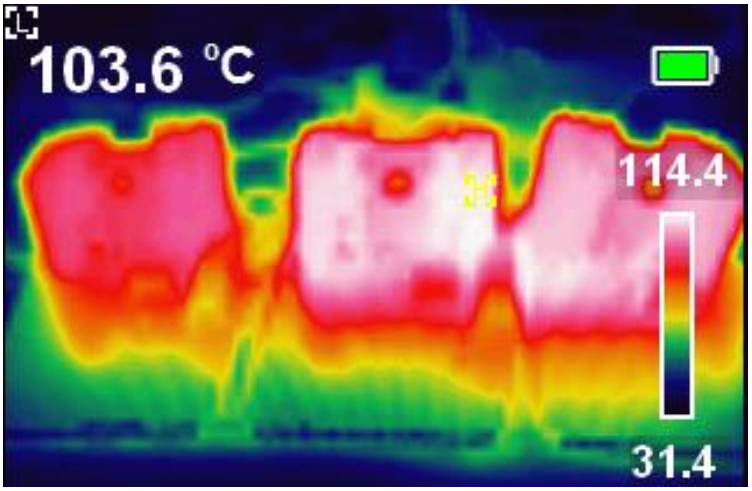



**Figure 25.** Thermal image of the 4-pin IGBTs in the interleaved Boost PFC.

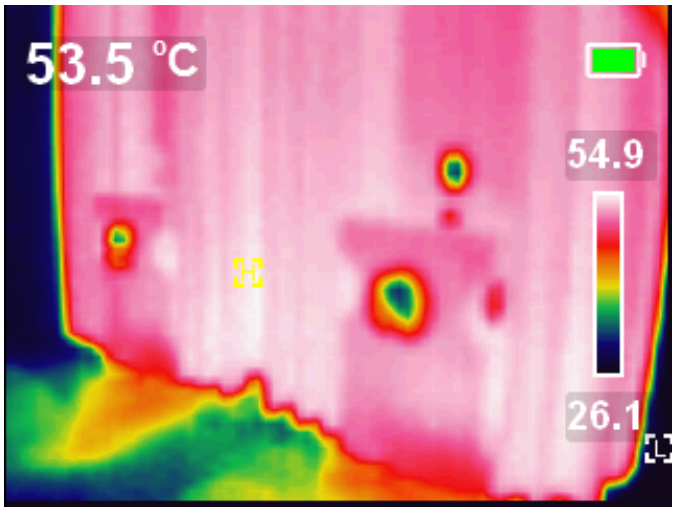



**Figure 26.** Thermal image of the MOSFETs in the LLC converter.

**Table 7.** An experimental comparison between 3-pin and 4-pin IGBTs, with the TO-247 package, used for Boost-PFC design and prototyping.

| | **3-pin IGBTs** | | | **4-pin IGBTs** | | |
|---|---|---|---|---|---|---|
| | **Total Loss for Three Interleaved PFC IGBTs (W)** | **Total Loss per IGBT (W)** | **Heat Sink/Junction Temperatures (°C)** | **Total Loss for Three Interleaved PFC IGBTs (W)** | **Loss per IGBT (W)** | **Heat Sink/Junction Temperatures (°C)** |
| Calculated | 93.7 | 31.24 | 118.1/ 128.1 | 66.6 | 22.2 | 95.61/ 102.73 |
| | • The total 4-pin package power loss reduction for 3 interleaved PFC IGBTs is 27.1 W.<br>• The single-IGBT power loss reduction is 9.04 W. | | | | | |
| Measured | 75 | 25 | 101.2/ 95.6 | 48.4 | 16.1 | 85.6/ 78.5 |
| | • The total 4-pin package power loss reduction for 3 interleaved PFC IGBTs is 26.63 W.<br>• The single-IGBT power loss reduction is 8.9 W.<br>• The junction temperatures are estimated according to package and heat sink temperatures. | | | | | |

Finally, the Electromagnetic Interference (EMI), measured for the entire charger, is depicted in Figure 27. EMI improvement measures included the PCB design, specifically focused on the gate drivers, the parasitic element reduction enabled by the suggested switches, and proper grounding and shielding.

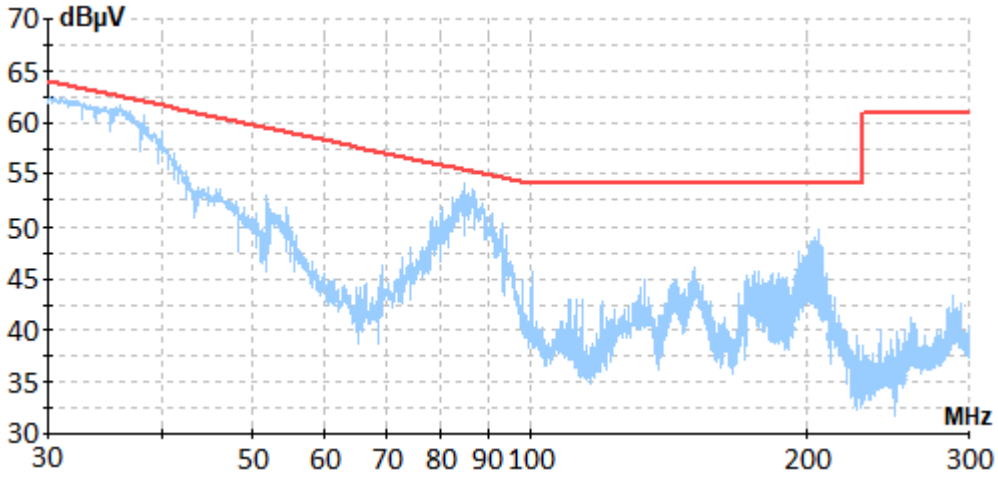



**Figure 27.** Electromagnetic Interference measured for the tested battery charger.

## 6. Results and Discussion

The results obtained in the conducted research can be summarised as follows:

- The statistical data collected from multiple 4-pin Kelvin-connected and their 3-pin analogue TO-247 IGBTs and MOSFETs show a power loss reduction for the 4-pin package. The calculations were conducted using Equations (1)–(19) describing both packages' power losses, and these are depicted graphically (Figures 3–6) in the range 20–30 A, consistent with conditions in automotive onboard battery chargers. The results show that the expected power loss reduction obtained by applying Kelvin-connected transistors is between 8.6 W and 17.9 W.
- The same calculations were applied to two specific IGBTs and MOSFETs (Table 1), including thermal models (Table 2) based on the equivalent circuits. The preliminary study shows that it can be expected that a 4-pin Kelvin-connected package offers a power loss reduction, leading to lower junction temperatures (Table 3). The results are obtained due to reduced ON and OFF switching times and, respectively, $E_{on}$ and $E_{off}$ energies, for the Kelvin-connected transistors, as depicted in Figures 7 and 8.
- The 4-pin Kelvin-connected packages were successfully utilised in the design methodology of the Boost PFC (using IGBTs) and the resonant LLC converter (using MOSFETs). The case studies for both converters show that applying Kelvin-connected IGBTs to the interleaved Boost PFC reduces the switching loss. For the LLC converter, CoolSiC 4-pin MOSFETs can be recommended. The experimental study shows the stable operation of the Boost-PFC (Figures 17 and 18) and LLC converters (Figures 20 and 21).
- The experimental study confirms the analytical results, showing a total power loss reduction of 26.63 W, or 8.9 W per transistor, for the three interleaved IGBTs in the Boost-PFC converter. The power loss reduction and efficiency improvement, experimentally depicted in Figures 23 and 24, match the preliminary results presented in Section 2 and shown in Figures 3–6.
- Due to the power loss reduction, the heat sink temperature decreases proportionally from 101.2 °C to 85.6 °C, as the infrared images in Figure 22 show. Further temperature reductions, potentially leading to heat sink minimisation and power density improvement, could be achieved by applying SiC 4-pin MOSFET to the Boost-PFC converter (Figures 23 and 24).

- The experimental study also shows fewer gate circuit oscillations in both converters (Figure 15) and stable operation on the gate-drive circuits (Figures 14 and 16). This result leads to acceptable EMI, as depicted in Figure 25.

Based on the presented results, it can be concluded that the 4-pin Kelvin-connected TO-247 transistors are a good candidate for further power loss reduction and efficiency improvement in power converters. In the presented research, such a result was demonstrated in the context of Boost-PFC and DC-DC LLC converters as a part of the automotive battery charger.

## 7. Conclusions

This research has conducted and presented analytical and experimental studies focused on the Kelvin-connected transistor package and its utilisation in the primary converters of a battery charger topology. The thorough literature review supported and defined the necessity of the presented results. The primary data obtained were used in the following design processes. The central battery charger converters, Boost PFC and DC-DC LLC, were designed with 4-pin Kelvin-connected TO-247 IGBT and MOSFET packages. Finally, the experimental results confirmed the expected power loss reduction and efficiency improvement. Furthermore, both converters showed stable operation with minimised oscillations, improved thermal operation, and power density improvement.

**Author Contributions:** Conceptualization, B.D. and R.M.; methodology, B.D.; validation, B.D. and R.M.; formal analysis, B.D. and R.M.; investigation, B.D. and R.M.; resources, B.D.; data curation, R.M.; writing—original draft preparation, B.D.; writing—review and editing, R.M.; visualization, B.D.; supervision, R.M. All authors have read and agreed to the published version of the manuscript.

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**Conflicts of Interest:** The authors declare no conflicts of interest.

## Appendix A

**Table A1.** IGBTs with the 4-pin Kelvin-source TO-247 package, used for the statistical analysis.

| Infineon [60] | ON Semiconductor [61] | ST Microelectronics [62] |
|---|---|---|
| IPZA65R029CFD7; IPZA60R024P7 | FCH023N65S3L4 | stw48n60m2-4; stw56n60m2-4 |
| IPZA60R016CM8; IPZ65R019C7 | FCH041N65EFL4 | stw56n65m2-4; stw57n65m5-4 |
| IPZ60R017C7; IMZA65R030M1H | NTH4L027N65S3F | stw65n023m9-4; stw68n60m6-4 |
| IMZA65R027M1H; IMZA65R027M1H | NTH4L040N65S3F | stw70n60dm6-4; stw70n60m2-4 |
| IMZA65R020M2H; IMZA65R015M2H | NVH4L040N65S3F | stw75n60m6-4; stw75n65dm6-4 |

**Table A2.** MOSFETs with Kelvin source TO-247 4pin, used for the statistical analysis.

| Infineon [60] | ON Semiconductor [61] | ST Microelectronics [62] |
|---|---|---|
| IGZ50N65H5; IGZ75N65H5; IGZ100N65H5<br>IKZ50N65EH5; IKZ75N65EH5; IKZ75N65ES5<br>IKZA50N65EH7; IKZA75N65EH7; IKZA100N65EH7 | FGH4L50T65MQDC50<br>FGH4L75T65MQDC50<br>FGH75T65SHDTL4<br>FGH75T65SQDNL4<br>FGHL50T65MQDTL4<br>FGHL75T65MQDTL4 | STGW50H65DFB2-4<br>STGW60H65DFB-4<br>STGW75H65DFB2-4<br>STGW100H65FB2-4 |

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