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Highly Accurate Digital Current Controllers for Single-Phase LCL-Filtered Grid-Connected Inverters

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Abstract: Photovoltaic (PV) systems are the most promising technology for residential installation as an alternative source of energy. To interface the primary source of PV to the electrical grid, an LCL-filtered inverter is being broadly adopted due to its low volume compared to the L-filtered one and the superior ability to filter high-frequency harmonics. In this context, this paper proposes highly accurate digital current controllers for single-phase LCL-filtered grid-connected inverters. The proposed controllers are: Integral-single-lead, integral double-lead, integral double-lead taking into account the effect of pulse width modulation (PWM) delay and the proportional-resonant (PR). These controllers are different from the traditional Proportional-Integral (PI), Proportional-Derivative (PD), and Proportional-Integral-Derivative (PID). One of the novelties of this paper is the detailed, step-by-step procedure for tuning each parameter of the proposed digital controllers considering the dynamic behavior of the LCL filter. The proposed PR has a different and more straightforward tuning methodology than those procedures commonly found in the literature. Therefore, this paper is an attractive tool for a fast, accurate, and reliable way to tune digital current controllers for a single-phase LCL-filtered grid-connected inverter. The controllers were verified in the digital signal controller (DSC) TMS320F28335 while the power structure runs in a hardware-in-loop (HIL device). Results show the efficacy of the proposed controllers.

Keywords: LCL filter; current controller; power inverter; PV systems

1. Introduction

1.1. Background and Literature Review

The high penetration of PV system in residences brought new challenges to the distribution utilities. Several concerns never worried about before are now causing severe problems, obliging utilities to impose restrictions on the customers. One such issue is the injection of high frequencies components generated by the pulse width modulation (PWM) of the electronics' converters used in PV systems [1,2]. This led industries and academia to develop high-order passive filters. After some decades, the LCL-type become the most dominant output filter of power inverters. Some reasons that made the LCL-type one of the best options are the low-volume compared to L-type and the superior ability to filtering high frequencies components. However, the LCL filter presents a natural resonant frequency, which needs particular attention to prevent high oscillation and instability through it.

At the same time, the development of the current controller for LCL-filter grid-connected inverters took special attention in the scientific community. The design of an accurate current controller is vital for the appropriate operation of the inverter. The controller must follow its reference signal with negligible steady-state error and must be able to reject disturbances that may appear in the systems.

Regarding the power distribution system, the LCL-filter inverter usually can be connected to single- or three-phase systems. For residential installations of PV, the connection to a single- or three-phase distribution system often depends on the rated power of the PV and the availability of such systems. For high power PV systems, the three-phase grid is preferably chosen [3]. Nevertheless, for low power and limited availability, several PV systems with LCL-filtered inverter are connected to single-phase distribution system around the world.

Current controllers for LCL-filtered grid-connected inverter are continually being proposed in the literature [3]. There are a variety of types of controllers like the proportional-integral (PI) [4], PR [5], sliding mode, fuzzy-based [6], model predictive control (MPC) [7,8], and so on. Most of the research covering such controllers is proposed for a three-phase system, admitting that the parameters of the distribution system are known and they do not change along time [9]. In case of real violation of such assumptions, the performance of the controller may be deteriorated. Controllers that can operate under uncertainties in the parameters of the distribution system were proposed in [10,11]. Their proposals are for three-phase systems and do not pay the desired attention to single-phase systems.

Three-phase current controllers are mature and very well spread in the literature. In [12], a controller based on state feedback linearization was proposed. The nonlinear system of the LCL-filtered grid-connected inverter is mapped to a controllable standard type. Then, classical linear system control method is adopted to design the controller. A PR controller with the ability to ride through faults in the grid was proposed in [13]. In [14], a control strategy for LCL-filtered inverters was developed for weak grids. The proposed design method can guarantee the inverter stability and robustness simultaneously without needing any compensation network, additional hardware, or the complicated iterative computations that cannot be avoided for the conventional inverter design method.

Regarding controllers for a single-phase LCL-filtered grid-connected inverter, the most dominant is the PR. A PR controller with disturbance rejection was proposed in [15]. The paper uses some state observers, which may not be highly accurate in case of uncertainties. On the other hand, [16,17] presented an optimized method for design current controllers. One drawback of grey wolf optimizer and the state current observe controller methods is the necessity of a sophisticated algorithm leading to use of a relatively low sampling frequency. The PI controller is sometimes employed in a single-phase system. Even knowing that the PI is unable to follow sinusoidal references without null error, its usage is sometimes justified because the PI is designed to present a low and acceptable steady-state error. The procedure for tuning a PI, in this case, can be found in [4]. In [18] the mathematical model of the grid-connected inverter was investigated. Then, its linearized small-signal state-space model was obtained, and a linear quadratic regulator was achieved by the solution of algebraic Riccati equation while in [19] an adaptive control of LCL-filtered with time-varying parameters using reinforcement learning was proposed.

Attempts to use three-phase control strategies in single-phase are also found in the literature. The idea behind that is to preserve the features and simplicity of three-phase in single-phase systems. In this case, simplified controllers can be adopted to make the output current follow its reference signal with negligible steady-state error. The use of PI is largely used. The books [3,9] describe the procedure for designing single-phase current controllers using three-phase approaches. However, the performance of the controller is very dependent on the Phase-Locked Loop (PLL) performance, and there is an effect of axis coupling. In [20,21], the authors proposed a decoupled technique to the direct-quadrature (*dq*)-reference frame in a single-phase system. The efficacy of the proposal was demonstrated, but it brings complexity to the control strategy and dependence of other functions.

The dynamic characteristics of the LCL filter in DC-DC or DC-AC converter are the same. The differences fall in the nature of currents and voltages across the LCL and in the manner how the

elements are charged and discharged. In DC-DC converters, the current through the inductors is DC, having finite, non-null value and ripple. In this context, the LCL elements are analyzed using concepts of DC circuits. Inductors are charged and discharged with positive current, but interchanging the sign of the derivative of the current.

The LCL of DC-AC converters handles AC current and voltage. In this case, the average value of current and voltage is zero. Therefore, the charge and discharge of the LCL elements happens naturally during the cycles of the AC variables. From the point of view of the current controller, the dynamic characteristic of the LCL must be modeled in order to make the most suited controller. Since the controlled current is AC, the controller needs to have high accuracy.

1.2. Novelties and Goals

All the previously mentioned research has their efficacy and legitimacy. However, new issues can be addressed. The integral single-lead and integral double-lead controllers are familiar topics in the literature. However, these controllers were employed only to DC-DC converters and, in most cases, the approach is in the continuous-time domain. The dynamic behavior of the LCL-filtered inverter is entirely different from the dynamic behavior of DC-DC converters, requiring special care in tuning the controllers. In this context, the use of the controllers mentioned above was not properly investigated in the literature for applications in LCL-filtered grid-connected inverters.

This paper brings to the state of the art about controlling single-phase grid-connected inverters a proper design procedure for tuning the integral single-lead and integral double-lead controllers considering the dynamic behavior of the LCL-filtered inverter. These controllers are different from the traditional PI, PD, and PID. To enhance accuracy, there is also a proposal of a tuning procedure taking into account the PWM delay effect on the integral double-lead controller. Finally, a digital PR controller was also proposed. The proposed PR has a different and simpler tuning methodology then those procedures commonly found in the literature. While conventional procedures for PR controllers in the literature deal with complex and trigonometric equations, the proposed procedure for the PR controller is simpler and straightforward. The step-by-step procedure for computing each parameter of the four proposed digital current controller is carefully presented. The proposed controllers can be applied to LCL-filtered inverters with passive and active resonance damping.

Some advantages of the proposed controllers are: It does not need to know the grid impedance for their designing, there is no need for voltage feedforward action, it does not need variable transformation as found in alpha-beta and *dq*-reference frames, it works in a satisfactory manner in weak grids and voltage with harmonic distortions, it is not dependent on the performance of a PLL, it takes into account the current sensor gain, it can be used in three-phase *abc*-reference frame control strategies, and it can be employed for active and passive damping-based LCL filters.

The controllers covered in this paper are defined as highly accurate digital current controllers. The reason for such a definition is because there is an equation for each parameter of the controllers. No one parameter is computed by trial-and-error or empirical methods. Moreover, for digital implementation, the coefficients of the controllers were programmed with 11 decimal places. This results in highly accurate digital controllers.

Therefore, this paper contributes to presenting an attractive guide for a fast, accurate, and reliable procedure for tuning digital current controllers for a single-phase LCL-filtered grid-connected inverter.

2. Single-Phase LCL-Filtered Grid-Connected Inverter

Figure 1 presents the LCL-filtered inverter connected to a single-phase power distribution grid. The inverter is made by a half-bridge converter with two DC sources. Nevertheless, all the content of this paper is also valid for a full-bridge converter with one DC source, as indicated in the figure. The DC sources represent the PV system plus a DC-DC converter. For the sake of verification of the proposed controllers, the DC sources will be assumed with fixed value and also with a fixed-plus-10% of oscillation. The LCL components have the letters *c*, *g*, *f*, and *d* as subscripts, meaning converter-side,

grid-side, filter, and damping, respectively. The LCL has a passive damping action, even though the content of this paper is also valid for active damping action based on capacitor current feedback. The LCL-filtered inverter is connected to the point of common coupling (PCC). The grid-side inductor current and the PCC voltage are measured and sent to the digital control strategy. The PCC voltage is used only to generate a synchronized current reference signal while the grid-side inductor current is used as feedback to the controller. The block of the digital controller is a simplification of the control strategy, having the Analog to Digital Converter (ADC), Zero-Order Holder (ZOH), PWM, and the proposed controllers. The electric grid has a line impedance, represented by L_s and R_s. The relation of $R_s \gg X_{Ls}$ is preserved since this is commonly found in residential power distribution grids. The values of them are not necessary for tuning the proposed controllers.
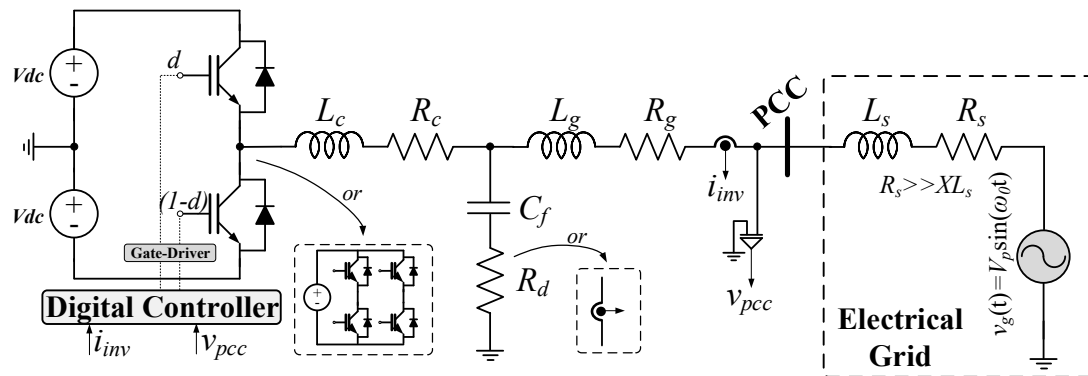
Figure 1. Simplified diagram of the single-phase LCL-filtered grid-connected inverter.

The DC sources in Figure 1 may also represent other sources instead of a PV system with DC-DC converter. They may represent batteries or a DC link of back-to-back converter. For such cases, a bidirectional power flow is usually required. The procedures for tuning the digital current controllers are also valid when there is a need of bidirectional power flow. As will be observed later, the controllers are able to make the output current follow sinusoidal reference with negligible steady-state error. The direction of power, i.e., from the grid or to the grid, is dependent on the phase displacement of the current reference signal with the PCC voltage. For a power flow from the DC sources to the grid, the phase displacement is null. For a power flow from the grid to the DC sources, the phase displacement is 180°. In both cases, the reference is sinusoidal. Therefore, the controllers are able to handle bidirectional power flow.

3. Highly Accurate Digital Current Controllers

Figure 2 presents a simplified diagram of the control strategy. The larger rectangle shows the digital environment. The inverter output current and the PCC voltage are measured through sensors and sent to the Digital Signal Controller (DSC) via a conditioning circuit (not shown). The DSC has an ADC with a sampler and zero-order holder (ZOH). The PCC voltage passes in a PLL [22,23] to generate a synchronized reference signal. The reference is compared to the inverter output current. The result is the error signal, which in turn is applied to the current controller $C_i(z)$. The figure shows that the current controller can be one of the highly accurate controllers proposed in this paper. The PWM interfaces the DSC and the LCL-filtered inverter. Note that both the PWM and LCL-filtered inverter are described by transfer functions in *s*-domain. This is necessary to properly design the digital current, as explained in the following.
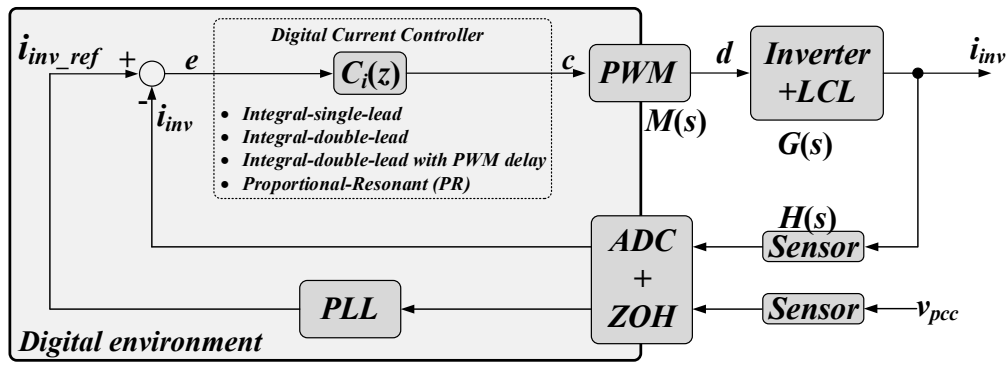
Figure 2. Simplified diagram of the control strategy.

The PLL used in the control strategy deservers special attention. Its purpose is only to generate a clean sinusoidal signal, synchronized with the PCC voltage. Such a signal is used as reference to the output current of the LCL-filtered inverter. The performance of the four digital current controllers shown in Figure 2 is independent of the performance of the PLL. Taking as example control strategies running in dq-rotating reference frame [24], if the PLL fails to be accurately synchronized with the PCC voltage, the control strategy will not perform as expected because the reference frame will not be correct. As a result, the inverter output current may present a highly distorted waveform and the whole system may become unstable. In the proposed controllers, if the PLL fails to be accurately synchronized with the PCC voltage, the inverter output current keeps following the reference signal, even though it may exist a short phase displacement between the output current and the PCC voltage. Obviously, this is not a desired situation. To overcome that, the PLL must assure the generation of a clean and synchronized reference signal even under distorted voltage grid.

Independently of what kind of controller is employed in the control strategy, tuning the parameters may be performed in a variety of manners. Figure 3 shows a chart of the most traditional methods for tuning a digital controller. Starting from the system modeling in *s*-domain, the designer can choose between two paths: (i) apply the Z-transform in the *s*-domain model, getting the *z*-domain model. In this approach, the effect of the ZOH is taken into account. Then, the current controller can be tuned through pole placement [25], state-feedback [26,27], and through conventional methods using the fictitious *w*-plane [28]. These methods, even though very mature and broadly adopted, have some drawbacks. The pole placement method is not trivial because the designer must define the location of the poles in the closed-loop system. The state-feedback method requires the measurement of several variables and its performance is deteriorated under parameter variations. The conventional methods through *w*-plane require several domain transformations, leading to inaccuracy. On the other hand, the designer can choose the path (ii). By choosing that, the controller is designed in *s*-domain, and later it is discretized, reaching the digital controller. For the majority of applications, this method results in an accurate controller up to the Nyquist frequency. Throughout this paper, path (ii) is adopted. The designed current controllers will be plotted with their equivalent *s*-domain controllers to show the accuracy of them. Moreover, the choice for path (ii) justifies the definition of the PWM in *s*-domain as shown in Figure 2.
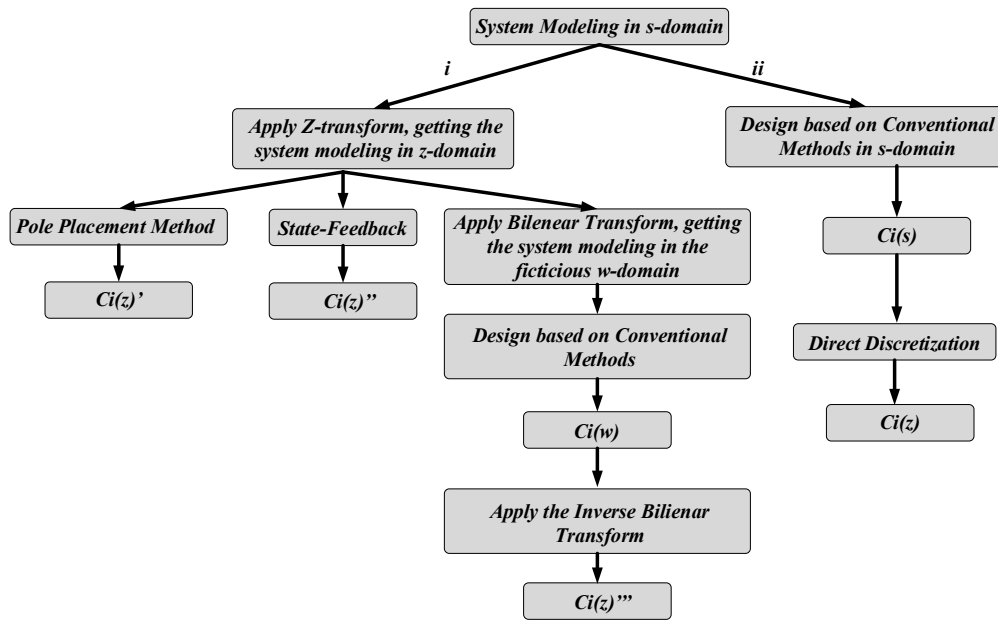
Figure 3. Techniques for tuning a digital controller.

3.1. System Modeling in s-Domain

The dynamic model of the LCL-filtered grid-connected inverter is commonly found in the literature. Its obtaining procedures as well as the dimensioning of the LCL components are beyond the scope of this paper, but are found in [24,29,30]. The transfer function that relates the grid-side current i_{inv} and the inverter duty-cycle d is defined as $G(s)$ and given by

$$G(s) = \frac{i_{inv}(s)}{d(s)} = K_{inv} \frac{sC_f R_d + 1}{s^3 L_g L_c C_f + s^2 C_f R_d (L_c + L_g) + s(L_c + L_g)} \tag{1}$$

where K_{inv} is the inverter gain, defined as:

$$K_{inv} = 2V_{dc} \tag{2}$$

The previous equations are valid for the LCL filter with passive damping, as shown in Figure 1. For the case where active damping with capacitor current feedback is employed, the transfer function that relates the grid-side current i_{inv} and the inverter duty-cycle d is [4]:

$$G_{ad}(s) = \frac{i_{inv}(s)}{d(s)} = K_{inv} \frac{1}{s^3 L_g L_c C_f + s^2 \frac{C_f L_g K_{inv}}{k_a} + s(L_c + L_g)} \tag{3}$$

where k_a is the coefficient gain of the active damping action. Throughout this paper, Equation (1) is adopted for tuning the proposed, highly accurate digital current controllers. Nevertheless, Equation (3) could be used as well. The elements R_c and R_g were neglected in (2) and (3) because their effects in the dynamic characteristic of the LCL filter are almost null. Their values can be approximated to zero without loss of generalities. Neglecting R_c and R_g is a common practice in LCL applications, as observed in [29–31].

The transfer function of the PWM without considering the effect of its delay is given by:

$$M(s) = \frac{1}{2c_k} \tag{4}$$

where c_k is the amplitude of the carrier signal. The numeral 2 in the denominator is due to the double-update method used in the PWM [25].

The transfer function of the PWM, taking into account the effect of its delay, is given by the Pade's approximation as [32]:

$$M_{delay}(s) = -\frac{1}{2c_k}\frac{s - \frac{2}{t_d}}{s + \frac{2}{t_d}} \qquad (5)$$

Note a minus signal in front of the equation. The variable t_d is the PWM delay, given by:

$$t_d = \frac{1}{1.5f_s} \qquad (6)$$

where f_s is the sampling frequency. In this case, the switching frequency is equal to the sampling frequency. The choice of the sampling frequency must respect the Nyquist criteria in order to avoid the aliasing effect [28] and must be sufficiently high to allow the computation of all required calculus for a proper operation of the control strategy. Assuring that will avoid losing switching periods. Regarding the switching frequency, the choice of its value usually depends on the technologies of the employed semiconductors and on passive components volume requirements. The procedures proposed here are valid for any kind of transistor technologies and for any value of switching frequency.

The value of 1.5 that appears in (6) is due the natural one-sample delay of digital applications summed with half-sample of the computational time needed to run the control strategy. The value of 1.5 is largely adopted in control strategies when the delay is modeled [3]. Other values may be used as 1 or 2, depending on the design specifications. In this paper, the value 1.5 is enough for taking into account all the delays presented in the system.

The current sensor is modeled with a transfer function in *s*-domain. Its definition is just the sensor gain H_i, given by:

$$H(s) = H_i \qquad (7)$$

According to Figure 2, the open-loop transfer function (OLTF) without considering the current controller is given by:

$$OLTF_u(s) = G(s)M(s)H(s) \qquad (8)$$

The subscript *u* means uncontrolled. It is essential to highlight that $G(s)$ may be replaced by $G_{ad}(s)$ and $M(s)$ for $M_{delay}(s)$ depending on the system configuration and the interest in considering the effect of the PWM delay.

For the sake of comparison, Figure 4 presents the Bode diagrams of the transfer function that relates to the grid-side current i_{inv} and the inverter duty-cycle d considering passive and active damping. In this case, the switching frequency is 10 kHz and the value for K_a is 0.55. The figure shows a region of interest, which is from approximately 1.5 kHz and below. Such a region is the region where the controller acts, taking into account that the desired cutoff frequency for the system should be from 8 to 10 times lower than the switching frequency [33]. The curves are almost coincident for the magnitude, while there is a slight difference in the phase curves. This justifies that the proposed controllers presented in the next sections are useful for both methods of LCL damping, the passive and active. Considering the active damping method will require a more significant phase advance in the controller, the proximity of these curves also depends on K_a factor.
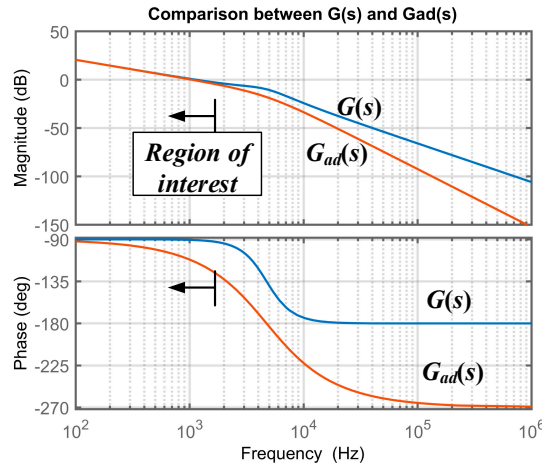
Figure 4. Comparison of the transfer functions that relates to the grid-side current i_{inv} and the inverter duty-cycle d considering passive and active damping.

The procedures presented in the following sections are independent of each other. Even though they have coefficients named equally, they are not directly related. In other words, the coefficient R_1 in the integral single-lead controller is not the same as the coefficient R_1 in the integral double-lead controller. This is also valid for all variables that appear in the procedures. The choice of using the name of the same coefficients in different controllers is to keep the method as simple as possible. Additionally, the procedures proposed in this paper may serve as a guide for tuning current controllers. The reader can follow only the procedure of the controller that best fits his or her goals.

3.2. Tuning the Integral Single-Lead Digital Current Controller

The integral single-lead controller has a pole at the origin and a single pole–zero pair. The pole at the origin is an integral part of the controller, while the pole–zero pair is responsible for leading the phase [32]. Throughout this paper, this controller will be called C_{i_sl}. Its transfer function in *s*-domain is given by:

$$C_{i\_sl}(s) = \frac{1 + sR_2C_1}{sR_1(C_1 + C_2 + sR_2C_1C_2)} \tag{9}$$

The procedure for tuning the integral single-lead controller starts with the definition of the desired cutoff frequency (f_c), in Hz, and the desired phase margin (MF_d), in degree. The most recommended definition of the cutoff frequency is to pick a value that is 8 to 15 times lower than the switching frequency, while the phase margin is any value from 30 to 90°. With that defined, the next step is to get the value of the phase at the desired cutoff frequency in the uncontrolled OLTF. This is expressed as:

$$\varphi_{sl} = \angle OLTF_u(f_c) \ [deg] \tag{10}$$

Similarly, the value of the gain at the desired cutoff frequency in the uncontrolled OLTF is given by:

$$G_{sl\_dB} = \left| OLTF_u(f_c) \right| \ [dB] \tag{11}$$

The gain at the desired frequency obtained in the previous equation is in dB and must be converted into real value. This is performed by:

$$G_{sl} = 10^{\frac{|G_{sl\_dB}|}{20}} \tag{12}$$

To better visualize where φ_{sl} is located in a Bode diagram, Figure 5 shows a generic Bode diagram indicating the points for the desired cutoff frequency, the phase φ_{sl}, and gain G_{sl} at the desired cutoff frequency. This Bode diagram is just for illustration and has nothing to do with the system covered in this paper.
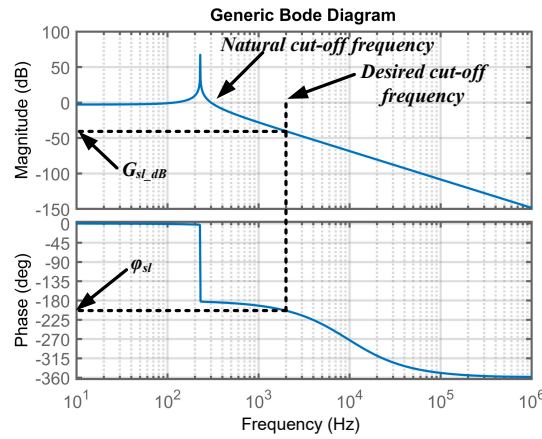
Figure 5. Bode diagram indicating the points for phase φ_{sl} and the gain G_{sl} at the desired cutoff frequency.

The phase that the integral single-lead controller must lead is given by:

$$\alpha = MF_d - \varphi_{sl} - 90° \ [deg] \tag{13}$$

The 90° in the equation is due to the phase delay caused by the controller itself [32]. The maximum phase that the integral single-lead controller is able to lead is 90°, as will be shown later. In case there is a need for lead more than 90°, the integral double-lead controller should be used.

The next step is to compute the *K*-factor using [34]:

$$K_{sl} = tan\left(\frac{\alpha}{2} + 45°\right) \tag{14}$$

At this point, it is convenient to define the following constant:

$$C_{sl} = \frac{1}{2\pi f_c G_{sl} K_{sl}} \tag{15}$$

In this way, the parameters of the current controller in *s*-domain are given by the following equations:

$$C_2 = must \ be \ defined \ (100n \ for \ example) \tag{16}$$

$$R_1 = \frac{C_{sl}}{C_2} \tag{17}$$

$$C_1 = C_2\left(K_{sl}^2 - 1\right) \tag{18}$$

$$R_2 = \frac{K_{sl}}{2\pi f_c C_1} \tag{19}$$

By computing the four previous equations, the integral single-lead current controller in the *s*-domain is finally tuned. Before discretizing the controller, it is necessary to check if the desired cutoff frequency and phase margin were obtained. To do that, the OLTF considering the designed controller is given by:

$$OLTF_{c\_sl}(s) = C_{i\_sl}(s)OLTF_u(s) = C_{i\_sl}(s)G(s)M(s)H(s) \tag{20}$$

The subscript *c* means controlled.

The closed-loop transfer function (CLTF) is given by:

$$CLTF_{sl}(s) = \frac{OLTF_{c\_sl}(s)}{OLTF_{c\_sl}(s) + 1} \tag{21}$$

Since the cutoff and the phase margin are in accordance with that desired values, the controller is discretized. The integral single-lead current controller is discretized through the backward Euler approximation [28], given by:

$$C_{i\_sl}(z) = C_{i\_sl}(s)\big|_{s=\frac{1-z^{-1}}{T_s}} \tag{22}$$

where T_s is the sampling period. The result of the previous equation is the digital current controller whose transfer function is given by:

$$C_{i\_sl}(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \tag{23}$$

The following equations give the coefficients of the digital current controller:

$$\beta_{sl} = 4R_1 R_2 C_1 C_2 + 2T_s R_1 (C1 + C2) \tag{24}$$

$$b_0 = \frac{T_s^2 + 2T_s C_1 R_2}{\beta_{sl}} \tag{25}$$

$$b_1 = \frac{2T_s^2}{\beta_{sl}} \tag{26}$$

$$b_2 = \frac{T_s^2 - 2T_s C_1 R_2}{\beta_{sl}} \tag{27}$$

$$a_0 = 1 \tag{28}$$

$$a_1 = \frac{-8R_1 R_2 C_1 C_2}{\beta_{sl}} \tag{29}$$

$$a_2 = \frac{4R_1 R_2 C_1 C_2 - 2T_s R_1 (C1 + C2)}{\beta_{sl}} \tag{30}$$

This ends the tuning procedure for the integral single-lead digital current controller.

3.3. Tuning the Integral Double-Lead Digital Current Controller

The integral double-lead controller has a pole at the origin and two pairs of zero–pole. This controller can lead the phase twice higher than the integral single-lead controller. Throughout this paper, the integral double-lead controller will be called C_{i_dl}. Its transfer function in *s*-domain is given by:

$$C_{i\_dl}(s) = \frac{s^2 R_2 C_1 C_3 (R_1 + R_3) + s(R_2 C_1 + R_1 C_3 + R_3 C_3) + 1}{s^3 R_1 R_2 R_3 C_1 C_2 C_3 + s^2 [R_1 R_3 C_3 (C_1 + C_2) + R_1 R_2 C_1 C_2] + s R_1 (C_1 + C_2)} \tag{31}$$

The procedure for tuning the integral double-lead controller also starts with the definition of the desired cutoff frequency (f_c), in Hz, and the desired phase margin (MF_d), in degrees. For convenience, the desired cutoff frequency and phase margin will be the same as from the previous. As a result, the names of these variables are preserved.

The next step is to get the value of the phase at the desired cutoff frequency in the uncontrolled OLTF, expressed as:

$$\varphi_{dl} = \angle OLTF_u(f_c) \ [deg] \tag{32}$$

In a similar way, the value of the gain at the desired cutoff frequency in the uncontrolled OLTF is given by:

$$G_{dl\_dB} = \left| OLTF_u(f_c) \right| \ [dB] \tag{33}$$

The gain at the desired frequency obtained in the previous equation is in dB and must be converted into real value. This is performed by:

$$G_{dl} = 10^{\frac{|G_{dl\_dB}|}{20}} \tag{34}$$

Note that the previous three equations are the same for the integral single-lead controller. It is worth highlighting that in case the phase to be led can be obtained by using the integral single-lead controller (lower than 90°), the use of the integral double-lead controller is unnecessary.

The *K*-factor for the integral double-lead controller is given by:

$$K_{dl} = \left[tan\left(\frac{\alpha}{4} + 45° \right) \right]^2 \tag{35}$$

The value of α is the same as previously computed. Notice that the K-factor for this controller is different from the previous one. The parameters of the current controller in *s*-domain are given by the following equations:

$$R_1 = must\ be\ defined\ (1000\ for\ example) \tag{36}$$

$$C_2 = \frac{1}{2\pi f_c G_{dl} R_1} \tag{37}$$

$$C_1 = C_2(K_{dl} - 1) \tag{38}$$

$$R_2 = \frac{\sqrt{K_{dl}}}{2\pi f_c C_1} \tag{39}$$

$$R_3 = \frac{R_1}{K_{dl} - 1} \tag{40}$$

$$C_3 = \frac{1}{2\pi f_c R_3 \sqrt{K_{dl}}} \tag{41}$$

The integral double-lead current controller in the *s*-domain is finally tuned. The OLTF considering the designed controller is given by:

$$OLTF_{c\_dl}(s) = C_{i\_dl}(s)OLTF_u(s) = C_{i\_dl}(s)G(s)M(s)H(s) \tag{42}$$

The closed-loop transfer function (CLTF) is given by:

$$CLTF_{dl}(s) = \frac{OLTF_{c\_dl}(s)}{OLTF_{c\_dl}(s) + 1} \tag{43}$$

Since the cutoff and the phase margin are in accordance with the desired values, the controller is discretized. The integral double-lead current controller is also discretized through the backward Euler approximation [28], given by:

$$C_{i\_dl}(z) = C_{i\_dl}(s)\Big|_{s = \frac{1-z^{-1}}{T_s}} \tag{44}$$

The result of the previous equation is the digital current controller whose transfer function is given by:

$$C_{i\_dl}(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3}}{a_0 + a_1 z^{-1} + a_2 z^{-2} + a_3 z^{-2}} \tag{45}$$

The coefficients of the digital current controller are given by the following equations, together with the definition of five constants, D_1 to D_5:

$$D_1 = R_2 C_1 C_3 (R_1 + R_3) \tag{46}$$

$$D_2 = R_2 C_1 + R_1 C_3 + R_3 C_3 \tag{47}$$

$$D_3 = R_1 R_2 R_3 C_1 C_2 C_3 \tag{48}$$

$$D_4 = R_1 R_3 C_1 (C_1 + C_2) + R_1 R_2 C_1 C_2 \tag{49}$$

$$D_5 = R_1 (C_1 + C_2) \tag{50}$$

$$\beta_{dl} = D_3 + D_4 T_s + D_5 T_s{}^2 \tag{51}$$

$$b_0 = \frac{T_s D_1 + D_2 T_s{}^2 + T_s{}^3}{\beta_{dl}} \tag{52}$$

$$b_1 = -\frac{2 T_s D_1 + D_2 T_s{}^2}{\beta_{dl}} \tag{53}$$

$$b_2 = \frac{T_s D_1}{\beta_{dl}} \tag{54}$$

$$b_3 = 0 \tag{55}$$

$$a_0 = 1 \tag{56}$$

$$a_1 = -\frac{3 D_3 + 2 D_4 T_s + D_5 T_s{}^2}{\beta_{dl}} \tag{57}$$

$$a_2 = \frac{3 D_3 + D_4 T_s}{\beta_{dl}} \tag{58}$$

$$a_3 = -\frac{D_3}{\beta_{dl}} \tag{59}$$

Effectively completing all procedures for the integral double-lead digital current controller, the next section will continue with further recommendations. However, it is necessary to take special view on the lead phase that the integral single-lead and integral double-lead controllers can employ. Figure 6 shows the relation between lead phase versus the *K*-factor for both controllers. The integral single-lead controller can lead the phase at most 90°, as previously mentioned. As observed, increasing the K-factor from 50 and beyond will not result in an increase in the lead phase. On the other hand, the integral double-lead controller has its maximum lead phase at 180°. This chart is useful because depending on the value the designer computes for α in the previous procedures will define what controller can or must be used.
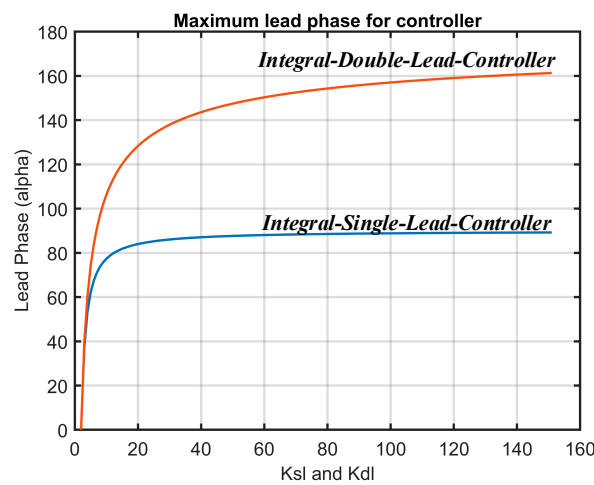
Figure 6. Relation between lead phase versus the *K*-factor for the integral single-lead and integral double lead controllers.

3.4. Tuning the Integral Double-Lead Digital Current Controller Considering the PWM Delay Effect

The two previous controller tuning procedures neglected the effect of the PWM delay. Neglecting such effect is quite acceptable in designing current controllers for LCL-filtered grid-connected inverters, since the switching frequency is usually high and the time constant of the controller is relatively low. However, one may desire to take into account the effect of PWM delay on the procedure for tuning the controller. This section presents the tuning procedure for the integral double-lead digital current controller considering the PWM delay effect. As will be observed later, the consideration of the PWM delay effect does not cause any change in the magnitude curve of the OLTF, but it modifies the phase curve.

In this context, the transfer function of the PWM is presented in Equation (5) and repeated here for simplicity.

$$M_{delay}(s) = -\frac{1}{2c_k}\frac{s - \frac{2}{t_d}}{s + \frac{2}{t_d}} \tag{60}$$

The OLTF without considering the current controller is passes to be:

$$OLTF_u(s) = G(s)M_{delay}(s)H(s) \tag{61}$$

From now on, the procedure for tuning the integral double-lead digital current controller is the same as the previous one and will be omitted here, paying attention that the previous equation takes over.

In the end, the transfer function of the designed controller is given by the following equation, paying attention that the coefficients here are different from the previous ones, even though they are named equally.

$$C_{i\_dl\_delay}(z) = \frac{b_0 + b_1z^{-1} + b_2z^{-2} + b_3z^{-3}}{a_0 + a_1z^{-1} + a_2z^{-2} + a_3z^{-2}} \tag{62}$$

For the sake of illustration, Figure 7 presents the OLTF for both considering and not considering the effect of the PWM delay. The magnitude curves are coincident, as expected. The phase curves are slightly different for the region of interest. The controller must lead to a higher phase when taking into account the PWM delay. Such an increase in the value of the phase to be driven is to compensate for the PWM delay.
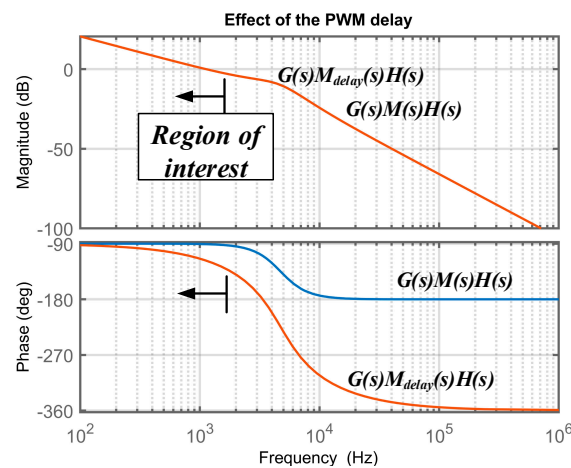

Figure 7. OLTF for both considering and not considering the effect of the PWM delay.

3.5. Tuning the Digital Proportional-Resonant Controller

The three previous digital controllers were implemented by a digital filter, defined by a *z*-domain transfer function. This means that the digital current controller $C_i(z)$ shown in Figure 2 can be one of the

following controllers: $C_{i\_sl}(z)$, $C_{i\_dl}(z)$, or $C_{i\_dl\_delay}(z)$. The implementation of the digital PR controller is different. Figure 8 show the block diagram of how the digital PR controller is implemented [5]. The PR controller is made by a proportional gain (k_p), a resonant gain (k_i) and a digital resonant filter, which in the z-domain transfer function is named $H_r(z)$.
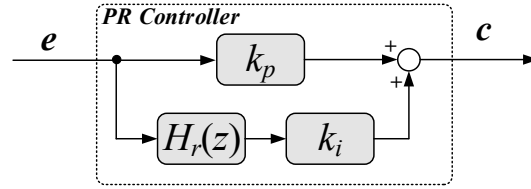
Figure 8. Block diagram of how the digital PR controller is implemented.

The procedure for tuning the digital PR controller consists of obtaining the proportional and resonant gain, as well as the coefficients of the digital resonant filter. The procedure proposed in this paper differs from those commonly found in the literature. There, the proportion and resonant gains are computed using nontrivial trigonometric functions [4]. Here, the procedure is more simplified and accurate.

The first step is to define the desired parameters of the PR controller. They are:

- Desired resonant frequency in Hz and rad/s, named f_r and $\omega_r = 2\pi f_r$, respectively. This frequency must be the grid frequency because the PR controller acts in the fundamental frequency for proper active power injection of the LCL-filtered grid-connected inverter.
- Damping factor, named ξ. Any value between 0.9 and 1 is a good choice.
- Desired bandwidth of the resonant filter in Hz and rad/s, named B_s And $B_r = 2\pi B_s$.
- Sampling frequency in Hertz and period in seconds, named f_s and T_s.

The proportional gain is obtained as [5,35]:

$$k_p = \frac{(2\xi + 1)\sqrt{(2\xi + 1)}\omega_r\left(L_g + L_c\right) - \left(R_g + R_c\right)}{\frac{V_{dc}}{2}H_i} \tag{63}$$

Notice that the current sensor gain is considered in computing the proportional gain. The resonant gain is obtained as:

$$k_i = \frac{\omega_r^2\left(L_g + L_c\right)\left[(2\xi + 1)^2 - 1\right]}{V_{dc}H_i} \tag{64}$$

The next step is to obtain the coefficients of the resonant filter $H_r(z)$. This is done by applying the Z-transform in its equivalent analog notch filter. The transfer function of an analog notch filter is given by:

$$H_r(s) = \frac{sB_r}{s^2 + 2sB_r + \omega_r^2} \tag{65}$$

Note that the above transfer function is defined in s-domain and it represents a non-ideal notch filter. By applying the Z-transform, it reaches the z-domain transfer function of the digital resonant filter, given by:

$$H_r(z) = \mathbb{Z}\{H_r(s)\} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{a_0 + a_1 z^{-1} + a_2 z^{-2}} \tag{66}$$

The coefficients are given by the following Equations, from (67) to (73).

$$\beta_{PR} = \frac{0.5B_r^2}{\sqrt{\omega_r^2 - 0.25B_r^2}}sin\left[\left(T_s\sqrt{\omega_r^2 - 0.25B_r^2}\right)\right]e^{-0.5B_rT_s} \tag{67}$$

$$b_0 = B_r T_s \tag{68}$$

$$b_1 = \left[-B_r e^{-0.5 B_r T_s} \cos\left(T_s \sqrt{\omega_r{}^2 - 0.25 B_r{}^2} \right) - \beta_{PR} \right] T_s \tag{69}$$

$$b_2 = 0 \tag{70}$$

$$a_0 = 1 \tag{71}$$

$$a_1 = -2 e^{-0.5 B_r T_s} \cos\left(T_s \sqrt{\omega_r{}^2 - 0.25 B_r{}^2} \right) \tag{72}$$

$$a_2 = e^{-B_r T_s} \tag{73}$$

By computing the previous equations, the tuning procedure for the digital PR controller is finished.

4. Case Study

This section presents a case study of tuning the integral single-lead, integral double-lead, integral double-lead considering the PWM delay effect and PR controllers based on the previous procedures. Table 1 shows the system parameters. The desired cutoff and the desired phase margin are listed at the end of the table.

Table 1. System parameters.

Parameter	Value	Unit
Grid Voltage	127	Vrms
Grid frequency	60	Hz
Converter-side inductor L_c	2.28	mH
Converter-side resistance R_c	0.01	Ω
Grid-side inductor L_g	990	uH
Grid-side resistance R_g	0.01	Ω
LCL capacitance C_f	1.64	uF
LCL damping resistance R_d	20.5	Ω
DC-link voltage V_{dc}	220	V
Grid resistance R_s	2	Ω
Grid inductance L_s	3	mH
Current sensor gain H_i	0.1	V/A
Switching frequency f_{sw}	10	kHz
Sampling period T_s	1×10^{-4}	s
Amplitude of the carrier c_k	1	V
Desired cut-off frequency f_c	1250	Hz
Desired phase margin MF_d	60	

Applying the values of Table 1 in the four procedures presented in Section 3 result in the designed digital current controller, whose final coefficients are listed in Table 2. The last column listed the coefficients of the digital resonant filter. The proportional and resonant gains are listed at the end of the table.

Figure 9 presents the frequency response of the designed digital current controllers. Note that the PR controller is written as $k_p + k_i H_r(z)$, which is the final transfer function of such a controller. At the desired cutoff frequency (1250 Hz) the controllers have similar behaviors, valid for magnitude and phase curves. This proves that the four covered types of controller are actually enough to control the output current of an LCL-filtered grid-connected inverter. The PR controller has a resonant peak at 60 Hz, showing that its design is accurate.

Table 2. Coefficients of the designed digital current controllers.

| Coefficient	$C_{i\_sl}(z)$	$C_{i\_dl}(z)$	$C_{i\_dl\_delay}(z)$	$H_r(z)$
b_0	0.72530697012	0.85193622372	0.82069570170	0.00094247779
b_1	0.13349036402	−1.17619397828	−1.23998086046	−0.0009418083
b_2	−0.59181660609	0.40596708885	0.46836864477	0
b_3	-	0	0	-
a_0	1.00000000000	1.00000000000	1.00000000000	1.00000000000
a_1	−0.79315175064	−1.8623848218	−1.75577338175	−1.99763758092
a_2	−0.20684824935	1.01692028896	0.84860413978	0.99905796619
a_3	-	−0.15453546714	−0.09283075802	-
k_p	-	-	-	0.55163792409
k_i	-	-	-	156.532858927
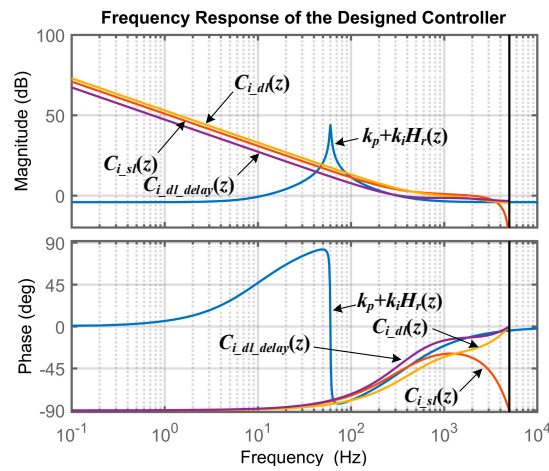
Figure 9. Frequency response of the designed digital current controllers.

Figure 10 presents the Bode diagrams of the designed current controller in the *s*-domain and *z*-domain. For all of them, the curves for magnitude and phase are almost coincident, especially at the desired cutoff frequency. This proves that the methodology of designing a digital controller based on conventional methods in *s*-domain and later applying a discretization technique is valid and highly accurate. For the PR controller, Figure 10d, only the comparison of the resonant filter is shown for better visualization. Figure 10d also shows that the gain is unitary (0 dB) only at 60 Hz. All other frequencies are attenuated. As a result, only the 60 Hz component will pass through this filter. Another point that deserves attention is that the phase is slightly different in the s and z domain. This means that the obtained phase margin is different from the desired one. However, such difference is minimal and does not invalidate the proposed tuning procedure.

(a) (b) (c) (d)
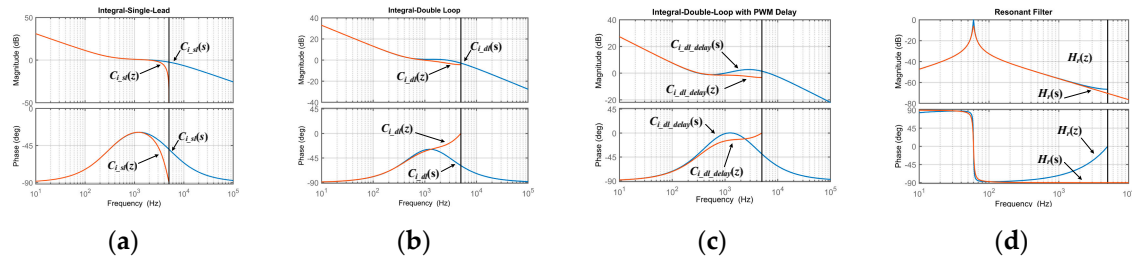
Figure 10. Bode diagrams of the designed current controller in *s*-domain and in *z*-domain: (**a**) Integral-single-lead, (**b**) integral double-loop, (**c**) integral double-loop considering the PWM delay effect, and (**d**) resonant filter.

It is important to highlight that in Figure 10 the three first controllers present high gain at 120 Hz. It means that they are able to minimize considerably the effect of the double-frequency pulsation commonly found in single-phase applications. For the PR controller, Figure 10d, and since its approach is to operate at 60 Hz, the ability to minimize such a pulsation is shown as a very low gain at 120 Hz. For the low-frequency region, the three first controllers present high gain. This is attractive because the steady-state error is inversely proportional to the gain at very low frequencies. For the last controller, the analysis of the steady-state error is different. For this case, the error can be computed at the tuned frequency. At the tuned frequency, the gain is 0 dB, which is 1 in real values. This means that the output variable is equal to 1 multiplied by the input. As a result, the output is equal to the input, as expected for component at the tuned frequency.

Figure 11 presents the Bode diagram for the closed-loop transfer function considering the designed current controllers. Note that the curves are for the closed-loop transfer function. The names of the controllers pointing at them are just in indication of what controller was used to plot such a curve. These diagrams are plotted in *s*-domain. Concerning the magnitude curves, the implementation of the proposed controllers makes the closed-loop system present similar behavior along the frequencies in the region of interest. For low frequencies, all of them present a gain of 0 dB, which makes the steady-state error to be null. At the cutoff frequency, the curves begin to fall. The curve for PR controller begins to fall first because its tuning procedure is different from the other controller regarding the definition of the desired cutoff frequency. In the phase curves, it is evident that all of them are stable and reached the desired phase margin. A zoom is presented for better visualization.
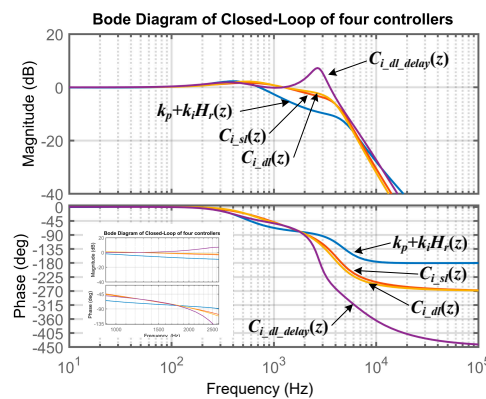

Figure 11. Bode diagram for the closed-loop transfer function considering the designed current controllers.

5. Hardware-in-Loop Experimental Verification

The control strategy presented in Figure 2 was experimentally verified in the DSC TMS320F28335 while the power structure was emulated in the HIL 402 device from Typhoon company. The digital current controller designed in Section 4 was implemented one by one. Results were collected using a desk oscilloscope. Figure 12 presents a diagram of the experimental and HIL verification as well as a picture of it. The HIL sends a signal of variables along the power structure to the DSC through the interface board. In this case, the signals that are sent are the inverter output current and the PCC voltage. The DSC runs the control strategy with the digital current controller and generates the PWM signal, which in turn acts in the HIL. The DSC is connected directly in the interface board. Once the HIL has fidelity to emulate power electronic systems in real time, the DSC receives, processes, and sends signal to the HIL in a similar way of real systems. Therefore, from the point of view of the DSC, the proposed, highly accurate digital current controllers for a LCL-filtered grid-connected inverter is verified experimentally. To visualize in the oscilloscope the reference signal, which is within the DSC, the digital-to-analog converter (DAC) of the interface board was used. The reference signal in the following results show some steps due to the DAC are buffer-type and the relation of the sampling frequency and the reference signal frequency is not an integer number. However, the reference signal

within the DSC is purely sinusoidal. This is verified in the inverter output waveforms presenting sinusoidal shape.
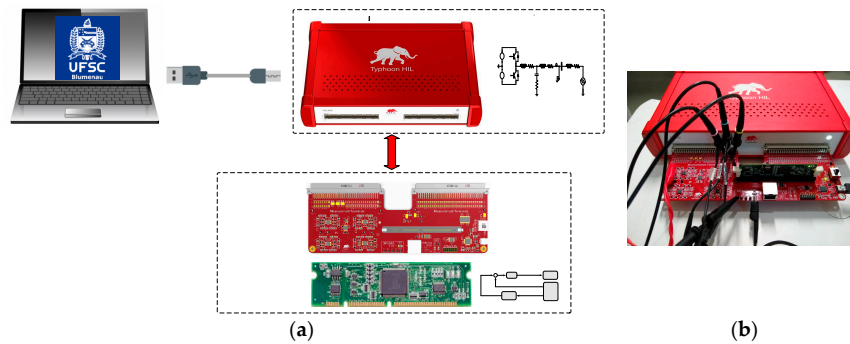

Figure 12. Experimental and HIL verification: (**a**) Simplified diagram (**b**) picture.

The interface board is needed to fit the signals that come from the HIL and go to the analog inputs of the DSC. The HIL delivers signal varying from −5 to 5 V while the DSC supports signals ranging from 0 to 3 V. Therefore, there was a need for programming, such as compensation in the DSC. The amplitude and offset compensation programmed into the DSC was not shown in Figure 2. Another gain adjustment was necessary before the digital current controller as $5C_i(z)$ for the integral single-lead, integral double-lead, and integral double-lead with PWM delay effect and as $5k_p$ for the PR controller. These amplitude, gain, and offset adjustments are just for implementation purpose and do not invalid the tuning procedures of the current controllers.

Figure 13 presents the PCC voltage, the inverter output current, and its reference signal for the four designed controllers during initializing. Initially, the reference is null. Later, the reference goes to its maximum value. Before and after the initialization, it is clear that the output current is following its reference with negligible steady-state error for all controllers. This shows the efficacy of the highly accurate, proposed controllers and their tuning procedures. During transitory behavior, the PR controller shows superior performance. Even though the integral single-lead and integral double-lead considering the PWM delay effect showed relative high overshoot, this could be minimized by imposing the reference at zero phase of the grid or making a slow ramp on its amplitude. To show the behavior of the controllers, the time of the reference step was applied randomly. Concerning the PCC voltage, its waveform is not purely sinusoidal, showing a typical power distribution voltage grid with $R_s \gg X_{LS}$. This is valid for before and after the initialization of the inverter. This is attractive because it shows the ability of the proposed controller to work in weak grids, which are the most severe for current controllers. Another point that deserves attention is that the controller designed without considering the PWM delay effect showed a satisfactory performance.
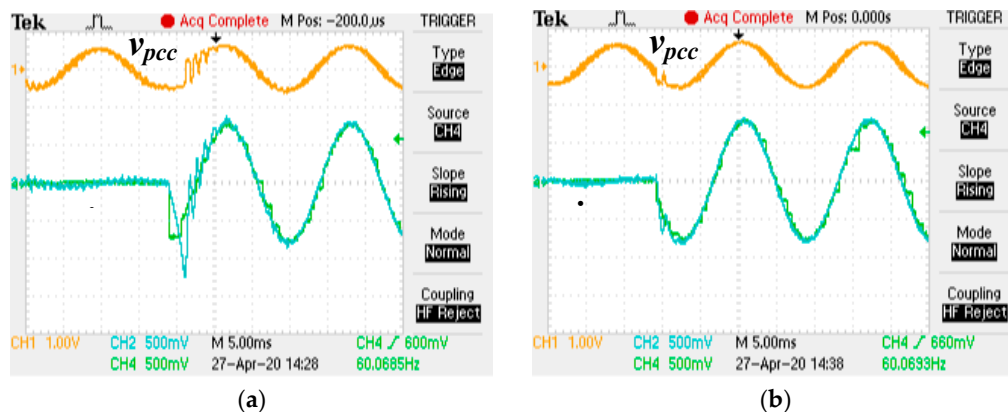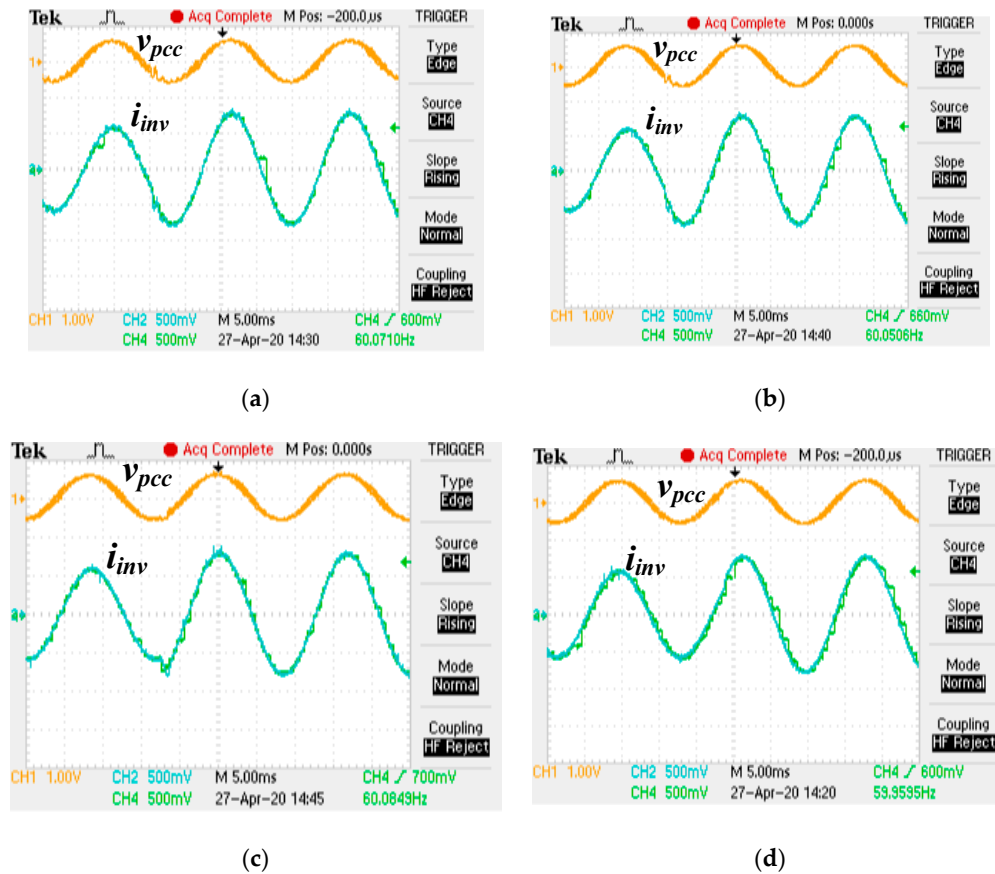

Figure 13. *Cont.*
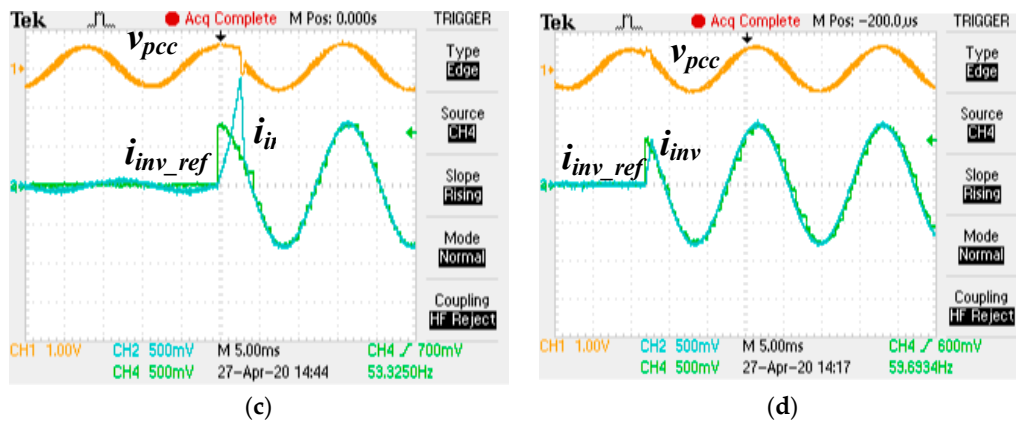
Figure 13. PCC voltage, the inverter output current, and its reference signal during initialization for: (**a**) Integral-single-lead controller, (**b**) integral double-lead controller, (**c**) integral double-lead controller considering the PWM delay effect, and (**d**) PR controller. (Ch1: 360 V/V; Ch2: Ch4: 20 A/V).

Figure 14 presents the PCC voltage, the inverter output current, and its reference signal during a step in the reference signal from 0.75 to 1 pu. All controllers showed accurate performance, not presenting overshot and oscillatory behavior.

Figure 14. PCC voltage, the inverter output current, and its reference signal during a step in the reference signal from 0.75 to 1 pu: (**a**) Integral-single-lead controller, (**b**) integral double-lead controller, (**c**) integral double-lead controller considering the PWM delay effect, and (**d**) PR controller. (Ch1: 360 V/V; Ch2: Ch4: 20 A/V).
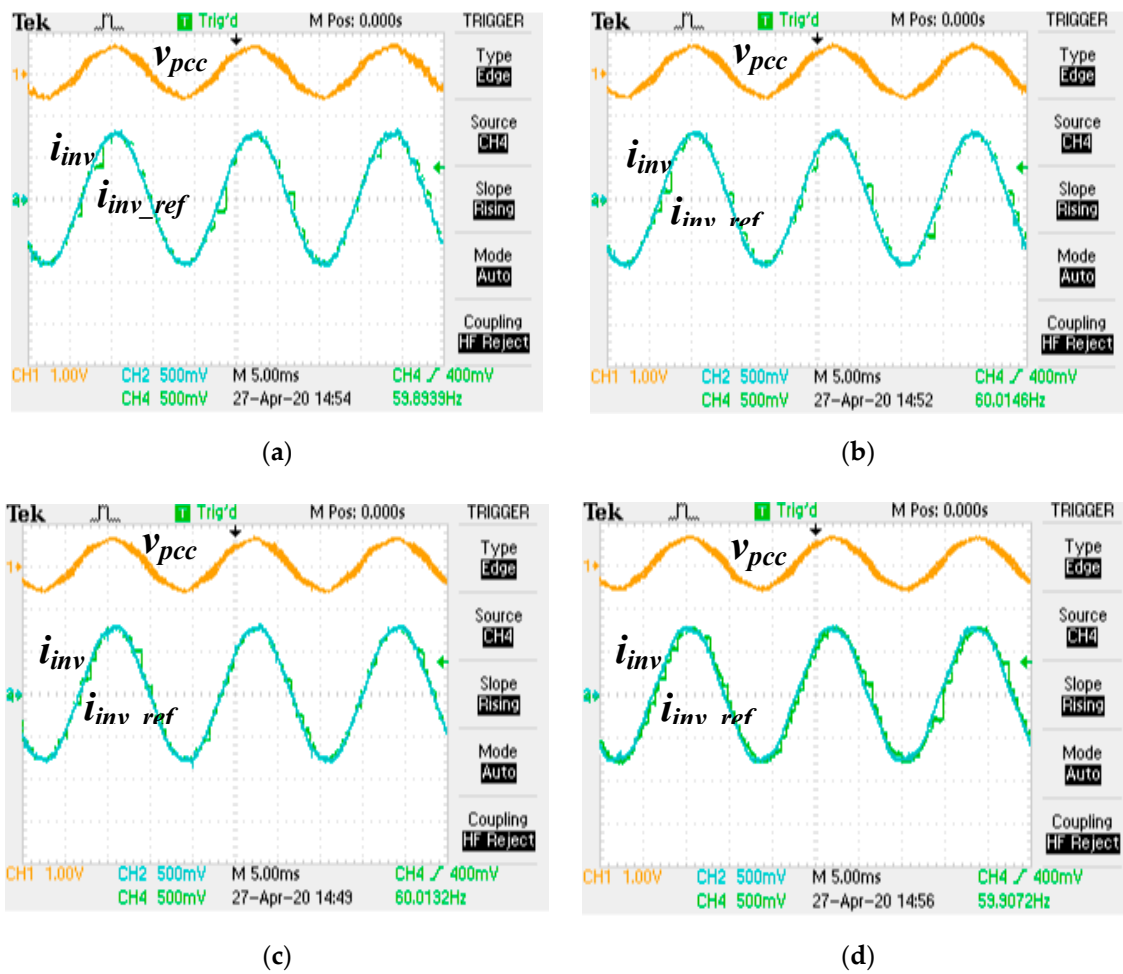
Figure 15 present the PCC voltage, the inverter output current, its reference signal, and the DC voltage during the inclusion of oscillation at the DC link. The oscillation has 10% of the DC voltage and 120 Hz. The output current keeps following its reference signal, as the oscillation was inexistent. This scenario may represent a malfunction in the PV plus DC-DC converter that is connected to the DC link of the LCL-filter inverter or the inevitable double-frequency pulsation in single-phase systems. Even in these cases, the results show the ability of the proposed controller to keep working accurately.
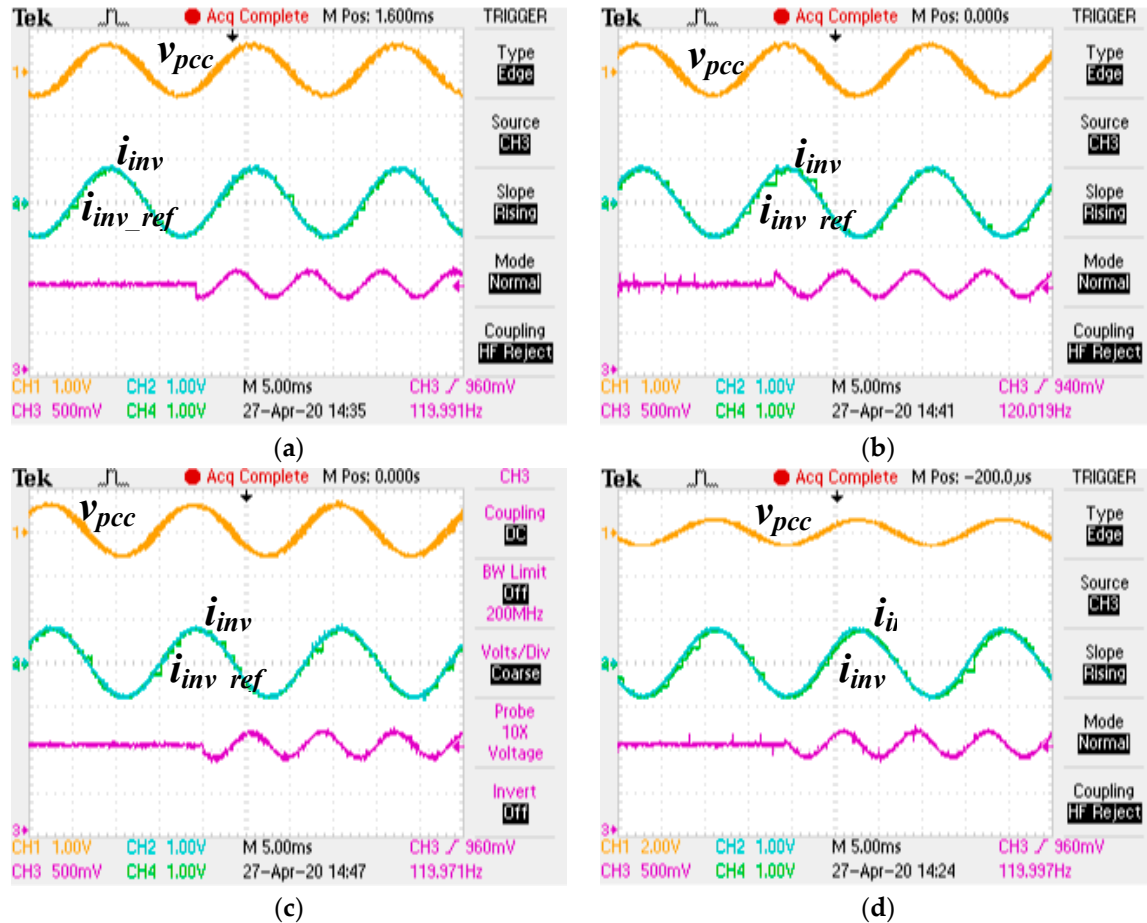
Figure 15. PCC voltage, the inverter output current, its reference signal, and the DC voltage during the inclusion of oscillation at the DC link: (**a**) Integral-single-lead controller, (**b**) integral double-lead controller, (**c**) integral double-lead controller considering the PWM delay effect, and (**d**) PR controller. (Ch1: 360 V/V; Ch2: Ch4: 20A/V; Ch3: 225 V/V).

The PCC voltage with harmonic distortion is more and more common in the power distribution system. Figure 16 shows the PCC voltage, the inverter output current, and its reference signal when the grid voltage has 5% related to the fundamental at the fifth harmonic. The controllers keep following their reference signal.

(a)

(b)

(c)

(d)

Figure 16. The PCC voltage, the inverter output current, and its reference signal when the grid voltage has 5% related to the fundamental at the fifth harmonic: (**a**) Integral-single-lead controller, (**b**) integral double-lead controller, (**c**) integral double-lead controller considering the PWM delay effect, and (**d**) PR controller. (Ch1: 360V/V; Ch2: Ch4: 20A/V).
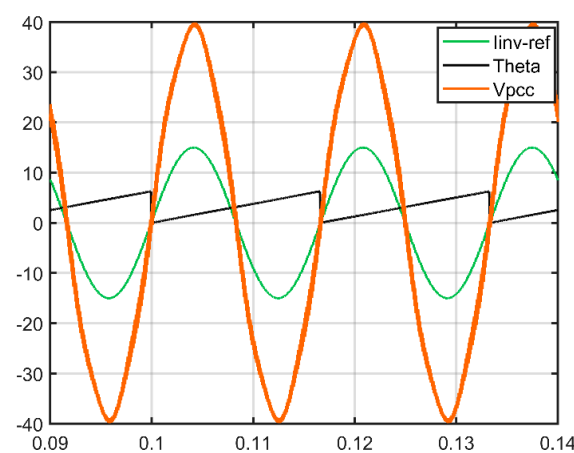
6. Discussion

This section discusses some relevant extra issues of the proposed research. The first is the evaluation of the controllers under bidirectional power flow. Figure 17 presents results when the reference signal for the output current changes its phase related to the PCC voltage. Initially, the current is sinusoidal and in phase with the PCC voltage. Then, the reference signal suffers a 180-degree phase shift. After the transitory interval, the output current returns to follow its reference with negligible steady-state error. Before the transition in the reference, the inverter was injecting active power into the grid. After, the inverter is consuming power from the grid. The inverter output current for the four controllers shows similar behavior as those found during initialization. No unpredictable behavior or instability was observed, indicating that the controllers designed using the proposed procedures were efficient for bidirectional power applications.
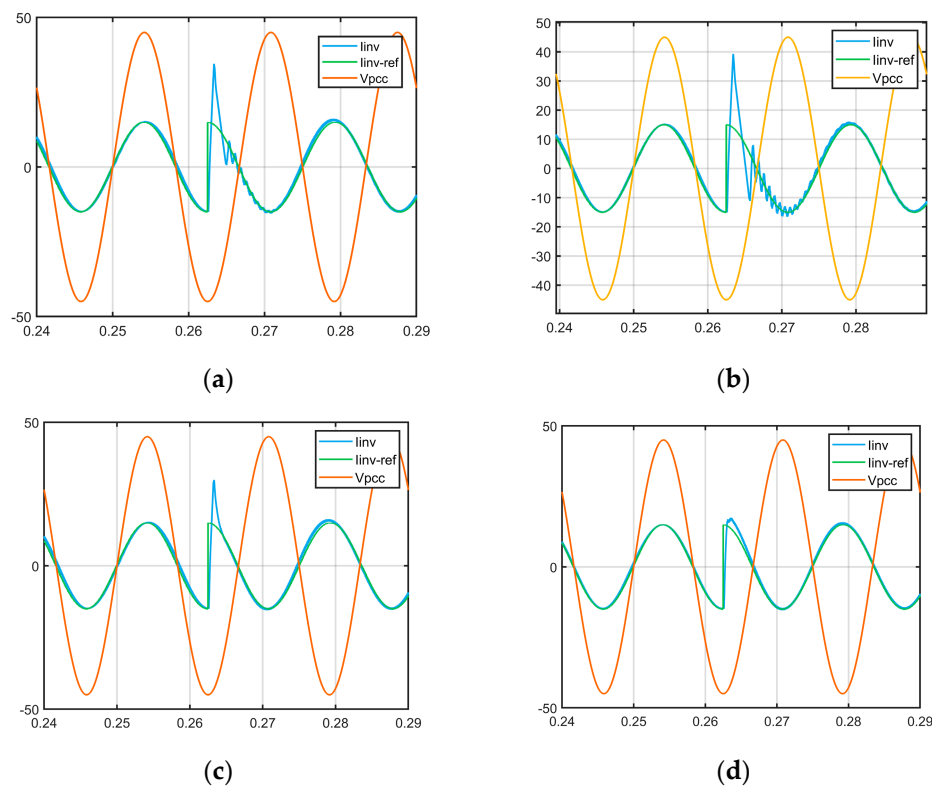
Figure 17. The PCC voltage (divided by 4), the inverter output current, and its reference signal when bidirectional power flow is investigated: (**a**) Integral-single-lead, (**b**) integral double-loop, (**c**) integral double-loop considering the PWM delay effect, and (**d**) resonant filter.

The second topic is the performance of the PLL. Figure 18 shows the PCC voltage, the current reference signal, and the theta signal of the PLL with 5% related to the fundamental at the fifth harmonic. The theta signal, as well as the reference signal for the inverter output current, is clean even in the presence of harmonics. The reference signal is purely sinusoidal. This shows that the PLL employed in this paper was enough to operate under distorted voltage grids.
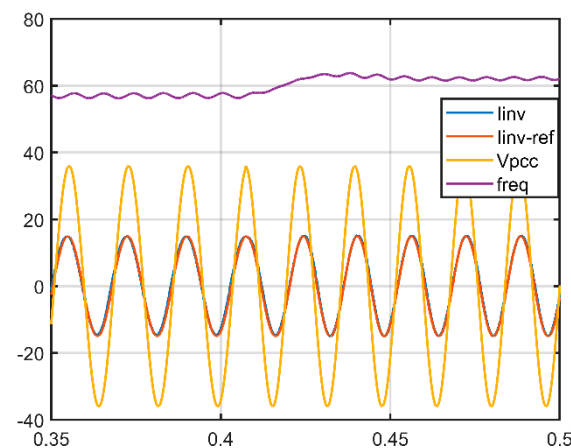

Figure 18. The PCC voltage (divided by 4.5), the current reference signal, and the theta signal of the PLL with 5% related to the fundamental at the fifth harmonic.

Another topic that deservers discussion is the frequency of the grid where the inverter is connected. Even though the procedures proposed in this paper used 60 Hz as frequency of the grid, their equations were valid to grid with 50 Hz as well. Attention must be paid to design the PR controller, in which

the tuned frequency must be 50 Hz. Moreover, it is attractive to choose the frequency and sampling frequency as multiple of the grid frequency. This makes the ratio between the switching frequency and the grid frequency an integer number, which avoids loss of information during programming the DSC.

Weak grids often experience frequency variation at the PCC. Consequently, a grid-connected inverter must be able to work under frequency variation conditions. Depending on the deviation of the frequency value, the inverter must either switch off or keep working [3]. Concerning the four controllers proposed in this paper, the PR is the more sensitive for frequency variation. In order to make a PR able to track the frequency variation at the PCC, its parameter tuning procedure needs to be adaptive. Adaptive approaches were beyond the scope of this paper. However, the PR designed in this paper as well as the PLL can work under frequency variation. This is due to the non-null bandwidth of them. Figure 19 shows the PCC voltage, the inverter output current, its reference signal, and the frequency measurement of the PLL during a transition in the frequency of the PCC from 57 to 62 Hz. Such a variation is one of the most severe in weak grids and their limits may not last for more than seconds. The inverter output current keeps following its reference signal with negligible steady-state error. The oscillation in the frequency measurement was expected because the PLL is designed to work at 60 Hz. This oscillation does not compromise the performance of the controller. Therefore, the proposed PR controller is able to work satisfactorily in a weak grid with frequency variation.

Figure 19. The PCC voltage (divided by 5), the inverter output current, its reference signal, and the frequency measurement of the PLL during a transition in the frequency of the PCC from 57 to 62 Hz.

7. Conclusions

This paper prosed highly accurately digital current controllers for LCL-filtered grid-connected inverters. The current controllers were the integral single-lead, integral double-lead, integral double-lead taking into account the effect of PWM delay, and the PR. A step-by-step procedure for each one was carefully presented and investigated. Later, the controllers were designed, and the Bode diagram showed the achievement of pre-specified desired parameters.

The proposed controllers were implemented in a physical DSC TMS320F28335 while the power structure was run in the HIL 402 (Typhoon HIL Inc., Novi Sad, Serbia). Results showed the accurate performance of the controller in making the inverter output current follow its reference signal with a steady-state null error. The controlled variables did not show either oscillatory or unpredictable behavior. Therefore, the controllers proposed in this paper are attractive solutions for single-phase LCL-filtered grid-connected inverters. Moreover, the tuning procedures are an easy, fast, and accurate way to design the proposed digital current controllers.

Author Contributions: T.D.C.B. proposed the main idea of this research. He prepared the formulation, the simulation, and the settings of the HIL under the supervision of M.G.S. Additionally, T.D.C.B. ran, collected the results, and wrote this paper while M.G.S. and K.Z. revised it. All the authors were involved in preparing the submitted version of this manuscript. All authors have read and agreed to the published version of the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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