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High Output Third-Order Intercept Point Low-Noise Amplifier Design Based on 0.13 μm CMOS Process for High-Precision Sensors †

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Abstract: This paper proposes a highly linear low-noise amplifier (LNA) using a cascode configuration. In the proposed topology, the linearity of the circuit is enhanced through the application of derivative superposition technology. The technology combines an auxiliary transistor operating in the moderate inversion region with a main transistor operating in the strong inversion region, and two degenerative inductors are connected in series at the source nodes of both transistors. The primary objective of this design is to mitigate the negative impacts of second-order and third-order nonlinearities on the third-order input intercept point (IIP3) through their interactions, thereby enhancing the linear performance of the circuit. An on-chip active bias circuit is designed to effectively address fluctuations in the IIP3 during process and temperature variations by stabilizing the transconductance of the common-source transistor, enabling the LNA to operate reliably in complex environments. During post-layout simulation in DongBu High-Tech's 0.13 μm CMOS process, the circuit's output third-order intercept point (OIP3) exhibits minimal fluctuations across different process corners and temperature variations. At the typical nmos and typical pmos (TT) process corner and a temperature of 30 °C, it achieves an OIP3 of 33.9 dBm with a power consumption of 42 mW sourced from a 2.8 V power supply. Furthermore, it realizes a relatively flat gain of 16 dB, a noise figure (NF) of 0.91 dB, input return loss less than −8 dB, and output return loss less than −10 dB.

Keywords: low-noise amplifier; derivative superposition; linearity improvement

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1. Introduction

In recent years, the rapid development of Internet of Things (IoT) technology has significantly boosted the network access demands of various devices, while high-performance sensors, as the core components of IoT systems, are responsible for collecting real-time and precise data from the environment and devices [1]. However, ensuring that these data can be transmitted to IoT platforms with high reliability, low latency, and high data rates has become a crucial challenge driving the future development of IoT. To overcome the limitations of previous cellular standards, the Fifth Generation (5G) of mobile communication technology emerged, providing a powerful impetus for the leapfrog development of IoT. Among its innovations, 5G's introduction of Multiple Input Multiple Output (MIMO) technology utilizes multiple antennas for signal transmission and reception, achieving substantial increases in data transmission rates, notable reductions in latency, and enhanced transmission reliability [2]. Nevertheless, as the number of antennas and modulation points grows, the issue of mutual interference between adjacent frequency signals becomes increasingly severe, posing higher demands on the distortion suppression capabilities

of radio frequency (RF) receiving modules during signal reception. In this context, the low-noise amplifier (LNA), a vital component in the RF receiving link, has become a significant research and optimization topic regarding its linearity performance and stability under varying temperatures and process corners. In numerous IoT fields, LNAs with high linearity play a significant role in transmitting sensor data with high fidelity. For example, in industrial automation, high-linearity LNA can markedly optimize the data transmission from industrial sensors to the central controller, thereby enabling precise adjustment and control during production processes. In intelligent transportation systems, they enhance the signal transmission between vehicular communication devices and traffic management systems, improving the accuracy of traffic information transmission. In the agricultural IoT, high-linearity LNA ensure stable signal transmission between various sensors in farmland and data centers. In the field of smart healthcare, high-linearity LNA further elevate the communication quality between medical devices. All these instances demonstrate the important role of LNA in transmitting sensor data with high fidelity. Therefore, in advancing the continuous development of IoT technology, it is not only necessary to continue exploring the potential of advanced communication technologies like 5G but also to attach great importance to and effectively address the performance optimization of key components such as LNA, ensuring high quality, efficiency, and reliability in IoT data transmission.

For LNA, maintaining linearity stability across different manufacturing processes and varying temperatures poses a challenge. In [3,4], researchers propose a method that involves adjusting the source inductances of both the auxiliary and main transistors. This adjustment strategically manipulates the amplitude and phase of the third-order nonlinear coefficients of the auxiliary transistor. The objective is to achieve a condition where the vector sum of these third-order coefficients from both transistors is equal in magnitude but opposite in direction. By achieving this condition, third-order intermodulation distortion can be effectively cancelled out, leading to an improvement in the overall third-order intermodulation performance of the amplifier.

To mitigate the significant variations in the third-order input intercept point (IIP3) caused by process and temperature fluctuations, ref. [3] employs an independently programmable circuit to precisely control the gate bias voltage. This approach offers high accuracy but introduces complexities in circuit design and incurs additional hardware costs. Ref. [5] simplifies the regulation process by dedicating separate pads for the gate voltages of both the main transistor and the auxiliary transistor. These pads are connected to an external DC power supply, allowing direct adjustment to optimize the IIP3 for different scenarios. While this approach is easy to implement, it greatly increases the time required for testing and maintenance in large-scale production or complex system integrations. Ref. [6] mentions that by applying substrate biasing techniques to the auxiliary transistor, its optimal bias point can be made more stable compared to gate voltage control under process, voltage, and temperature (PVT) variations. However, experiments have revealed that the improvement effect of this approach is limited.

Another challenge in this design pertains to crafting a current source that boasts a straightforward circuit architecture and minimal fluctuations across varying process temperatures. Ref. [7] describes a method of deriving a current source by subtracting two proportional-to-absolute-temperature (PTAT) currents. However, during practical implementation, it was observed that the resistors in the two PTAT circuits experienced different environmental conditions and other influencing factors, leading to varying ratios of resistance changes under different process corners. This, in turn, resulted in significant fluctuations in the final current output across different process corners. Alternatively, ref. [8] introduces an accurate current reference utilizing a temperature and process compensation current mirror (TPC-CM). Nevertheless, this approach is quite intricate and necessitates individual chip calibration, adding to the complexity of the design process.

In this paper, we investigate methods to maintain stable linearity under varying process and temperature conditions and present the realization of an LNA based on the derivative superposition method with source bias. The Section 2 of the article delves into

the analysis and design of the circuit, while the Section 3 presents the simulation results. The Section 4 discusses the overall study and its implications.

2. Circuit Analysis and Design

2.1. Linearity Analysis

The nonlinearity of a transistor is caused by the voltage–current conversion, and the relationship between the drain current of the transistor and the gate-source voltage can be expressed as follows:

$$i_d = g_{m1}V_{gs} + g_{m2}V_{gs}^2 + g_{m3}V_{gs}^3 + \dots \quad (1)$$

where i_d represents the drain current of the transistor, and V_{gs} represents the gate-source voltage of the transistor. g_{m1} is a small signal transconductance, g_{m2} is called the second-order nonlinear coefficient, and g_{m3} is called the third-order nonlinear coefficient.

The derivative superposition method is achieved by taking advantage of the different polarities of the transistor's third-order nonlinear coefficient under different operating conditions. Under appropriate biasing conditions, the transistor operating in the strong reflective region is connected in parallel with a transistor operating in the weak inversion region. This arrangement is designed so that the negative nonlinear peak of the transistor in the strong inversion region is aligned with the positive nonlinear peak of the transistor in the weak inversion region, thus effectively canceling out the mutual nonlinear effects in a certain range of V_{gs}. Therefore, the total third-order nonlinearity coefficient that characterizes the nonlinearity of the combined system is approximately zero in this V_{gs} range.

Apart from the third-order nonlinear coefficients, second-order nonlinear components may also propagate back to the signal source through specific feedback mechanisms. When these second-order components mix with the original signal, they can generate third-order intermodulation distortion (IMD3), further exacerbating the third-order offset phenomenon. For instance, in a source-follower negative feedback configuration, the source degeneration inductance provides a feedback path that allows the drain current to couple through the gate-source capacitance to the gate-source voltage. This feedback path can inadvertently return the second-order nonlinear components to the input, exacerbating the overall nonlinearity. Consequently, to enhance the IIP3, it is crucial to mitigate not only the third-order nonlinearity but also the second-order nonlinearity.

2.2. Low-Noise Amplifier Circuit Design

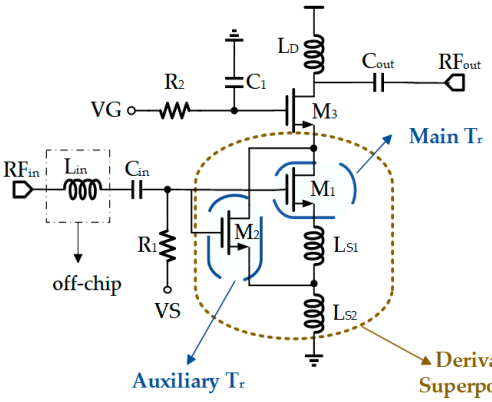
The schematic diagram of the proposed LNA is shown in Figure 1. The core architecture of the presented LNA is a cascode type. The derivative superposition section is composed of the main transistor M_1, auxiliary transistor M_2, and source degeneration inductors L_{s1} and L_{s2}. In this configuration, M_1 operates in the strong inversion region, while M_2 operates in the moderate inversion region. The source degeneration inductors L_{s1} and L_{s2} help mitigate the degradation of the IIP3 that can be caused by the second-order nonlinear coefficients of M_1. M_3 is a common-gate transistor. L_{IN} serves as an off-chip input matching element, and by adjusting its size, it can accommodate operational requirements across different frequency bands. L_D and C_{OUT} form the output matching network. Resistors R_1 and R_2 play a role in limiting the current to prevent excessive current from flowing into the circuit and damaging the transistor. Capacitor C_1 is used to filter out high-frequency noise. Furthermore, ESD protection circuits have been designed at the RF input, RF output, and power supply terminals, significantly enhancing the reliability of the circuit.

The main noise sources of the circuit are shown in Figure 2, and the main noises of the MOSFET transistor are drain current noise and gate-induced noise. The formula of drain current noise is shown in Equation (2), and the formula of gate-induced noise is shown in Equation (3).

$$\overline{i_{nd,X}^2} = 4kT\Delta f\gamma_X g_{d0,X} \quad (2)$$

$$\overline{i_{ng,X}^2} = 4kT\Delta f\delta_X g_{g,X} \quad (3)$$

where $i_{nd,x}^2$ is the drain current noise of transistor X, $i_{ng,x}^2$ is the gate-induced noise of transistor X, K is the Boltzmann constant, T is the absolute temperature, and Δf is the frequency spacing. γ_x and δ_x are the bias-dependent noise coefficients of transistor X. $g_{d0,x}$ is the drain-source conductance at zero V_{DS} of transistor X, V_{DS} is the drain-source voltage of the transistor, and $g_{g,x}$ is the gate admittance under high-frequency excitation of transistor X.



Component	Value
M_1	W/L=140×4/0.13μm
M_2	W/L=480×4/0.385μm
M_3	W/L=320×4/0.385μm
L_{in}	20n
C_{in}	3.57p
L_{s1}	0.5n
L_{s2}	0.7n
$R_{1,2}$	32.26k
C_1	3.73p
L_D	12n
C_{out}	3.96p

Figure 1. The proposed low-noise amplifier structure.

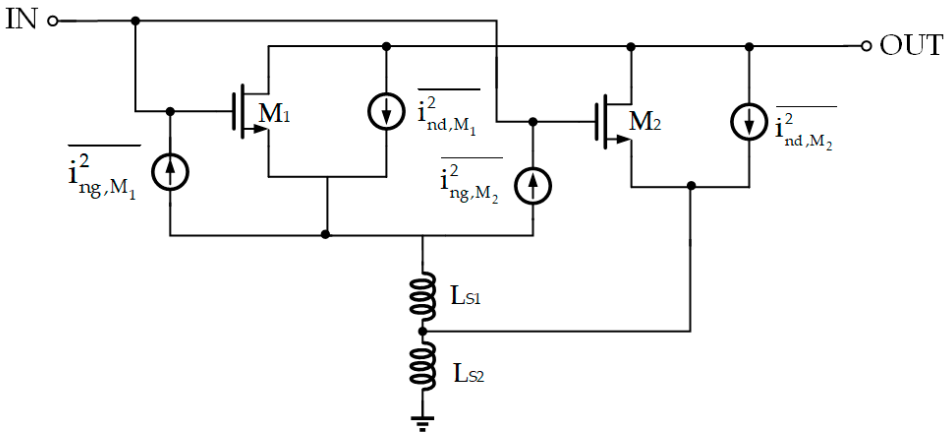


Figure 2. The proposed schematic diagram of the main noise sources.

The final derived minimum noise expression is shown in Equation (4).

$$F_{min} \approx 1 + \frac{2}{g_{m,M_2}} \sqrt{\gamma_{M_2} g_{d0,M_2} [\delta_{M_1} g_{g,M_1} + \delta_{M_2} g_{g,M_2} (1 - |c_{M_2}|_2)]} \quad (4)$$

where F_{min} represents the minimum noise figure and $g_{m,X}$ represents the transconductance of transistor X.

The size of the transistor can be reasonably designed based on this formula to minimize the noise of the circuit as much as possible.

2.3. Bias Circuit Design

For a common source amplifier with negative feedback at the active pole, the IIP3 expression is as follows:

$$A_{IIP3} = \sqrt{\frac{4|g_{m1}|}{3|g_{m3}|}} \quad (5)$$

The expression for g_{m1} is shown in Equation (6).

$$g_{m1} = \frac{g_m}{1 + g_m R_S} \tag{6}$$

where R_s represents the value of the negative feedback resistance at the source. The expression for g_{m3} is as follows:

$$g_{m3} = -\frac{\mu_n^2 C_{ox}^2 W^2 R_s}{2(1 + g_m R_S)^5 L^2} \tag{7}$$

The expression for g_m is as follows:

$$g_m = \mu_n C_{ox} \frac{W}{L}(v_{gs} - v_{th}) \tag{8}$$

where μ_n represents the effective mobility of electrons, C_{ox} represents the capacitance per unit area of the gate oxide layer, W is the channel width, L is the channel length, and vth is the threshold voltage. μ_n and vth are parameters related to process and temperature.

From Equations (5)–(7), we can get the expression of A_{IIP3} as follows:

$$A_{IIP3} = \sqrt{\frac{4g_m}{3R_s}} \frac{2L(1 + g_m R_s)^2}{\mu_n C_{ox} W} \tag{9}$$

From Equation (9), it can be observed that ensuring the stability of the transconductance of the common-source transistor can assist in reducing fluctuations in the IIP3 across different process corners and temperature variations.

The bias circuit structure used in this paper is shown in Figure 3. Iout is a process- and temperature-independent current reference source. Transistors M_4 and M_5 are connected as diodes and provide gate bias voltages VS and VG, respectively, for the common source and common gate stages. Resistors are used to increase the value of VG.

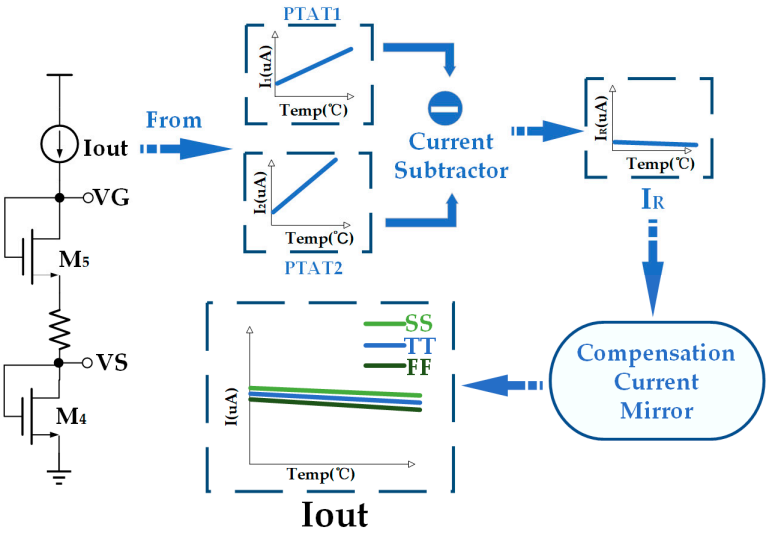


Figure 3. Bias circuit.

As depicted in Figure 4, the current source design in the bias circuit involves subtracting the currents obtained from PTAT1 and PTAT2 using a current subtractor circuit. To compensate for the varying ratios of resistance changes in the PTAT1 and PTAT2 circuits due to different environmental conditions or other factors, which can result in a significantly smaller current at the slow nmos slow pmos (SS) process corner compared to the typical nmos and typical pmos (TT) and fast nmos fast pmos (FF) process corners, a compensation

current mirror circuit is incorporated. The switch (SW1) of this compensation current mirror can be directly controlled by high and low levels provided by an external power supply, or it can be controlled based on the output level of a comparator that compares the potential at point A with the magnitude of a reference voltage. Considering the importance of circuit simplicity, this paper adopts the approach of directly controlling the conduction and cutoff of this current path through an external power supply. Consequently, a current source, Iout, with minimal variations due to temperature and process changes is achieved.

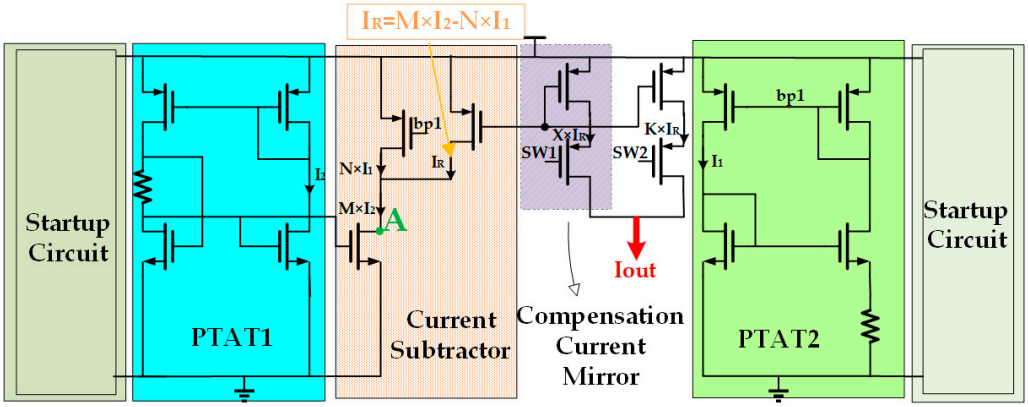


Figure 4. Current source circuit.

The common source stage bias voltage is as follows:

$$VS = \sqrt{\frac{2Iout}{\mu_n C_{ox}(\frac{W}{L})_{M_4}}} + V_{TH,M_4} \quad (10)$$

As can be seen from Equation (10), when the process and temperature change, the threshold voltage of transistor M_4 also changes. When transistor M_4 and common source transistor M_1 choose the same type of transistor, and at the same time, the position of the two transistors is reasonably considered, so that the threshold voltage of the two transistors can change the same under the influence of process and temperature, so that the threshold voltage change in transistor M_4 cancels the change in the threshold voltage of common source transistor M_1, maintains the stability of the transconductance of common source transistor M_1, and improves the stability of output third-order intercept point (OIP3) of the circuit.

3. Simulation Results

The proposed LNA was simulated using the 0.13 μm CMOS process from DongBu Hi-Tech. The layout of the proposed LNA, as shown in Figure 5, occupies an area of 0.575 × 0.390 mm^2. With an inductance value of 20 nH for the off-chip input matching inductor and a corresponding quality factor (Q-factor) of 40, the LNA operates within the frequency band of 703 MHz to 850 MHz. As depicted in Figure 6, the simulation results indicate that within the specified frequency band, the input return loss remains below −8 dB, the output return loss is less than −10 dB, the peak gain achieves 16 dB, and the minimum noise figure (NF) is 0.9 dB. A linearity test was conducted on this designed LNA using a two-tone signal with a power of −30 dBm and a frequency spacing of 5 MHz. Figure 7 presents the simulation results of OIP3 under different process corners and temperatures, demonstrating a notable improvement in the stability of OIP3 compared to [5]. Table 1 compares the LNA designed in this paper with related published papers. The results indicate that the LNA designed in this paper exhibits certain advantages in terms of noise performance and linearity.

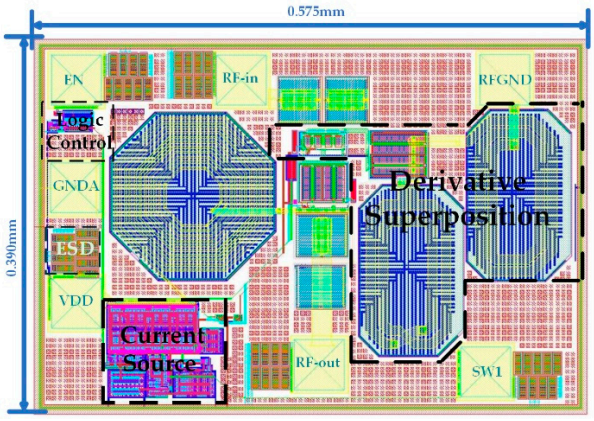


Figure 5. Layout of LNA.

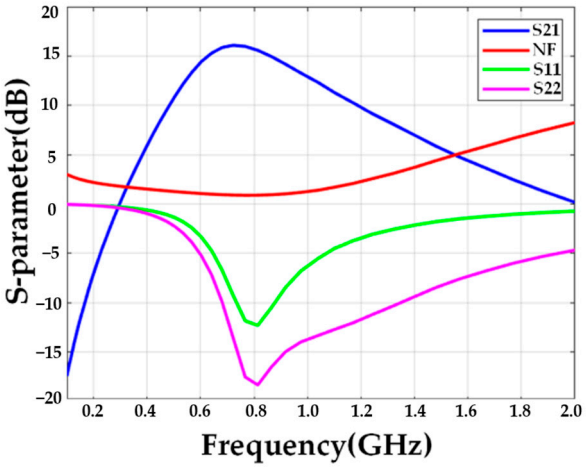


Figure 6. S-parameters results of the proposed LNA.

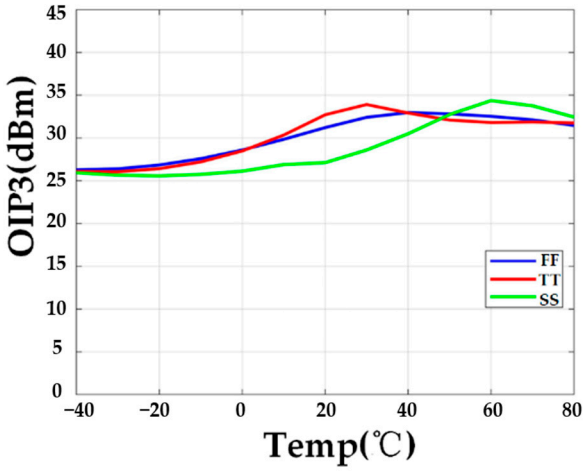


Figure 7. The output third-order intercept point of the proposed LNA under different process corners and different temperatures.

Table 1. Comparison of the proposed LNA with other studies.

Ref.	Technology (nm)	Frequency (GHz)	Pdc (mW)	S21 (dB)	NF (dB)	OIP3 (dBm)
[9]	90 nm CMOS	1.3	132	15.4	1.36	33.7
[10]	0.18 μm SiGe	14.4–21.4	18	20.3	2.14	5.1
[11]	0.13 μm CMOS SOI	7.1	24.5	16.5	1.03	23.7
[12]	45 nm CMOS SOI	32.5	32.5	19.5	2	11.5
This study	0.13 μm CMOS	0.8	42	16.0	0.91	33.9

4. Conclusions

This paper presents the design of a high-linearity LNA based on the derivative superposition method, utilizing DongBu High-Tech's 0.13 μm CMOS process. The design incorporates an active bias circuit to compensate for changes in the OIP3 caused by temperature and process variations. This not only enables the LNA to operate in complex environments but also improves the yield rate of the manufactured high-linearity chips. The LNA's layout measures 0.575×0.390 mm^2. Under the TT process corner and at a temperature of 30 °C, the LNA exhibits an OIP3 of 33.9 dBm, with a power consumption of 42 mW at a supply voltage of 2.8 V, a power gain of 16 dB, an NF of 0.91 dB, an input return loss of less than −8 dB, and an output return loss of less than −10 dB. The high-linearity LNA designed in this paper exhibits exceptional data transmission fidelity and adapts well to complex and diverse working environments. Taking the farmland IoT as an example, this LNA can transmit with high fidelity the data collected by various sensors in farmland (such as soil moisture sensors, temperature sensors, etc.) under different temperature conditions to a data center, greatly facilitating researchers' data processing tasks. Similarly, in fields such as intelligent transportation systems, industrial automation, and smart healthcare, sensors operating under various temperature conditions can all rely on the high-linearity LNA designed in this paper for stable data transmission.

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