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A Low-Cost Voltage Surge Monitor with Temperature Compensation for Electrified Aircrafts †

Zhao Song *, Jiarui Han, Qiang Shao and Yang Ma

AVIC Xi'an Flight Automation Control Research Institute (FACRI), Xi'an 710000, China; 18930315526@163.com (J.H.); shaoqiang0219@163.com (Q.S.); mayang14@126.com (Y.M.)

* Correspondence: szh-98@alumni.sjtu.edu.cn

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Abstract: Along with the trend of aircraft electrification, the penetration of power electronics converters in aircraft energy systems is gradually deepening. Due to the nonlinear behavior and low inertia of aircraft power grids, voltage overshooting and oscillation may occur. Therefore, a voltage surge monitor (VSM) is a safety-critical part in more-electric and electric propulsion aircrafts. VSMs often need a time delay response, so a stable delay time is important. Microprocessors and timer chips can realize accurate time delays but are relatively expensive. Having an extremely low cost and simple structure, RC filters with a discharge diode are popular in consumer electronics operating under narrow temperature ranges (0 °C~70 °C). However, it is unsuitable for aircrafts because of its severe temperature drift cause by the discharge diode. In this paper, a low-cost VSM with temperature compensation is proposed. A detailed mathematical model, simulation, and hardware experiments are conducted for demonstration and verification. Results have shown that the delay time of our VSM circuit has low temperature drift (<0.15%) and accuracy comparable to the typical timer chip LTC6994.

Keywords: voltage surge monitor; temperature compensation; electric propulsion; MEA

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1. Introduction

1.1. The Necessity of a Voltage Surge Monitor in Electrified Aircrafts

According to the statistics of the Intergovernmental Panel on Climate Change (IPCC), civic aviation transportation has become one of the fastest growing areas of greenhouse gas emission [1]. Aircraft electrification is a key technology for green aviation. Airplanes are currently experiencing two stages of electrification: more-electric aircraft (MEA) and electric propulsion aircraft (EPA). In MEAs, hydraulic and barometric energy are replaced with electricity, integrating electric generation, distribution, and consumption devices into one system [2]. Replacing fuel with electricity in primary power, EPA are a major and thorough innovation and revolution in aircraft electrification [3–6].

Along with the electrification of aviation, power electronics is gradually penetrating into the airplane energy system. The transient and nonlinear behavior of loads usually lead to grid voltage fluctuation. In addition, output voltage overshooting or oscillation also occur due to the low inertia of power electronics system [7]. In the fly-by-wire system of the A380 (see Figure 1), a typical MEA for example, the whole flight control system (FCS) is powered by power conditioning modules (PCMs). The output power quality of PCMs has a direct influence on FCSs.

Therefore, the voltage surge monitor (VSM) is indispensable. When the bus voltage or output voltage of a power converter is too high or too low, the VSM will raise a voltage fault flag for failure reporting, protection triggering, or power supply redundancy shifting. In fact, it is already a widely used unit in current aircrafts.

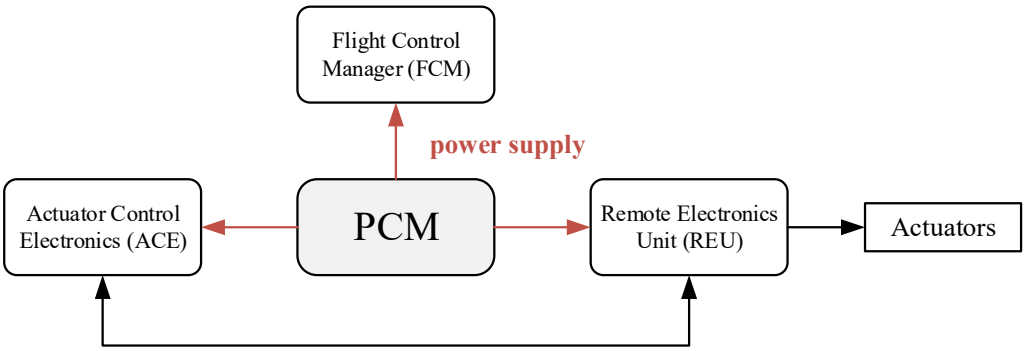


Figure 1. Power distribution of fly-by-wire system in MEA.

1.2. Time Delay in VSMs

The VSM is not just a voltage comparator because the endurance of loads against voltage over-ranges varies for different voltage values. For instance, the normal 28VDC voltage surge limitation is 47 V/5 ms, 40 V/30 ms, and 17 V/30 ms (RTCA/DO-160G, class-A equipment) [8], as shown in Figure 2. If the output voltage of a PCM is 43 V (greater than 40 V but less than 47 V) or 16 V (less than 17 V), the VSM should raise a fault state within 30 ms. However, if the voltage exceeds 47 V, the delay time becomes 5 ms, which means the VSM must respond earlier.

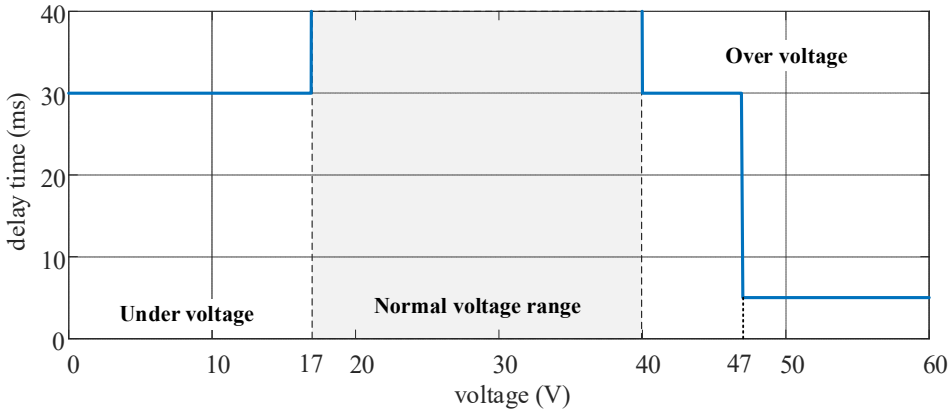


Figure 2. 28VDC normal voltage surge of RTCA/DO-160G class-A equipment.

As can be seen from the above, accurate delay time control is critical in VSMs. If the delay time is too short, an unexpected fault flag will be raised frequently, interfering with the normal function of the aircraft power system. Otherwise, the VSM will fail to alert on the fault state in time when the voltage exceeds the normal range.

Three popular delay methods are listed in Table 1. Microprocessors and timer chips (like the LTC6994 [9,10]) can realize an accurate time delay but are relatively expensive. Having an extremely low cost and simple structure, RC filters with a discharge diode are popular in consumer electronics with a low reliability requirement and narrow operating temperature. However, it is unsuitable for aircrafts because of its severe temperature drift cause by the reverse current of discharge diodes [11]. Resistance and capacitance will also change with temperature, causing a deviation in the RC time constant [12].

Table 1. Comparison of different delay methods.

Delay Method	Delay Time Accuracy	Cost
Microprocessor	High	Very High
Dedicated timer chips	High	High
RC filter with discharge diode	Low (high temperature drift)	Very Low

1.3. Contribution of This Work

In this paper, a low-cost VSM with low temperature drift is proposed. It derives from the low-cost RC delay circuits in consumer electronics, but contains a temperature compensation scheme. Our temperature compensation is extremely lucid—just by adding a shunt diode to counterbalance the reverse current of discharge diode. Although simple at a glance, detailed mathematical modeling, simulation, and hardware experiments are conducted for demonstration and verification. All results have shown that our simple VSM circuit has low delay time temperature drift and comparable accuracy to timing chips.

2. Architecture of the VSM

2.1. VSM for Electrified Aircrafts

Figure 3 is a simplified illustration of Figure 1, where the PCM distributes power from the aircraft bus bar to the load devices. The VSM monitors the PCM output voltage and raises a voltage surge flag. This flag can be transmitted to loads or to the PCM to activate the protection subsystem.

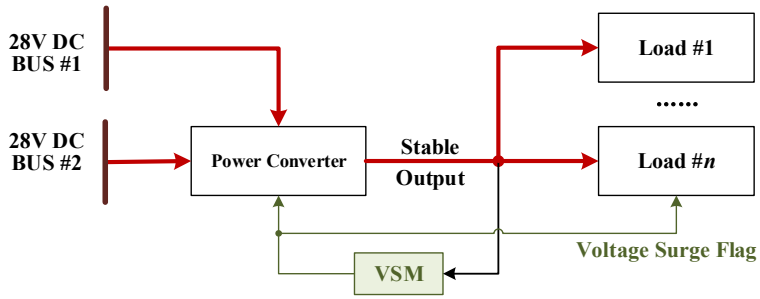


Figure 3. The VSM in an MEA power distribution system (simplified).

2.2. VSM Behavior Logic

Figure 4 is the architecture of the VSM. The monitored voltage U_{in} is firstly compared with multiple thresholds, and the comparison results are buffered and then converted into several digital values d_k. In each VSM branch, the delay circuit and the AND-gate delay the rising-edge of d_k, and S_k becomes logic-high if the time that d_k remains high exceeeds t_{dk}.

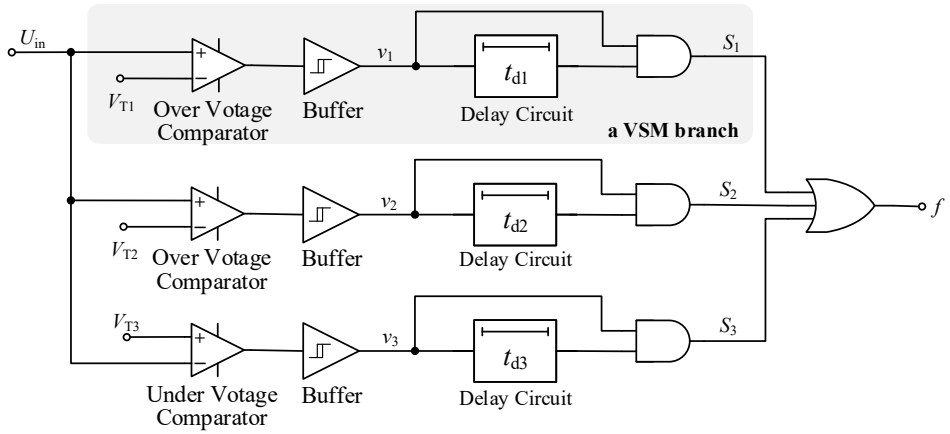
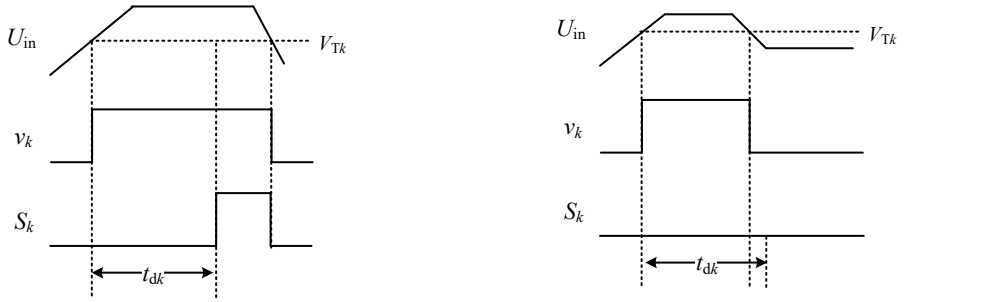


Figure 4. The proposed delay circuit.

The timing diagram of one VSM branch is shown in Figure 5. If one branch outputs a logic-high, the final output of VSM (f) becomes logic-high, indicating the surging voltage of U_{in} exceeds the safe limitation.



(**a**) The time when $V_{Tk} > U_{in}$ exceeds t_{dk} (**b**) The time when $V_{Tk} > U_{in}$ is less than t_{dk}

Figure 5. The timing diagram of a VSM branch (k = 1, 2, . . .).

3. Low-Cost Delay Circuit with Temperature Compensation

The delay circuit is the most important part of a VSM, which is shown in Figure 6. When the input voltage v_i is high ($v_i = V_{DD} = 5V$), the capacitor C is charged through resistor R. Then, the capacitor voltage u increases and the output v_o will become high when $u \geq V_T$. When $v_i = 0$, the capacitor C is discharged by D1 rapidly, thus resetting the output v_o. Shunt diode D2 is added for temperature compensation, and detailed analysis and explanation will be given later. Merely composed of a few passive components and a comparator, the circuit in Figure 6 is a very simple and cheap design.

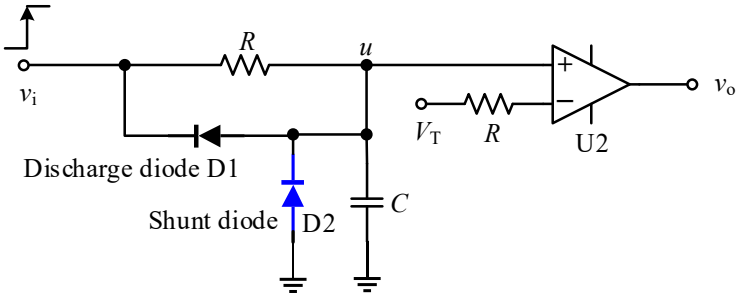


Figure 6. The proposed delay circuit.

3.1. Component Temperature Characteristics

Since the VSM shall work in a full temperature range (−40 °C~125 °C), resistance R and capacitance C are all functions of temperature T.

$$R(T) = [1 + \alpha(T - T_{nom})]R_{nom} \quad (1)$$

$$C(T) = \left[1 + \beta_1(T - T_{nom}) + \beta_2(T - T_{nom})^2\right]C_{nom} \quad (2)$$

where R_{nom} is the nominal resistance, T_{nom} = 25 °C is the reference temperature, and α, β_1, and β_2 are their temperature coefficients.

In order to realize a high precision delay with a low temperature drift, R is usually a high precision resistor with resistance error ε_R = 0.1% and temperature coefficient α = 25 ppm/°C. In this paper, the C0G MLCC manufactured by muRata is chosen for the delay capacitor C. The temperature coefficients can be obtained from a regression analysis of muRata official data [12]. We have $[\beta_1, \beta_2] = [4 \times 10^{-4}, 6 \times 10^{-6}]$, and $r^2 = 0.999$, $p < 10^{-5}$.

In a common RC delay circuit analysis, the reverse current of diode D1 is usually neglected. However, this reverse current increases with temperature dramatically. For the aircraft VSMs, the temperature characteristic of the diode reverse current should be taken into consideration for higher delay accuracy and stability. Figure 7 is the reverse current curve. It can be observed that the reverse current is influenced by both temperature T and

reverse voltage V_r. For $V_r < 20$ V, the reverse current can be fitted by Equation (3) based on the data given in Figure 7 [13].

$$\lg I_r(T, V_r) = \gamma_0 + \gamma_t T + \gamma_v V_r \tag{3}$$

where $[\gamma_0,\ \gamma_t,\ \gamma_v] = [0.1448,\ 0.0277,\ 0.0222]$, and $r^2 = 0.9793,\ p = 1.76 \times 10^{-13}$.

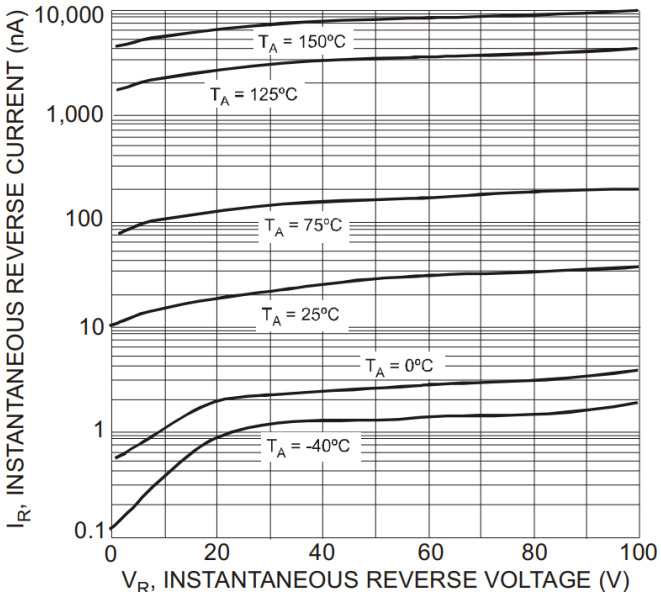


Figure 7. Diode reverse current (Figure 3 of [13]).

3.2. Circuit Modeling in Full Temperature Range

Based on the component temperature characteristics above, the proposed RC delay circuit can be modeled by a partial differential equation (PDE).

$$C(T)\frac{\partial u}{\partial t} = \frac{v_i - u}{R(T)} + I_{r1}(T,\ v_i - u) - mI_{r2}(T,\ u) \tag{4}$$

In Equation (4), the capacitor voltage is u, and I_{rk} denotes the reverse current of diode Dk. The input voltage, time, and temperature are v_i, t, and T, respectively. If the shunt diode D2 is introduced then $m = 1$, and m equals 0 otherwise. Diode D1 and D2 have the same parameters.

For the delay time calculation, the stimuli and initial criteria of Equation (4) are

$$\begin{cases} v_i = V_{DD}\varepsilon(t) \\ u|_{t=0} = 0(\forall T \in [-40^\circ\text{C}, 125^\circ\text{C}]) \end{cases} \tag{5}$$

where $\varepsilon(t)$ is the unit step function. Then, the delay time t_d satisfies $u|_{t=t_d} = V_T$.

4. Verification

4.1. Temperature Sweep Simulation

To verify the proposed model in Section 3, a VSM is designed subject to Figure 2 and simulated using PSpice. In the simulation circuit of Figure 8, all chips and diodes are PSpice models obtained from official websites of their manufacturer. The temperature sweep simulation results are shown in Figure 9. The solid lines denote the delay time curve calculated by the mathematical model in Section 3, and the dots are PSpice simulation results which is consistent with the mathematical model.

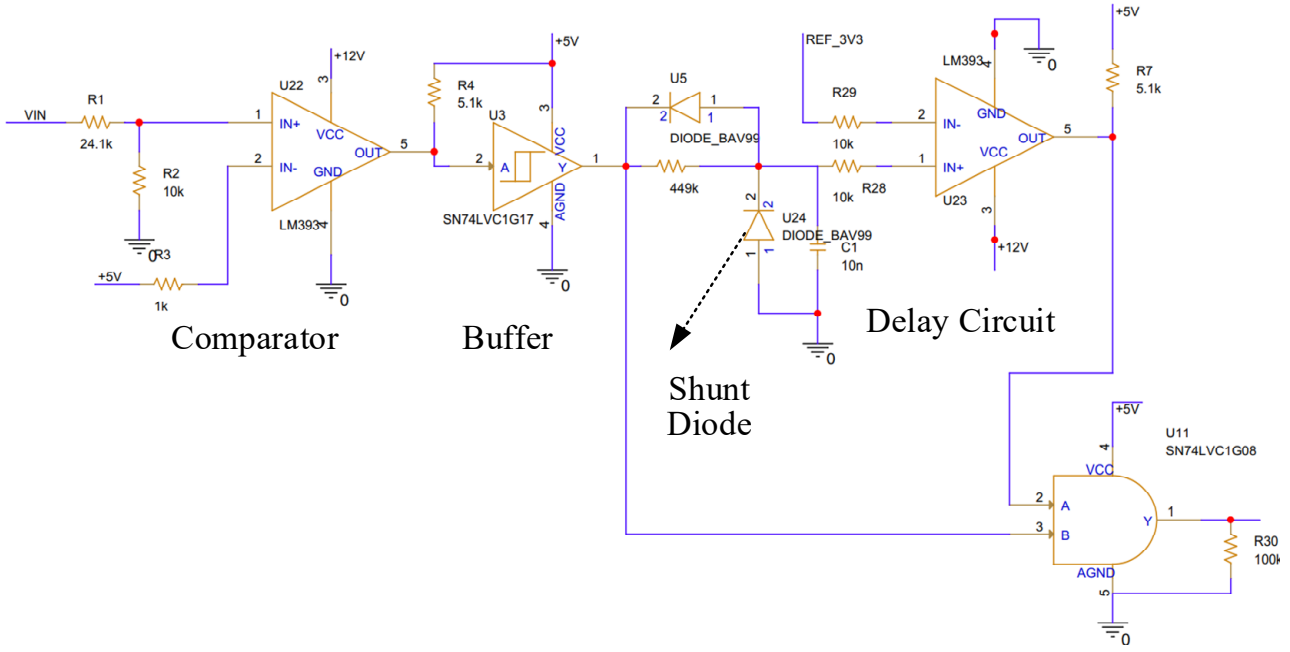
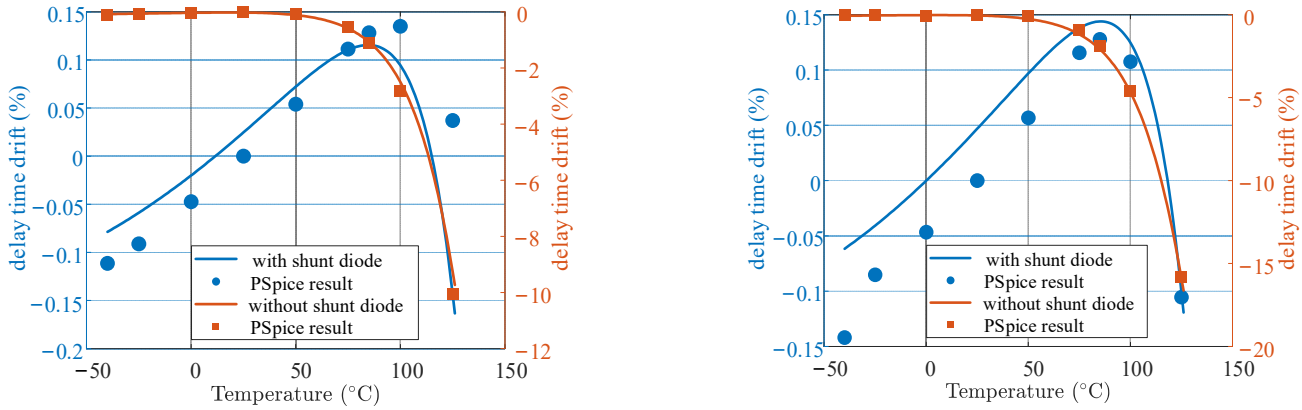


Figure 8. Simulation circuit in pSpice for temperature sweep.



(**a**) delay time drift for 5 ms delay (**b**) delay time drift for 30 ms delay

Figure 9. Temperature drift of VSM delay time.

It is obvious that the delay time rapidly decreases with T in the absence of shunt diode D2, resulting in significantly higher temperature drift or delay time error. By simply adding a shunt diode D2, the delay time deviation is suppressed within ±0.15%, which is comparable to the temperature drift data given in the LTC6994 datasheet.

4.2. Hardware Experiment

For further verification, a VSM prototype is built as in Figure 10. Important devices in the prototype are listed in Table 2.

Empirical waveforms of three VSM branches are shown in Figures 11–13. In Figure 11, for example, when the input voltage (the green curve) exceeds 47 V, the voltage comparator output becomes 5 V (the orange curve). Then, the capacitor begins to be charged, and its voltage increases gradually (the red curve). When the capacitor voltage reaches $V_T = 3.33$ V, the final output of the 47 V/5 ms monitor toggles (the blue curve). The rising edge delay between the orange curve and the blue curve is exactly 5 ms. Similarly, the delay time in Figures 12 and 13 is 30 ms, indicating the effectiveness of the proposed VSM.

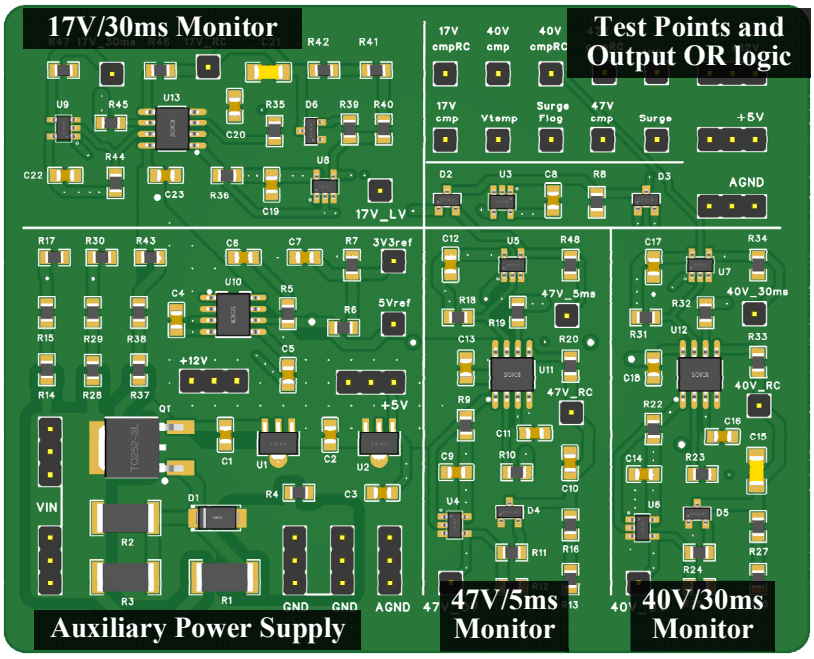


Figure 10. The VSM prototype to monitor the 28VDC normal voltage surge of Figure 2.

Table 2. Important devices in the prototype.

Devices	Part Name	Key Features
Voltage comparator	LM393BIDR (Texas Instruments, Dallas, TX, USA)	Low input bias current
Capacitor (for 30 ms delay)	GRM31C5C1H104FA01L (Murata, Kyoto, Japan)	100 nF ± 1%, C0G
Capacitor (for 5 ms delay)	GRM2195C1H103FA01D (Murata)	10 nF ± 1%, C0G
Resistors (for voltage dividing and time delay)	\	±0.1%, ±25 ppm/°C
Discharge and shunt diodes	BAV99Q-7-F (DIODE Inc., Plano, PX, USA)	2 diodes in one package

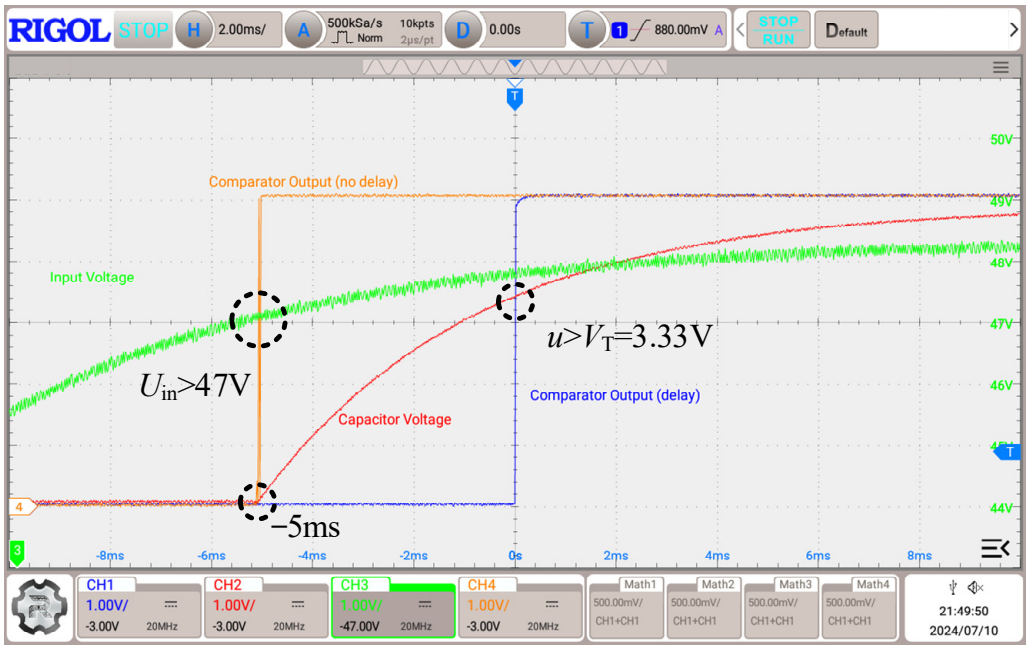


Figure 11. Output of 47 V/5 ms over-voltage monitor.

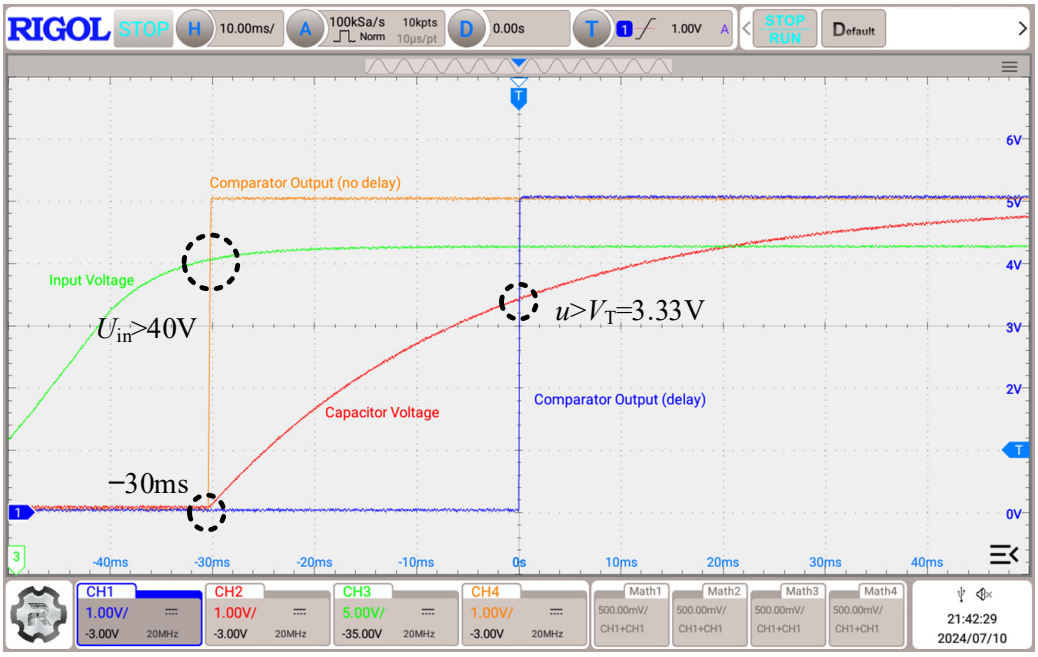


Figure 12. Output of 40 V/30 ms over-voltage monitor.

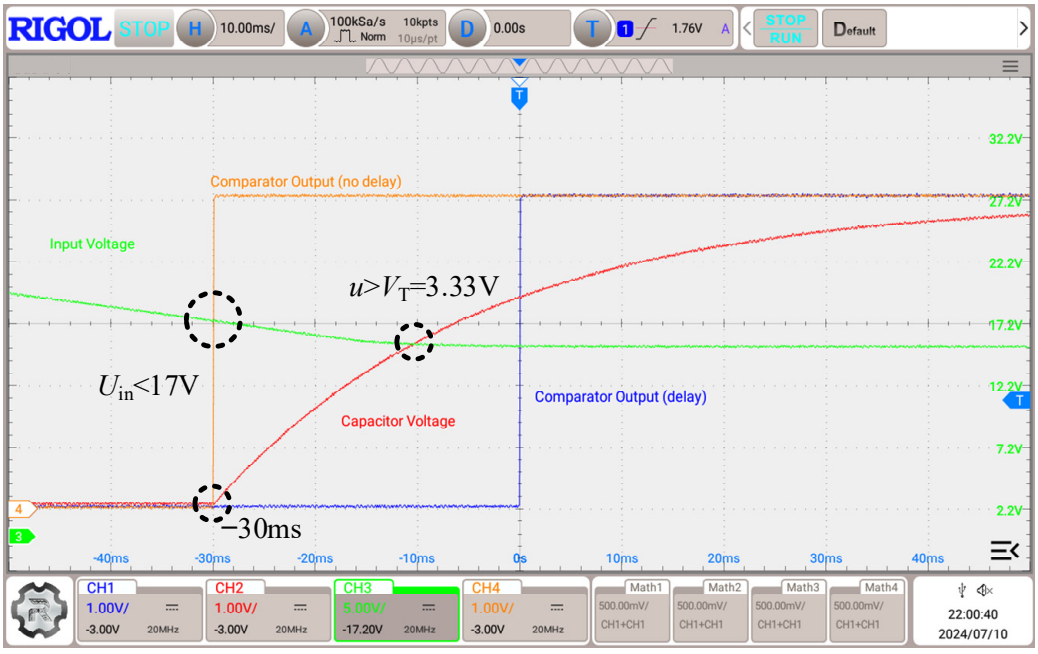


Figure 13. Output of 17 V/30 ms under-voltage monitor.

4.3. Delay Circuit Comparison

After the simulation and experiment, a comparison of performance and cost are conducted between the delay method in this paper and the timer chip LTC6994 (see Table 3). Here, the microprocessor is no longer considered because of its complexity (software involved) and high cost. Since the resistance and capacitance error are 0.1% and 1% in Table 2, the RC time constant error of the VSM is $(1+1\%)(1+0.1\%)-1 \approx 1.1\%$. So, the delay time accuracy of this paper is comparable to LTC6994, but the cost is only 21.3% that of LTC6994. Therefore, the delay method proposed in this paper has advantages in cost without too much performance degradation.

Table 3. Comparison between this paper and LTC6994.

Delay Method	This Paper	LTC6994
Delay time temperature drift	<0.2% (see Figure 9)	<0.5% [9]
Delay time error	1.1% (RC time constant)	<2.3% [9]
Cost (RMB, data comes from https://www.szlcsc.com/, accessed on 12 July 2024)	6.406 (one VSM branch)	30 (just one chip)
Number of components for time delay	10	1

In conclusion, both timer chips and the circuit in this paper are feasible methods for VSMs in electrified aircraft. For a low-cost design, the circuit in Figure 6 is more suitable. But when the available PCB area is extremely limited, the timer chip is a better choice due to its high integration.

5. Conclusions

In this paper, a low-cost VSM with temperature compensation is proposed. The architecture and behavior logic of the VSM is briefly demonstrated. Then, the mathematical model of the VSM is built for circuit operation under a full temperature range. To verify the proposed VSM, both a PSpice simulation and hardware experiment are carried out. The PSpice temperature sweep results and our model are generally consistent, and the delay time drift decreases from 10% to 0.15% by simply adding a shunt diode. Physical experiment results show that the proposed VSM can respond according to the expected delay time and voltage threshold. Finally, a comparison between the proposed VSM and the typical timer chip LTC6994 is given in this paper. The VSM delay time accuracy is comparable to LTC6994, but the cost is only 21.3% that of LTC6994.

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