



Proceeding Paper Design of a Signaling Scheme for Three Equal-Power Signals in a New Navigation Satellite System [†]

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Abstract: Design methods are presented for chip pulses and a constant envelope multiplexing (CEM) scheme for a new navigation satellite system in the S band. If we assume three equal-power signals are needed to transmit, the chip pulses of at least two signals can have two or more sample magnitudes for a high CEM power efficiency. Considering a case with two dual-magnitude signals, we can find the magnitude values for a target efficiency and then design the magnitude and sign patterns. We analyze the interference for all possible chip pulse sets and sorted them according to selected priorities. We also consider spectral separation between two different signal groups for a flexible operation. The design methods and the results provided in this paper can be a good reference for the signal design of a new navigation satellite system.

Keywords: signal design; chip pulse; constant envelope multiplexing; navigation satellite system

1. Introduction

In navigation satellite systems, except for GLONASS (Global Navigation Satellite System) and FDMA (frequency-division multiple access) [1], several independent signals are transmitted syn-chronously in time at an identical carrier frequency. They use direct-sequence spread-spectrum signals but, unlike typical wireless communication systems, the signals can have different chip rates and chip pulses [2–6]. Although the signals use different spreading codes, the chip pulses are designed to guarantee far lower inter-and intra-system interference. Furthermore, the signals in a frequency band are properly multiplexed to have a constant envelope, in order to maximize the power efficiency of the high-power amplifiers.

Most legacy navigation satellite signals use single-magnitude bi-phase chip pulses, so the constant envelope multiplexing (CEM) scheme can then be designed independently of the chip pulse design. On the other hand, some special requirements can unite the two designs. In this paper, we assume that three equal-power signals are transmitted and present a set of design methods for chip pulses and CEM, with example design results.

2. Design Methodology

In most cases of legacy navigation satellite systems, the signals transmitted in a frequency band have different data rates and/or target QoS's (qualities of services), and thus have different transmit powers. In this paper, on the other hand, we assume that all the signals in a frequency band have an identical transmit power and only the data rates are determined by the target QoS's. It is similar to the case of Galileo E5, where four signals transmitted with an identical power. But, if the number of equal power signals is three, we need some modifications or constraints in the design of the constant envelope multiplexing scheme, as well as the chip pulse waveforms.

If we simply use bi-phase chip pulse waveforms, which have a single sample magnitude, for equal power assumption, the CEM power efficiency cannot exceed 75%. That is, as



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Copyright: © 2023 by the author. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). much as 25% of the total transmit power is consumed in order to tailor the baseband sample constellation to have identical magnitudes. However, if we allow some of the chip pulse waveforms to have two or more magnitudes with equal average powers, the instantaneous signal powers can be different, and thus we can achieve a high CEM power efficiency. In this case, the designs of the CEM scheme and the chip pulse waveforms are tightly coupled.

In this paper, we assume to have a pair of dual-magnitude signals and a singlemagnitude signal to transmit in the S band centered at 2492.028 MHz with a bandwidth 16 MHz.

2.1. Constant Envelope Multiplexing Scheme

Let us denote the three baseband signals as $s_1(t)$, $s_2(t)$, and $s_3(t)$, where the chip pulse waveforms of $s_1(t)$ and $s_2(t)$ have two magnitudes, α and β ; $0 < \alpha < \beta$ at an equal probability of 0.5 and $s_3(t)$ is a bi-phase signal with single magnitude, γ . The equal average power condition requires $\alpha^2 + \beta^2 = 2\gamma^2$. We further assume $|s_1(t)| = \alpha$ whenever $|s_2(t)| = \beta$, and vice versa, for simple design. Then, the magnitude values are determined as $\alpha = \sqrt{\frac{\eta - \sqrt{(4\eta - 3)\eta}}{3}}$, $\beta = \sqrt{\frac{\eta + \sqrt{(4\eta - 3)\eta}}{3}}$, $\gamma = \sqrt{\frac{\eta}{3}}$ for a given target CEM power efficiency, with η and the CEM results in $s_{CEM}(t) = s_1(t) + s_2(t) + j \left[s_3(t) - \frac{3}{\eta} s_1(t) s_2(t) s_3(t) \right]$ [7].

2.2. Chip Pulse Waveforms

Under the constraints from the previous Section 2.1, the magnitude and sign patterns of the chip pulse waveforms are designed. With some heuristic efforts, we can employ the exhaustive search method, analyzing the interference for all possible sets of chip pulses to find the best set with the minimum worst inter- and intra-system interference. For a fast and efficient preliminary design, we can use the spectral separation coefficient (SSC) as an asymptotic metric of the interference [8].

In this paper, we sort the analysis results, first by the worst inter-system interference from a candidate signal set to the legacy signals, and then by the maximum inter-system interference from the legacy signals to the candidate signal set, and intra-system interference among the candidate signal set. The list is then investigated one by one to find the best signal set with a low out-of-band emission and transmitter and receiver complexity. If necessary, we can also apply an additional requirement that one of the three signals has its spectrum near the center of the S band, whilst the spectra of the other two are located at the outer parts of the band. The spectral separation allows for flexible operation in the inner and outer parts of the frequency band, with marginal interference between them.

3. Design Results

We performed the exhaustive analyses described in Section 2.2 with the CEM scheme in Section 2.1, for an arbitrary CEM power efficiency of $\eta = 0.93$, and sorted them. The list was shortened by constraining each worst SSC to not exceed the minimum worst SSC observed for all possible chip pulse waveforms by 10 dB or more.

3.1. Design Results without Spectral Separation

First, we searched for proper chip pulse waveforms without the requirement of separated spectra. Figures 1 and 2 show the chip pulse waveforms and their spectra, designed for the case of two 1.023 Mcps signals and a 2.046 Mcps signal. The inter-system SSCs to the legacy signals are observed to be less than -74.86 dB/Hz and the inter-system SSCs from the legacy signals and the intra-system SSCs are less than -66.73 dB/Hz. For another case, with a 1.023 Mcps signal and two 2.046 Mcps signals, we found the chip pulse waveforms in Figure 3, whose spectra are shown in Figure 4. In this case, the inter-system SSCs to the legacy signals are observed to be less than -71.92 dB/Hz and the inter-system SSCs from the legacy signals and the intra-system SSCs are less than -68.27 dB/Hz.



Figure 1. Chip pulses designed for two 1.023 Mcps signals and a 2.046 Mcps signal in the S band.







Figure 3. Chip pulses designed for a 1.023 Mcps signal and two 2.046 Mcps signals in the S band.



Figure 4. PSDs of the chip pulses designed for a 1.023 Mcps signal and two 2.046 Mcps signals in the S band.

3.2. Design Results with Separated Spectra

Let us assume that a signal has its spectrum in the inner band and the other two have their spectra in the outer band. Figures 5 and 6 show a proper design example for the case of two 1.023 Mcps signals and a 2.046 Mcps signal. In this case, the inter-system SSCs to the legacy signals are less than -63.50 dB/Hz, whilst the inter-system SSCs from legacy and the intra-system SSCs are less than -63.85 dB/Hz. It is obvious that the requirement of separated spectra significantly reduces the degree of freedom in the design, and we can see that the worst SSCs respectively increase by 11.36 dB and 2.88 dB, in comparison with those in Section 3.1.



Figure 5. Chip pulses designed for two 1.023 Mcps signals and a 2.046 Mcps signal with spectral separation in the S band.

Unfortunately, we could not find any signal set for the case with a 1.023 Mcps signal and two 2.046 Mcps signals. That means that either the worst inter- or intra-system SSC is larger than the minimum for all possible chip pulse waveforms by 10 dB or more. In this case, we should consider loosening the worst interference requirement. Frequency division multiplexing (FDM) can be another solution. However, the FDM signals should be carefully designed to have a constant envelope, unless separate high power amplifiers are used for each signal, which is typically undesirable in practice.



Figure 6. PSDs of the chip pulses designed for two 1.023 Mcps signals and a 2.046 Mcps signal with spectral separation in the S band.

4. Conclusions

A set of design methods for the chip pulses and CEM of three equal-power signals were presented. Under the condition of equal transmit powers, a pair of signals had dual magnitudes for a high CEM power efficiency. The proposed set of design methods had a high degree of freedom and thus novel sets of chip pulse waveforms could be obtained with relatively good interference performance. We designed the signals for the cases with and without the requirement of separated signal spectra and found that the worst interferences can significantly increase with spectral separation. The design methods presented in this paper and the design results can be a good reference for planning a new navigation satellite system, including the future Korea Positioning System.

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