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A Comparative Analysis of a Multilevel Inverter Topology Based on Phase Disposition Sinusoidal Pulse Width Modulation †

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Abstract: A Multilevel Inverter (MLI) meets the power requirements of most power electronic applications. It can provide an AC supply with better power quality. The higher number of levels in an MLI results in better power quality output. The fundamental question that comes to mind is what the optimal number of levels can be in designing an MLI for better performance. This paper aims to provide a comparison of three-, five-, and seven-level schemes based on a "Diode Clamped MLI" and will analyze their performance on the reduction of Total Harmonic Distortion (THD).

Keywords: multilevel inverters; voltage source inverters; control techniques; pulse width modulation; diode-clamped topology; switching losses; total harmonic distortion

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1. Introduction

In modern industries nowadays, conventional DC drives have been replaced by variable-speed induction motor drives. Although DC motor drives have good speed torque characteristics, they have certain limitations and disadvantages. Therefore, MLIs are considered the most empowered power alteration technology for various operations such as Flexible AC Transmission System (FACTS) devices, electric drives, etc. MLIs are preferred for employment in medium- and high-power operations. There are several advantages like reduced Total Harmonic Distortion (THD), less electromagnetic interference (EMI) at the output, and less power dissipation from electronic switches. MLIs have many advantages as compared with the traditional two-level inverter, and these include the ability to generate output with low switching losses and better power quality, the increased efficiency of the system without reducing the overall power of the system, decreases in Total Harmonic Distortion (THD), and the use of a very low rating of the devices [1]. In electrical energy production, transmission, and distribution sectors, MLIs are now considered the leading-edge technology for power conversion from DC to AC. The higher number of levels results in better power quality; however, there has been debate on what the optimal number of levels in an MLI can be. In the literature, several papers use multi-level topology; therefore, there is a need to identify an optimum number of levels in an MLI [2]. A diode clamp, flying capacitor, and a cascaded H-bridge are the basic MLI configurations. Certain limitations were faced by basic topologies, such as the drifted neutral-point voltage in the clamping diode inverter and unbalanced voltage appearing at the DC-link of the flying capacitor [3]. Many researchers have been trying to boost the output voltage level without using inductors and transformers; therefore, switched capacitor (SCs) inverters are now being used, which have the advantages of high output stepped waveform and high voltage gain [4]. In both commercial and residential applications, inverters without transformers

are widely used in PV systems that are grid-connected [5]. MLIs guarantee the reduction of harmonic contents and a shift to a high-frequency region, which automatically decreases the cost and size of the filters required [6].

A pulse width modulation (PWM) switching control scheme is a method of reducing the total power supplied by an electrical signal, which is accomplished by effectively dividing it into discrete parts. The value of the average voltage consumed by the load is controlled by the operation of the switch in the operating load at a fast rate. The PWM method uses many triangular carrier signals that are level-shifted or phase-shifted, and a comparison between a single sine wave-modulating signal and gating signal is generated by one intersection for the respective switches [7].

2. Methodology

The paper uses both a diode-clamped multilevel inverter (MLI) topology and Phase Disposition Sinusoidal Pulse Width Modulation (PD-SPWM) as a modulation technique. The proposed switching technique PD-SPWM offers lower switching losses, increased power-handling capability, and proficiency in power quality [8]. The diode-clamped inverter topology limits the voltage stress of power devices through clamping diodes and a common DC bus, while the selected number of switches and diodes depends upon the level to be designed [9]. The n-level diode-clamped multilevel inverter requires two $(n - 1)$ switches, one $(n - 1)$ input carrier wave, and one input sinusoidal wave $(n - 1)$ $(n - 2)$ diodes to generate the required levels of output with minimum harmonic distortion. The output voltage is half of the input DC voltage as the diode transfers a limited part of the voltage. The capacitance of the capacitors used is low, which minimizes switching losses during leveling output [5,9]. In the Phase Disposition SPWM technique, all the carrier signals are of the same frequency, amplitude, and in-phase but are level-shifted. Gating signals for the switches are generated at the time when the sinusoidal wave cuts the carrier waves to generate respective levels.

In this paper, we compared the results of a three-phase diode-clamped MLI topology for three levels, five levels, and seven levels with the PD-SPWM control technique. Open Loop MATLAB®simulation was performed with a reference sinusoidal modulating signal, and several triangular-shaped carriers were used, which were distributed by a Phase Disposition switching technique. Later in this paper, the conclusion results from a Fast Fourier Transform (FFT) analysis are reported.

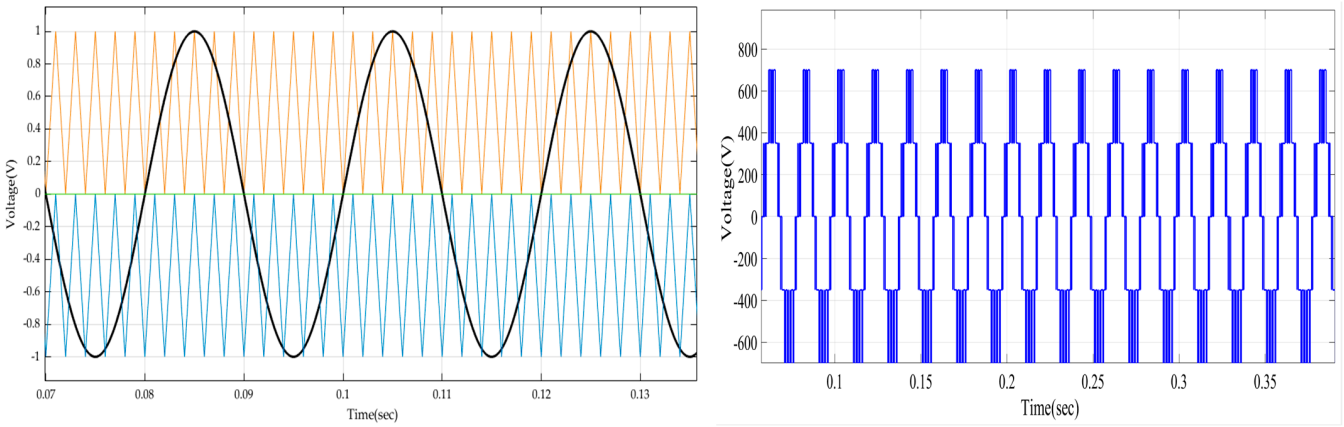
3. Simulation Results

3.1. Three-Phase Three-Level Inverter

Three-level inverters are widely used for power compensation as an alternative to medium- and high-voltage applications. The three-level inverter is widely used in industrial applications due to its simplicity [10]. There are three input waves, including one sinusoidal modulating signal and two triangular carrier waves of a magnitude of 1 volt, as presented in Figure 1a. Furthermore, the simulation output is shown in Figure 1b. Line-to-line voltages are also displayed for simplicity and better understanding.

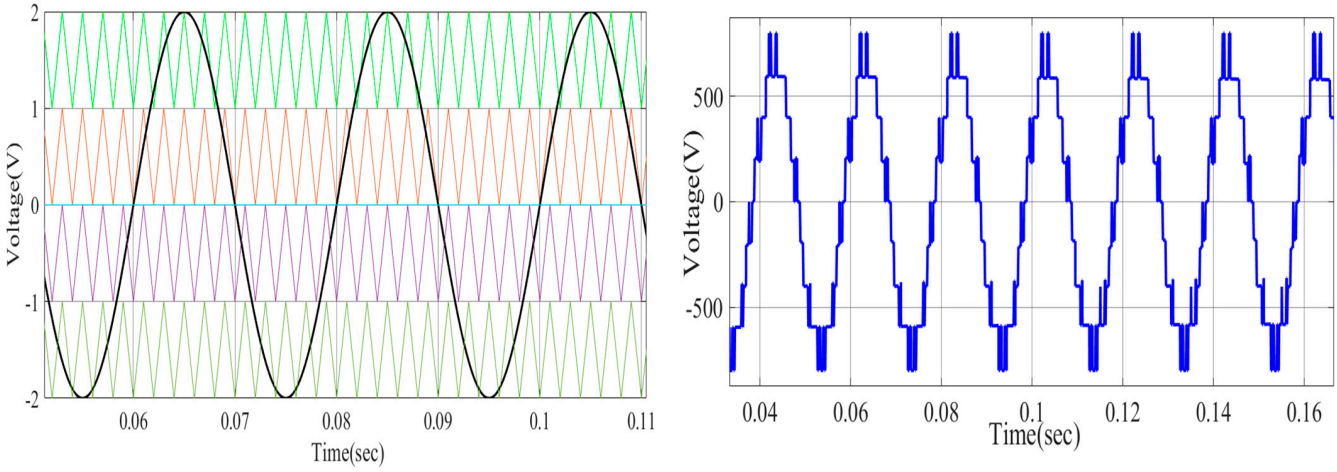
3.2. Five-Level Inverter

The five-level inverter has a popular application, i.e., injecting photovoltaic power into the grid to minimize switching losses and Total Harmonic Distortion. To generate five levels, we need to include one sinusoidal modulating signal and four triangular carrier signals of a magnitude of 1 volt, as shown in Figure 2a, and the output for five-level inverters, as shown in Figure 2b.



(**a**) (**b**)

Figure 1. (**a**) The input waveform of a per-phase three-level inverter (**b**) Line–line voltage of a three-level inverter.

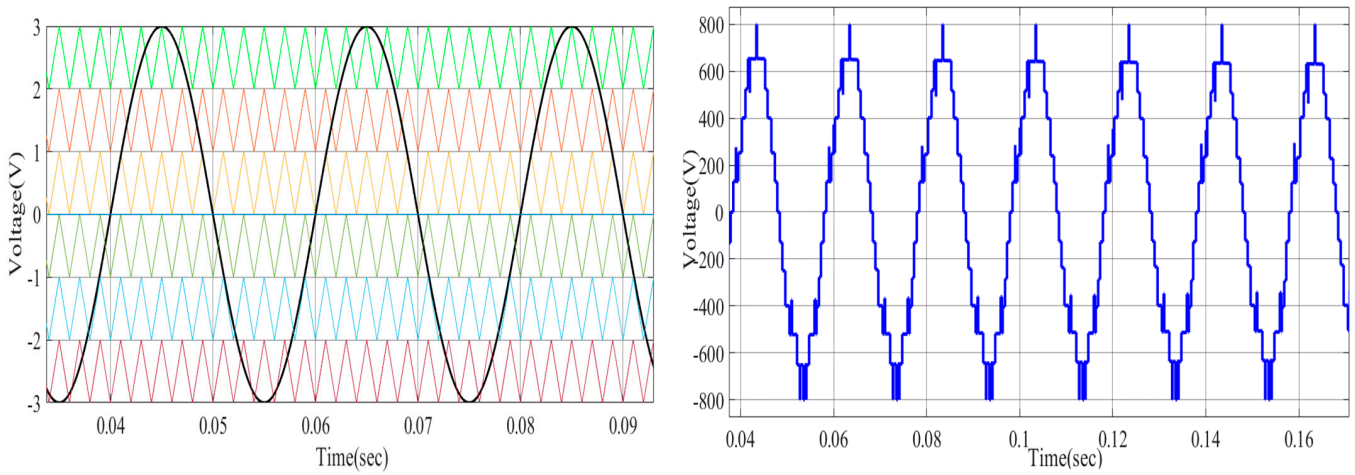


(**a**) (**b**)

Figure 2. (**a**) The input waveform of a per-phase five-level inverter (**b**) Line–line voltage of a five-level inverter.

3.3. Seven-Level Inverter

Seven-level inverters are used in numerous applications such as in Uninterruptable Power Supplies (UPS), Power Transmission through High Voltage DC (HVDC), RERs, and Variable Frequency Drives (VFDs). For seven-level inverters, we need to generate an input signal containing one sinusoidal modulating signal and six triangular carrier waves of a 1 volt magnitude, as shown in Figure 3a; and the output is shown in a line-to-line voltage for seven-level inverters, as shown in Figure 3b.



(**a**) (**b**)

Figure 3. (**a**) The input waveform of a per-phase seven-level inverter (**b**) Line–line voltage of a seven-level inverter.

3.4. Total Harmonic Distortion (THD) Plots

Variations in both switching angles and DC voltages of the inverter affect the power quality of the output voltage of the inverter. It can be reduced by using filters between the inverter and load or by increasing the number of levels. A Fast Fourier Transform (FFT) analysis is typically used for THD calculation in SIMULINK®. Furthermore, Figures 4–6 represent the results of a FFT analysis done in simulation.

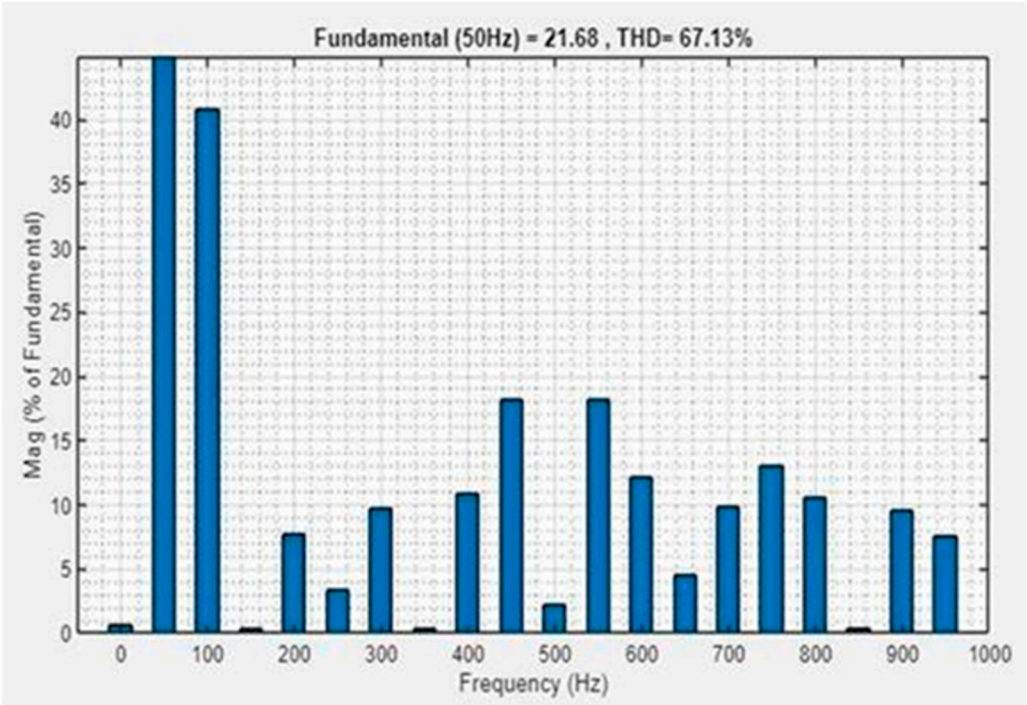


Figure 4. THD of a three-phase three-level inverter.

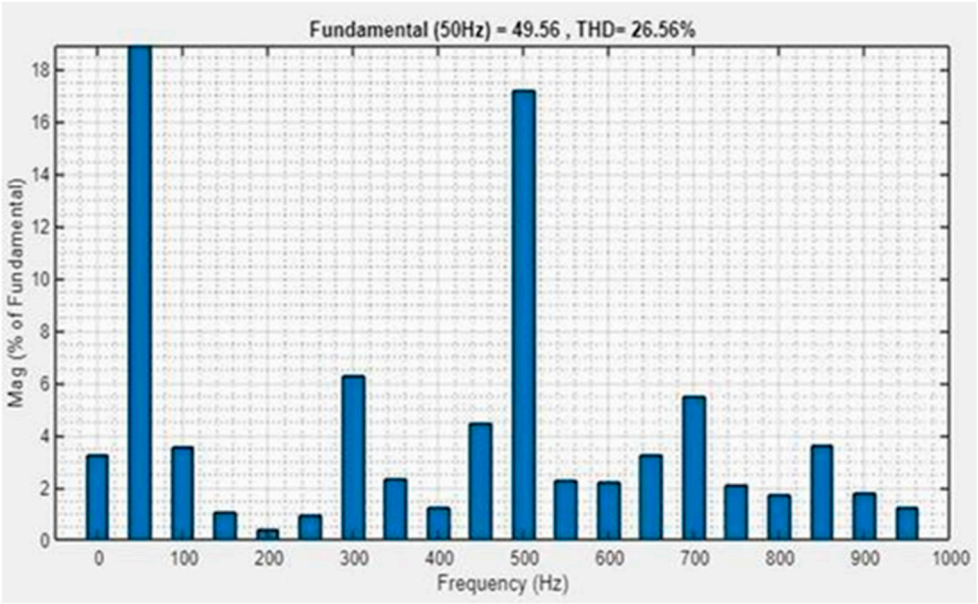


Figure 5. THD of a three-phase five -level inverter.

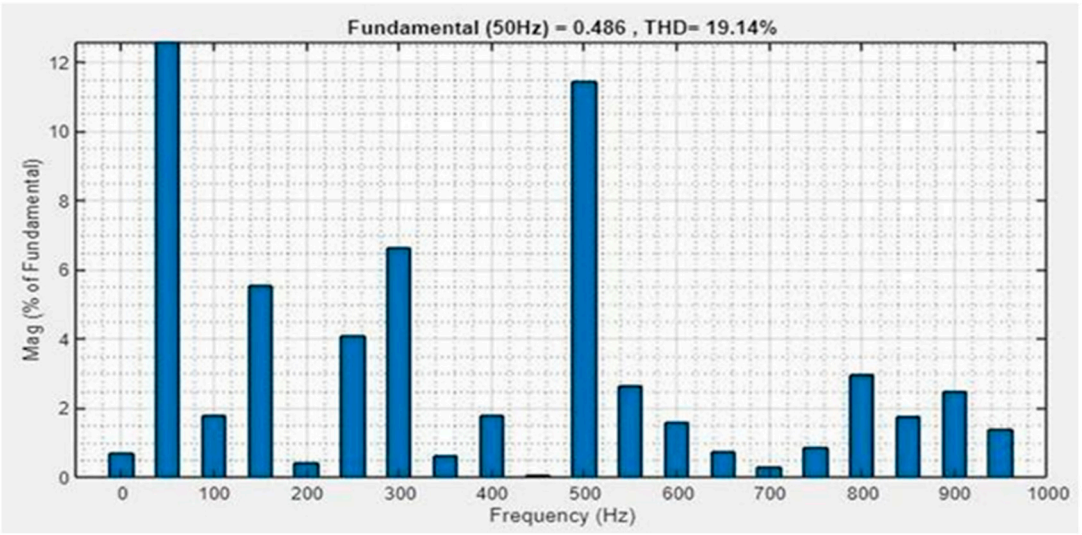


Figure 6. THD of a three-phase seven-level inverter.

3.5. Conclusions

Multilevel inverters are an essential need in the future for power electronic converters. This paper compares multilevel inverter topology and identifies seven levels as the optimum number of levels for a multi-level inverter. The Results section of this paper discussed the THD count of multilevel topologies. As the seven-level inverter had the lowest THD of 19.14, it can be concluded that by increasing the number of levels, reduced THD and improved power quality can be achieved. The switching losses of this topology are also reduced as, among various PWM techniques reported in the literature, PDSPWM has the lowest THD. The hardware setup for this paper is in progress; we have completed a Proteus simulation. In further analysis, the same techniques are to be implemented on hardware and can be utilized in real-time.

3.6. Future Scope

A DCMLI with the PDPWM control technique is preferred, as it results in lower switching losses and can be used in various applications such as to control the speed of the motor.

Author Contributions: The primary concept and research question were developed by M.H.U. He also supervised the project and helped with writing this article. He advised timely during the tenure of this project and assisted in every difficulty faced by the research team. A.A. and U.I. took the lead in refining the research design, including selecting the methodology and data collection tools that best suited the objectives of the study. We conducted an extensive literature review to identify gaps in existing research and to establish the theoretical framework for the study, the formulation of conclusions, and their significance in the broader context of the study. Most of the writing in this report was done by A.U. and M.R.S. All equally contributed to the simulation study and hardware setup of this project. All authors have read and agreed to the published version of the manuscript.

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