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Design of Efficient Phase Locked Loop for Low Power Applications †

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Abstract: The phase-locked loop is a technique that has contributed significantly to technological advancements in many applications in the fast-evolving digital era. In this paper, a Phase Locked Loop (PLL) is designed using 90 nm CMOS technology node with 1.8 V supply voltage. It features a PLL design with minimum power consumption of 194.26 µW with better transient analysis and DC analysis in an analog-to-digital environment. The proposed PLL design provides the best solution for many applications where a PLL is required with high performance but has to be accommodated in less area and low power consumption than state-of-the-art methods. This PLL not only works at high speed but also makes whole system work at low power in a very effective manner, which suits the present digital electronics circuits.

Keywords: Phase Locked Loop (PLL); Phase Frequency Detector/Charge Pump (PFD/CP); Low Pass Filter (LPF); Current Starved Voltage-Controlled Oscillator (CSVCO); Analog Digital Environment (ADE)

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1. Introduction

The current era is all about compact battery devices used in electronic devices. A PLL is used in all SOC devices where circuitry generates a system clock signal. Basically, a PLL has a feedback loop that controls the phase of the output signal with the input signal along with phase error.

Figure 1 shows the block diagram of a PLL. It mainly consists of four blocks namely Phase Frequency Detector (PFD), Charge Pump with Low Pass Filter, a Voltage-Controlled Oscillator (VCO) to provide oscillations and a Frequency Divider [1].

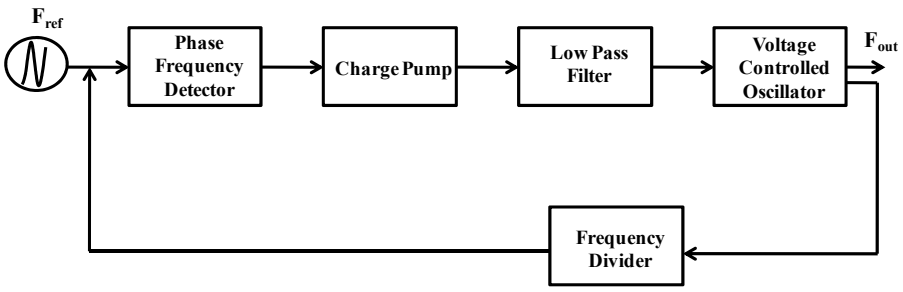

Figure 1. Block diagram of PLL.

2. Methodology

Previously, a multiplier was used as an analog phase detector, but it had a limited blocking range with a phase error of more than 90° where the output voltage is reduced. A digital phase detector was implemented where the mean value is proportional to the phase error [2]. The X-OR gate was used as a phase detector, which is linear, but if it were in phase and the error was greater than 180°, it would lose its linearity. Consequently, the phase-frequency detectors are designed to detect phase and frequency differences, which increases the speed of PLL. For the LPF design, first order filter could be used, but it would introduce ripples as the control voltage jumps high when current is injected from the charge pump. To solve this problem, a second-order low-pass filter was designed to suppress the generated ripple. Firstly, VCOs (Voltage Controlled Oscillators) were designed using LC oscillators or ring oscillators [3]. However, ring oscillators are not stable as they let the switching characteristics of logic gates fluctuate by +/−20% and the disadvantage of LC oscillators has more matrix area. Therefore, the current starved VCOs are realized in our proposed design.

The PLL works in three states: Free Running state, Capture state, and Phase Lock state. As the name suggests, the free-running state refers to the phase in which no input voltage is present. As soon as the input frequency is applied, the VCO starts switching and starts producing an output frequency to be compared, and this stage is called the capture state [4].

The frequency comparison stops as soon as the output frequency equals the input frequency. This phase is known as the phase-locked state. PLL is a convenient circuit block widely used in wireless applications and electronics, from cell phones to radios, televisions, Wi-Fi routers, areas like FM demodulators, AM demodulators, frequency synthesizers, and more recovery, etc. [5].

3. Design and Implementation

The proposed design of 90 nm PLL was composed using cadence virtuoso and consisted of all the blocks of a Basic PLL. In this design, the number of transistors is reduced when compared to the existing designs in [6]. Due to this, the area is reduced. The reduced transistors also lead to a decreased usage of the power consumption and cost. The design of blocks of the proposed PLL are shown and discussed below.

3.1. Phase Frequency Detector

The Phase Frequency Detector (PFD) mainly consists of two D-flip flops and NAND gates. The block diagram of the PFD is shown below in Figure 2. The main purpose of a PFD is to compare the phase and frequency of the input signal with the feedback signal. It has two output signals, UP and DOWN [7].

The design of the low power edge triggered D-Flip flop with 1.8 V is designed with a reduced number of transistors, and the respective output waveforms are shown in Figure 2. This D flipflop has been used in designing the PFD [8].

Figure 3 shows PFD with two input signals, reference signal CLKREF and the feedback signal which is the output of VCO, CLKVCO each as an input to the two D-flipflops. Output of the first D-flipflop enables the positive current source and another the negative current source of the charge pump. Assuming UP=DOWN=0, when CLKREF is high, UP rises thereby CLKVCO rises. When DOWN also is high, NAND gate resets both the D-flipflops. UP and DOWN are high at the same time for a short while, at this point the difference between their average values gives us the phase or frequency difference between both the input signals [9].

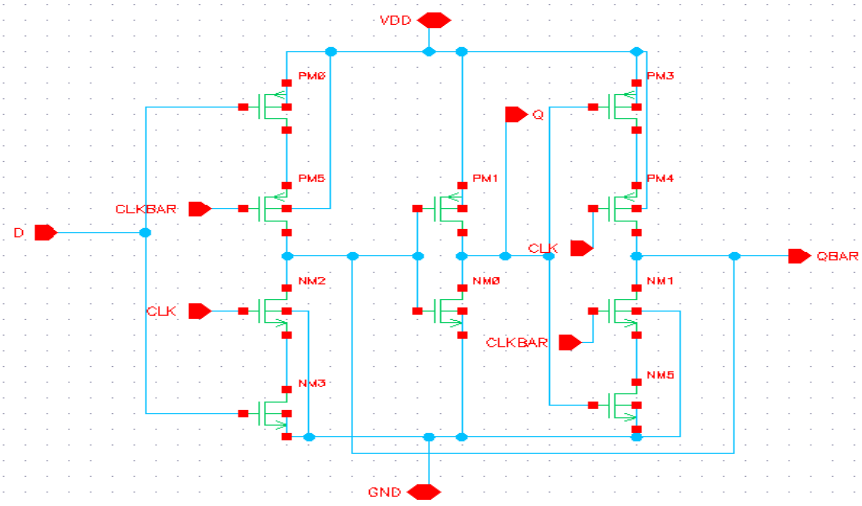

Figure 2. Schematic of D flip flop.

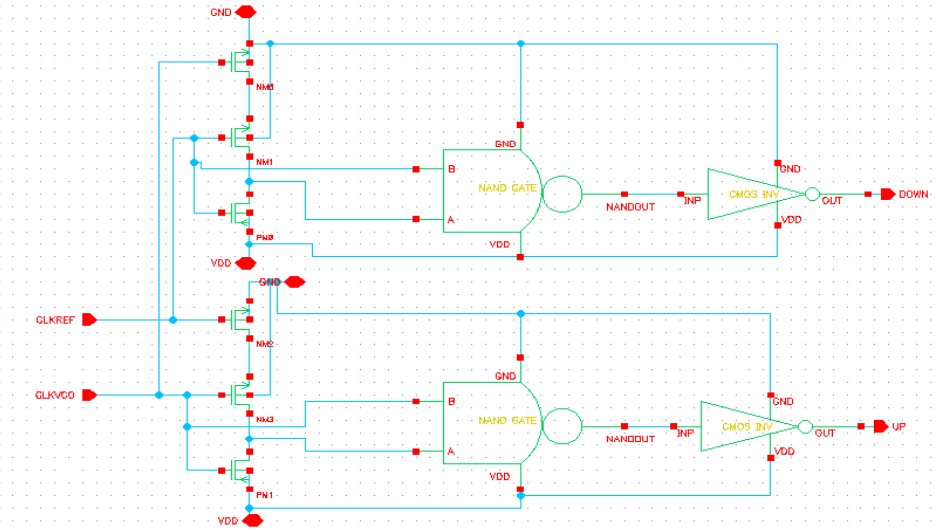

Figure 3. Schematic of Phase frequency detector.

3.2. Charge Pump and Low Pass Filter

The charge pump block in Figure 4 converts the output signals of PFD block i.e., UP and DOWN signals into a voltage that controls the VCO or $V_{control}$. This block also gives a constant voltage to hold the VCO at as the loop locks in at a particular frequency. When the UP signal is high, the positive current I_{PDI} flows through the circuit and increases the control voltage, When the downstream signal goes high, a negative I_{PDI} current flows through the circuit, which reduces the control voltage [10]. The output current of the charge pump is given below Equation (1):

$$I_{PDI} = K_{PDI} \times \Delta\varnothing \tag{1}$$

where,

$$K_{PDI} = \frac{I_{PUMP}}{2\pi}$$

$$\Delta\varnothing = \varnothing_{IN} - \varnothing_{REF}$$

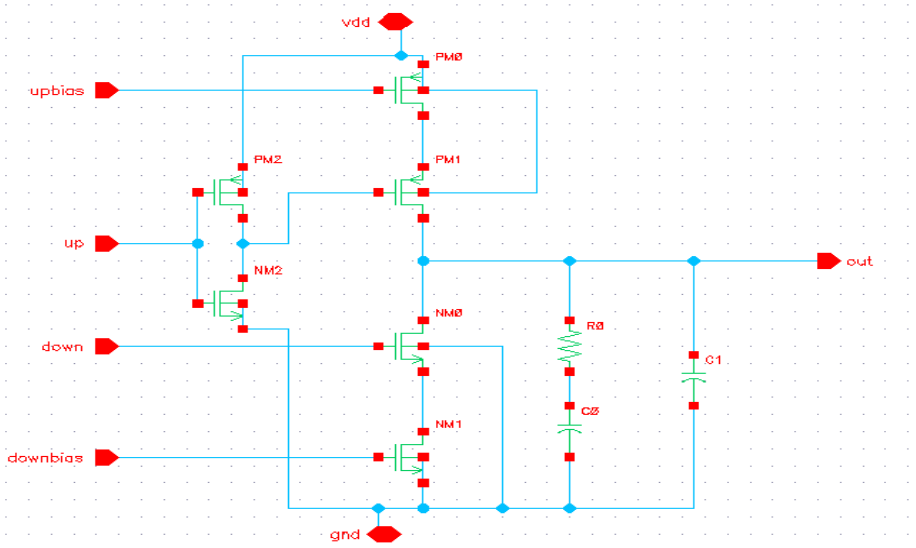

Figure 4. Schematic of charge pump with Low Pass Filter.

The control voltage of VCO is given in Equation (2):

$$V_{ctl}VCO = Kf \times I_{PDI} \quad (2)$$

The Low Pass Filter converts the charge pump current into voltage and the frequency of the VCO depends on the output of the LPF. When the charge pump current is positive, the oscillation frequency increases, otherwise it decreases [11]. Figure 4 shows the implementation of Charge Pump along with Low Pass Filter. Low Pass Filter here is important because it filters out higher frequencies and influences the speed of the circuit [12].

3.3. Voltage Controlled Oscillator

The implementation of a low current VCO circuit that is like a simple ring oscillator with an PMOS and NMOS transistor is done [13]. This limits the current that passes through each inverter, and is thus named a low current VCO. The transistors act as current source sand limit the current to the inverter and the inverter in the next stage is even more starved. This reduced the frequency due to reducing available current and increasing their time to charge and recharge [14]. The schematic of CSVCO is shown in Figure 5.

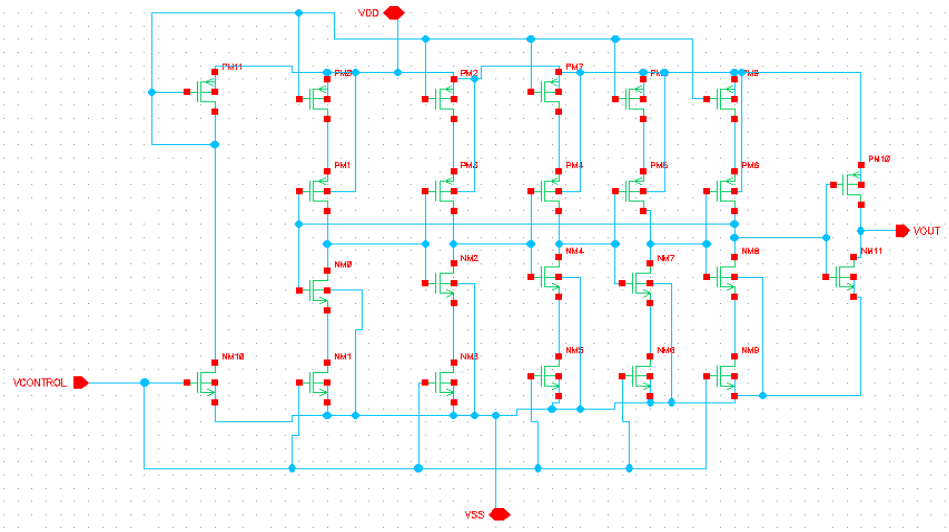

Figure 5. Schematic of Voltage controlled oscillator.

3.4. Frequency Divider

The output of the VCO is provided to the PFD via the frequency divider circuit. The frequency of the VCO output signal is divided by two by this frequency divider block [15]. Two D flipflops constructed using 5 NMOS and 5 PMOS transistors are used to implement the divider circuit, as shown in Figure 6.

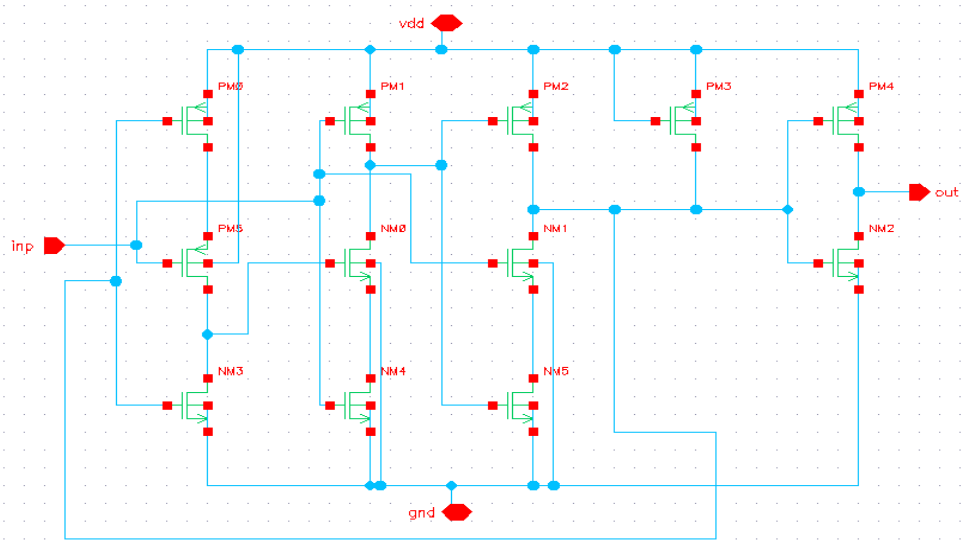

Figure 6. Schematic of the frequency divider.

4. Results and Observations

The design of a PLL is done in cadence virtuoso tool by Analog design environment using 90nm node. Here, the transient and DC analysis of proposed PLL and its blocks are discussed. A reference signal and a clock feedback signal are given as input to the PFD with output as UP and DOWN Signals. The output of the charge pump is given to the VCO, which acts as a Voltage control signal, and the output of VCO is given to a Frequency Divider where the output frequency is N/2, which is the feedback signal given back to PFD. Figure 7 shows the entire design of PLL schematic while Figure 8 shows the transient and DC analysis of the same.

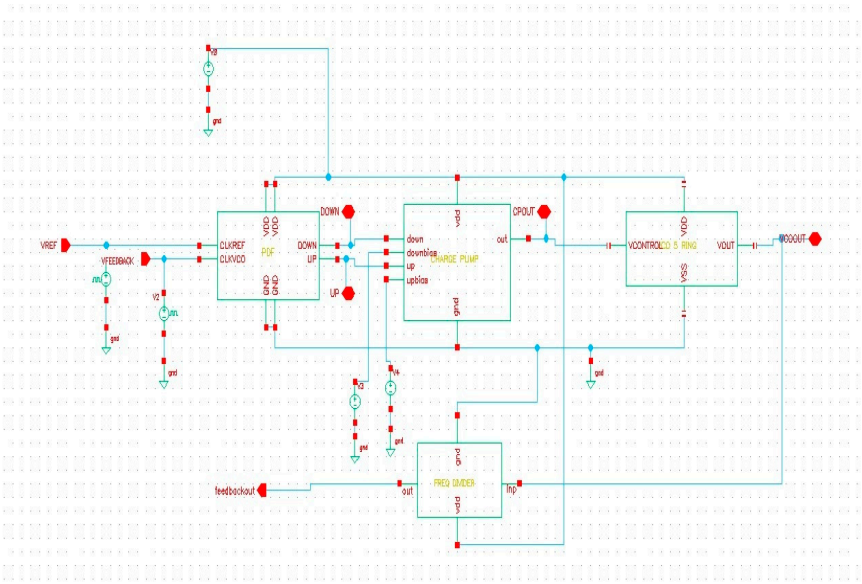

Figure 7. Architecture of Proposed PLL.

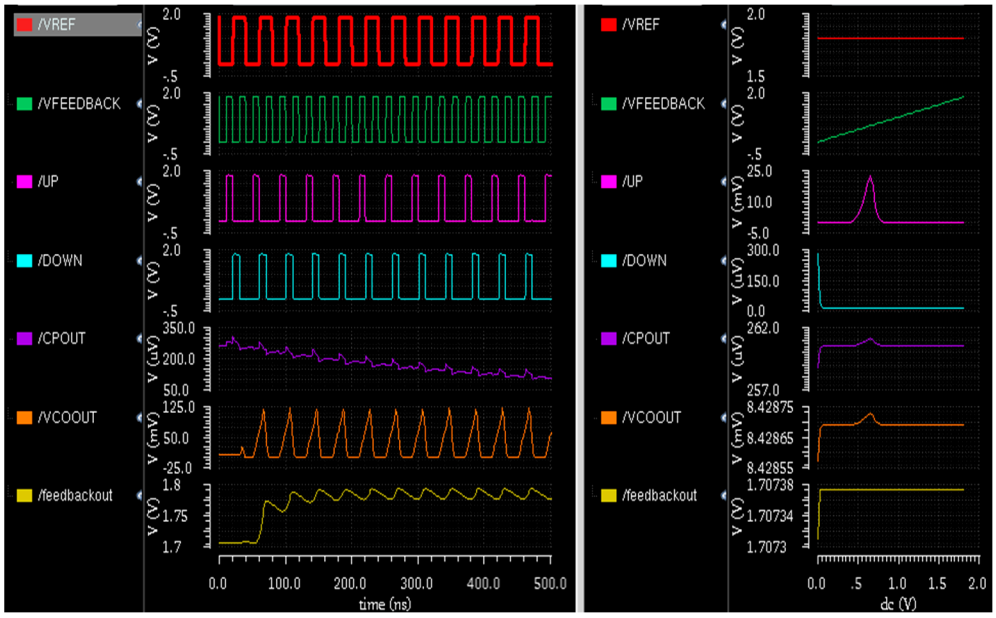

Figure 8. Transient analysis and DC analysis of proposed PLL.

Here, in Figure 7 the use of a novel design for PFD and a charge pump is used for reducing the power usage of whole system and it also shows how they are incorporated in the entire PLL.

Figure 8 shows transient and DC analysis of the proposed PLL that verifies the working of the PLL in an effective way. This not only shows the output PFD, i.e., UP and DOWN signals that act according to the clock signal but also show the output waveforms of the charge pump which varies according to the input signals. When both the input signals i.e., REF and FEEDBACK are high, the output of the charge pump is high; when both the input signals are low, there is a drop at the output signal of the charge pump, which is given as input to the VCO.

Figure 9 shows the two input signals to Charge Pump, UP and DOWN signals red and green respectively which are observed to be inverse of each other. The output signal of Charge Pump is in purple as OUT signal which is given as the input to the VCO as control signal.

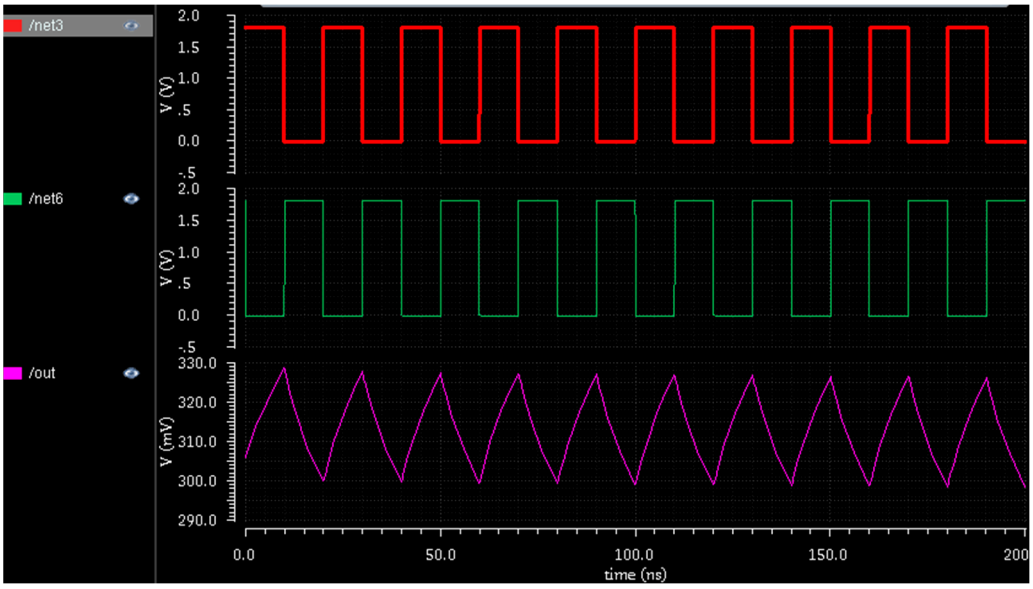

Figure 9. Output Waveforms of Charge Pump.

The output waveforms of VCO are shown in Figure 10 with respect to the input control signal. It shows the frequency of the signal produced by VCO at a constant voltage of $V_{control}$ = 800 mV.

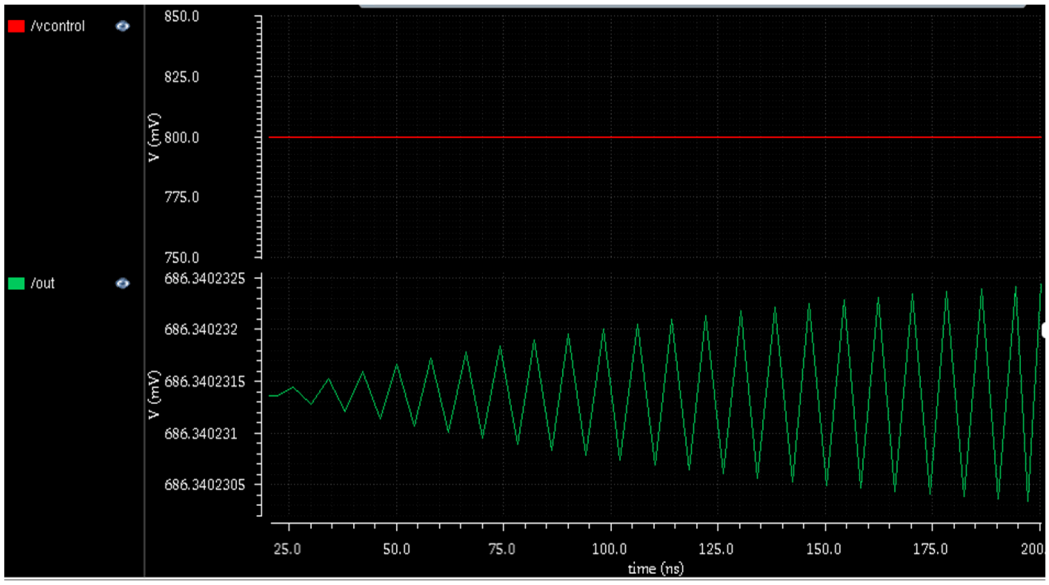

Figure 10. Output waveforms of VCO with $V_{control}$ signal.

Figure 11 shows input and output of the frequency divider. Visibly, the output pulses have half the frequency of the input pulses. In other words, the input frequency is divided by the frequency divider by a factor of 2.

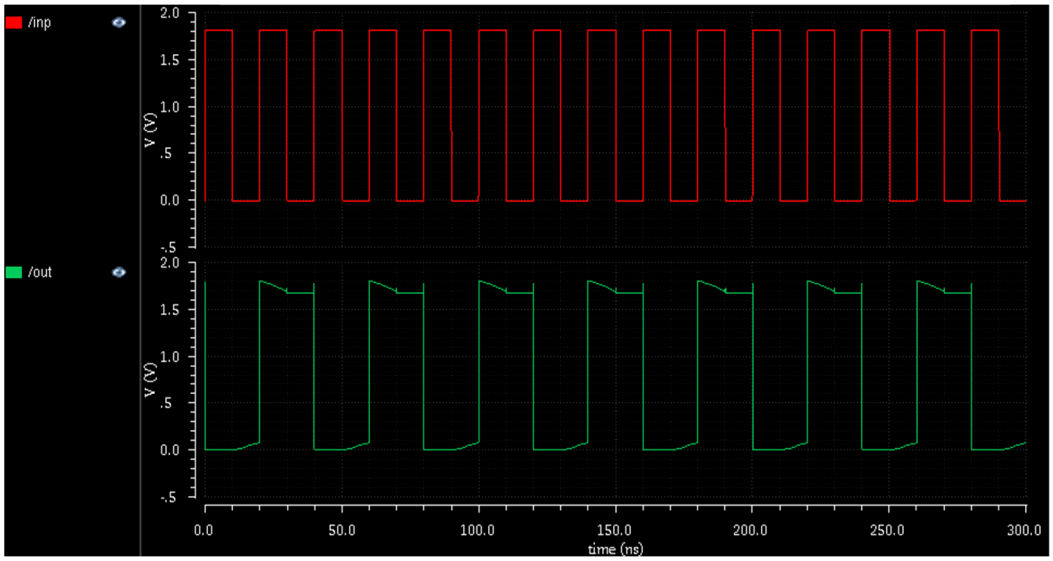

Figure 11. Output wave forms of Frequency Divider.

The DC total power analysis plot of the PLL is shown below Figure 12. The graph peaks at 194.24 µW which shows the total power consumption of the PLL circuit.

The results of the proposed work are better than the results of conventional state-of-the-art PLL design in terms of power consumption and the number of transistors used to design PLL, where power consumption is many times less than that of the conventional PLL. The comparative analysis of various parameters is presented in Table 1.

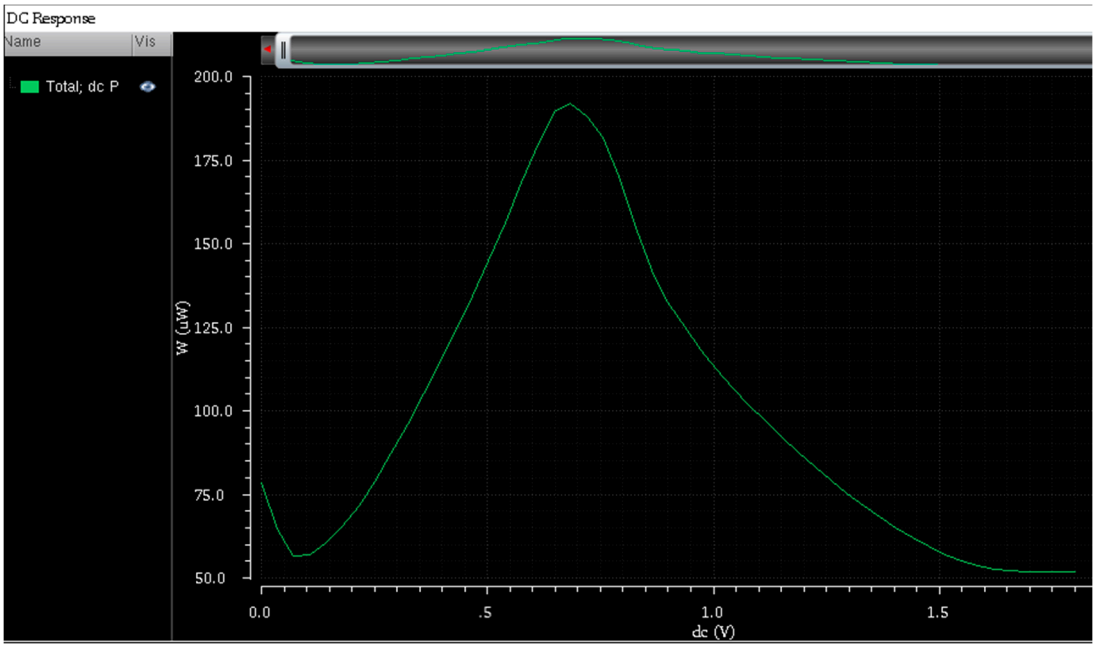

Figure 12. The plot of DC total power analysis.

Table 1. Parametric Analysis.

Parameters	Traditional PLL	Existing PLL	Proposed PLL
Number of transistors	112	56	48
V dd	-	1.8 V	1.8 V
Operating frequency	-	1 GHz	1 GHz
Power Consumption	-	4.2 mW	194.24 μW
Total Power Consumed	High	Medium	low
Technology	180 nm	90 nm	90 nm

Here, the comparative analysis of different parameters is shown. The parameters such as the number of transistors used in design of PLL, supply voltage, and operating frequency power consumed are used to implement PLL, and are analyzed above. From the analysis, the proposed PLL design has a 14% decrease in the number of transistors with a reduced area and 1000 times less power consumption. So, the proposed PLL can be effectively used in low power digital electronic applications and compact devices.

5. Conclusions

A design of PLL using a cadence virtuoso tool in an analog design environment by using GPDK 90nm technology with 1.8 V DC supply is performed. The simulation work presents a reduced number of transistors with a reduced area in proposed design with very low power consumed at DC voltage of 1.8 V. The Total Power Consumed by the proposed PLL design is 194.24micro-Watts. We know that the power consumed, the sizing of the transistors, and the selection of the power supply voltage at different levels may vary with the total power consumed, respectively. This not only allows the working of PLL at high speed, but also supports working at low power, which makes it very effective for low power applications.

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