

RF Transmit and Receive MMIC Front-End for V-Band Inter-Satellite Link [†]

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[†] Presented at the 15th EASN International Conference, Madrid, Spain, 14–17 October 2025.

Abstract

This research focuses on developing, manufacturing and testing a V-band single-chip transmit and receive front-end integrating an LNA, PA and switching functions for ISL terminals. A comparison is made between two technologies: a 60 nm GaN/Si HEMT from MESC and a 100 nm GaAs HEMT from UMS. In Tx mode, targets include 23 dBm saturated power, ≥ 20 dBm at 14 dB NPR and $\geq 5\%$ PAE. In Rx mode, the goal is a 4 dB noise figure. In both cases, the gain must exceed 20 dB across the 59–71 GHz band.

Keywords: V-band front-end; GaN/Si HEMT; GaAs HEMT; low-noise amplifier; power amplifier

1. Introduction

Inter-satellite links (ISL) are being increasingly considered for satellite constellations as they significantly reduce the complexity of the deployment of the ground infrastructure. Optical ISL are starting to be deployed and can offer very high data rates. However, due to the very narrow beams, establishing a link can take a significant amount of time and pointing and tracking mechanisms are very complex. RF-based ISL are potential alternatives in cases where moderate link rates in the order of 1–10 GBit/s are sufficient. In this respect, a V-band is very attractive as it offers a large spectrum and also leads to small antennas. In this paper, we present the design of a V-band transmit and receive single chip front-end integrating low noise amplifier (LNA), power amplifier (PA) and switching functions that are suitable for use in V-band-based ISL terminals supporting at least 1 GBit/s links over a distance of a few thousand kilometers. A comparative evaluation between the performance obtainable in two different technologies is carried out: namely, a 60 nm gate length GaN/Si HEMT technology, as provided by the MACOM Europe Semiconductor Center (MESC) [1], and a 100 nm gate length GaAs HEMT technology, as provided by United Monolithic Semiconductors (UMS). For each technology, the designs of the three basic functionalities composing the TRFE-V (namely the high-power amplifier, the low-noise amplifier and the SPDT switch) will be detailed. For each design, single blocks will be presented, and the circuit-level simulation of each function will be provided. The final layout is then presented as the result of a further electromagnetic simulation/tuning. The goal of Tx mode operation is to obtain 23 dBm saturated output power. The system level requirement is output power equal to 20 dBm min @ 14 dB NPR. The Power Added Efficiency is to be maximized, targeting at least 5%. The goal of Tx mode operation is to



Academic Editors: Spiros Pantelakis,
Andreas Strohmayer and
Gustavo Alonso

Published: 22 April 2026

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minimize the Rx NF, targeting 4 dB. In both cases, the gain shall be greater than 20 dB. The design bandwidth is 59–71 GHz. The simulated results attained with the two technologies are compared and critically assessed for Rx and Tx modes operation.

2. Circuit Design

The design of the MMIC front-end circuit begins with the development of the individual components (HPA, LNA and SPDT), each implemented and optimized with 50 Ω input and output terminations. These building blocks are then integrated to form the complete circuit. This paragraph illustrates the design procedure adopted for each individual component of the MMIC front-end circuit in both technologies, namely the 60 nm GaN/Si HEMT process from MESC and the 100 nm GaAs HEMT process from UMS.

2.1. HPA Design

Several simulations were performed to estimate the achievable power performance of suitable devices' geometries in the bandwidth of interest. Regarding the GaN technology, the drain bias voltage was derated to $V_{DD} = 8$ V, while the gate bias voltage was kept fixed at -1.25 V, corresponding to class AB operation ($I_D = 200$ mA/mm). Considering the power density of the technology, the required output power can be delivered by a single device in the final stage of the HPA, without the need for any power-combining structure. The most suitable device for this purpose was identified as the 4×50 μm transistor. After an extensive linear and nonlinear simulation campaign on the available device peripheries, it was determined that achieving an overall gain exceeding 20 dB requires a five-stage HPA architecture. The last two stages should be implemented using the 4×50 μm device, whereas the first three stages should rely on the 2×50 μm device.

In contrast, for the GaAs technology, the drain bias voltage was derated to $V_{DD} = 3$ V from the nominal 4 V, while the gate bias voltage was fixed at -0.125 V, corresponding to class AB operation ($I_D = 110$ mA/mm). Unlike the MESC GaN technology, in this case, a single device cannot deliver the required 25.5 dBm output power at the HPA output, making it necessary to combine several elementary devices in the final stage. After an extensive simulation campaign on the available device peripheries, five-stage architecture was also identified as the most suitable to achieve an overall gain greater than 20 dB. Assuming typical matching-network topologies, it was possible to estimate the device periphery required for each stage and to obtain a reasonable prediction of the overall performance, including the efficiency. The resulting HPA architecture employs a 4×20 μm device in the first stage, a 6×30 μm device in the second stage, an 8×50 μm device in the third stage, two 8×50 μm devices in the fourth stage, and a combination of four 8×50 μm devices in the final stage. The HPA layout of the MMIC for both the GaN and GaAs technologies is shown in Figure 1.

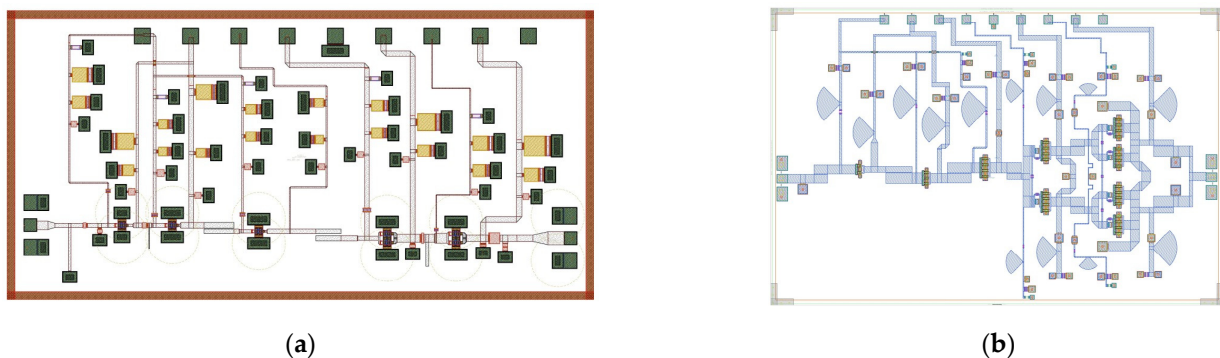


Figure 1. (a) GaN HPA layout and (b) GaAs HPA layout.

2.2. LNA Design

For both the GaN and GaAs LNAs, a preliminary analysis of the optimum device size and bias point for low-noise operation was carried out by evaluating the Minimum Noise Measure ($M_{\min}$) for several gate peripheries. In both technologies, the drain-to-source voltage was set to the lowest value for which the model is validated by measurements. In the GaN technology, the gate-to-source voltage corresponding to low-noise operation is approximately equal to 23% of the device's maximum current. Under these conditions, the optimum behavior is achieved with a device featuring a Unit Gate Width (UGW) of 20 μm . The number of fingers shows only a mild influence on the Noise Measure performance; therefore, a 2-finger device was selected, as larger devices introduce significant parasitic effects that reduce practical usefulness at the V-band, especially in terms of the position of the optimum terminations (Γ_{opt}). Based on the available gain, the minimum 20 dB overall gain requirement can be satisfied with a four-stage architecture [2].

For the GaAs technology, the gate-to-source voltage corresponding to low-noise operation is approximately equal to 12% of the maximum current. In this case, the optimum behavior is obtained with a device with a Unit Gate Width of 30 μm . Similarly to the GaN case, the number of fingers only mildly affects the Noise Measure performance, so a 2-finger device was selected, since larger peripheries would result in increased parasitics and therefore poorer practical behavior at the V-band, particularly in terms of Γ_{opt} . The LNA layout of the MMIC for both the GaN and GaAs technologies is shown in Figure 2.

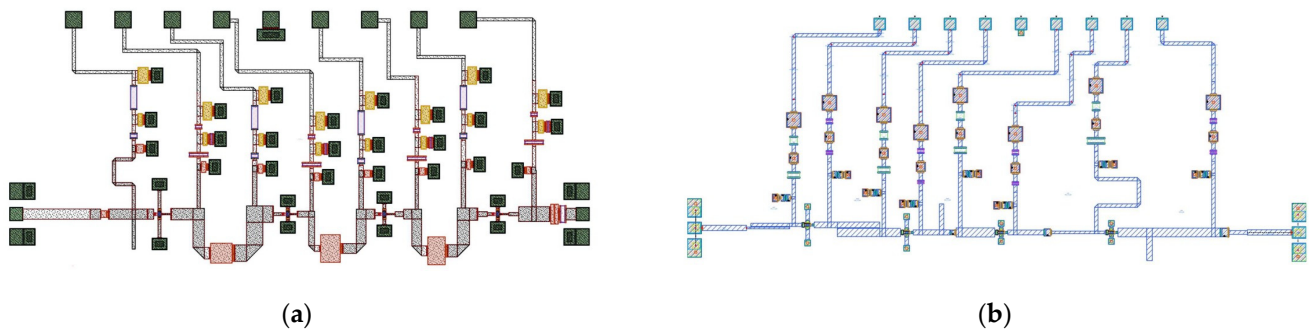


Figure 2. (a) GaN LNA layout and (b) GaAs LNA layout.

2.3. SPDT Design

The single-pole double-throw switch adopts a shunt FET configuration in combination with a quarter-wavelength transmission line. In this topology, the input terminal of the switch is connected to two branches, each incorporating a quarter-wavelength transmission line. At the end of each line, a transistor is placed between the line and ground. When the transistor is in the on-state, it presents a low impedance to the ground, which is transformed by the $\lambda/4$ line into a high impedance at the input—effectively isolating that branch. On the opposite branch, the transistor remains in the off-state and is impedance-matched to the transmission line using a parallel stub, implemented with an additional section of transmission line. This shunt stub enhances the isolation of the off-state branch, further improving the switch's overall performance. For the GaN technology, a control voltage of +0 V was selected for the ON state, while -10 V was chosen for the OFF state. For the GaAs technology, the selected control voltages are 0.8 V for the ON state and -6 V for the OFF state. The choice of a positive voltage for the ON state, instead of 0 V, was made to reduce the insertion loss. The SPDT layout of the MMIC for both the GaN and GaAs technologies is shown in Figure 3.

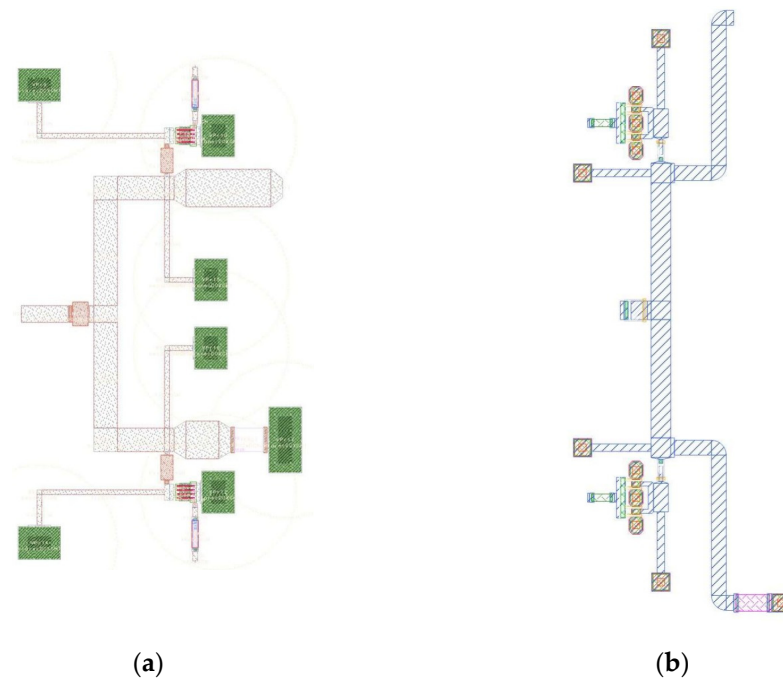


Figure 3. (a) GaN SPDT layout and (b) GaAs SPDT layout.

3. Layout and Simulated Performance

After designing the subsystems as standalone functional blocks, they were subsequently integrated to form the complete MMIC. Figure 4 shows the circuit layout implemented in both technologies. The two circuits are shown to scale to allow for a direct visual comparison of the device dimensions. As can be seen, the GaN MMIC occupies nearly half of the area of its GaAs counterpart.

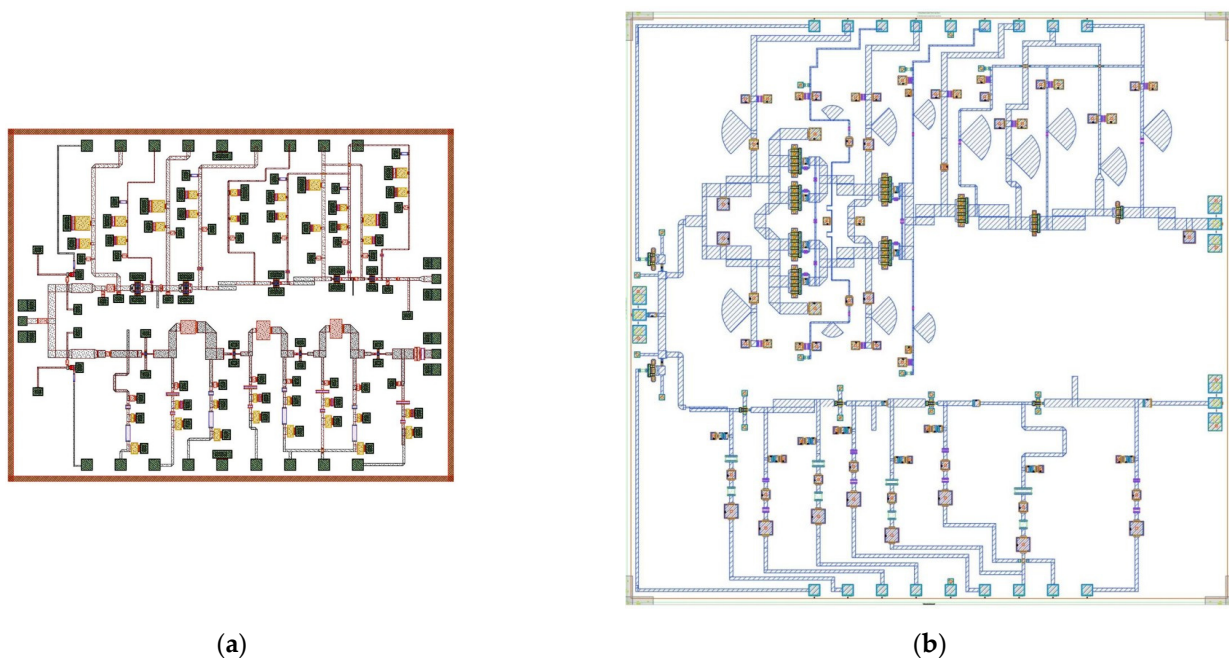
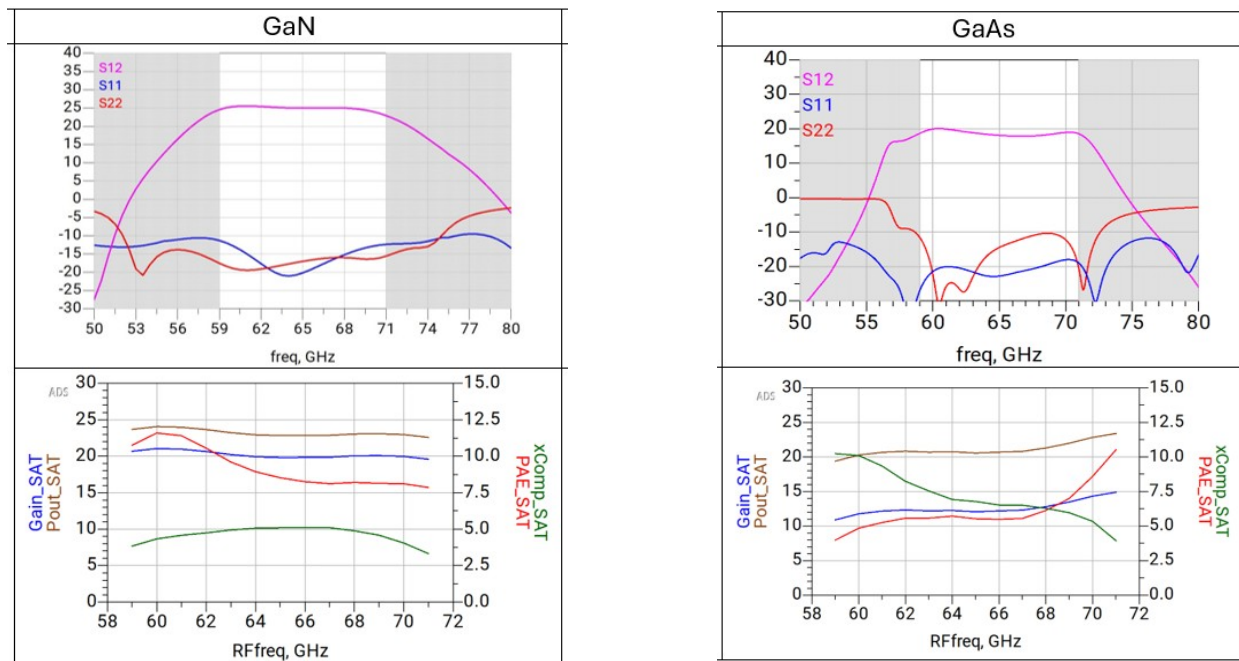


Figure 4. (a) GaN layout and (b) GaAs layout.

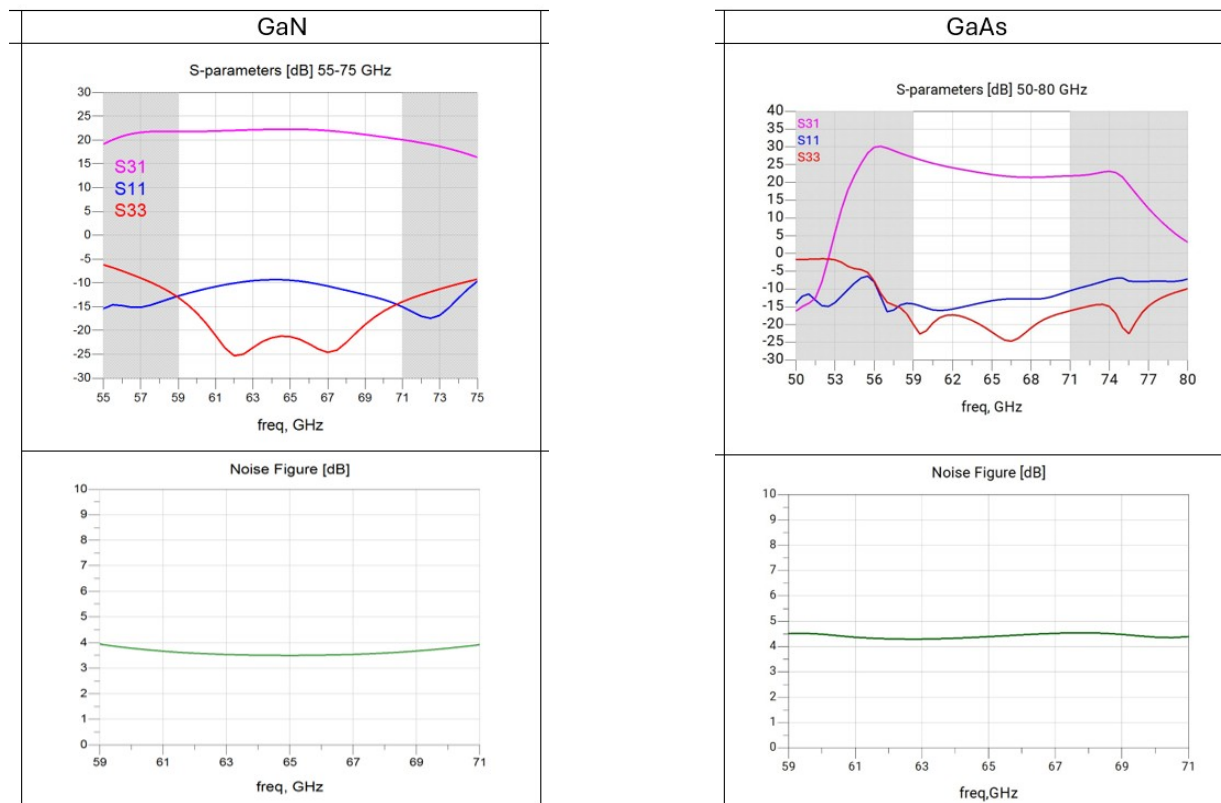
Figures 5 and 6 report on the linear behavior in Tx mode and Rx mode, expressed in terms of S-parameters focusing on the operating bandwidth 59–71 GHz. The critical performance for Tx and Rx modes are also reported. For RX behavior, this parameter is the noise figure, and for Tx, the parameters are output power (Pout) and PAE.



(a)

(b)

Figure 5. (a) GaN Tx performance and (b) GaAs Tx performance.



(a)

(b)

Figure 6. (a) GaN Rx performance and (b) GaAs Rx performance.

An analysis of the data presented reveals a clear advantage for the GaN solution over the GaAs solution. Although the gain levels of both solutions are comparable in transmit (Tx) and receive (Rx) modes, the GaN solution demonstrates a better noise figure (with

typical in-band values of 3.5 dB compared to 4.5 dB for GaAs). In Tx mode, the GaN chip readily achieves 23 dBm, while the GaAs version typically reaches 21.5 dBm. Additionally, the GaAs T/R chip exhibits a much lower nonlinear gain, thereby compromising its power-added efficiency (PAE).

4. Discussion

Many examples of GaN SCFEs are provided in the literature in bandwidths higher or lower than the V-band [3,4]. However, GaN and GaAs contributions at the V-band are very rare to find. Table 1 is provided in this section to comparatively evaluate this work with the literature, focusing on a V-band of 50–75 GHz.

Table 1. State-of-the-art table TR MMICs, focusing on V-band of 50–75 GHz.

Reference	[5]	[6]	[7]	T.W. GaN	T.W. GaAs
Tech.	130 nm SiGe CMOS	130 nm SiGe CMOS	65 nm CMOS	60 nm GaN/Si	100 nm GaAs
Config.	TR Chip	TR Chip	TR Chip	TR Chip	TR Chip
Freq [GHz]	57–67	52–63	57–67	59–71	59–71
$P_{out,TX}$ [dBm]	10.5	7.2	5	20	20
PAE_{TX} [%]	-	15.2	8.7	7	5
NF_{RX} [dB]	7.6	4.6	6.7	3.9	4.5
HPA, V_{DD} [V]	3.3	-	-	8	3
Gain TX-RX [dB]	16.5–20	14.7–14.1	24.5–21.5	20–20	18–18
Area [mm ²]	1.1	0.6	0.22	12.3	27.8

5. Conclusions

A V-band single-chip transmit/receive front end operating over the 59–71 GHz range has been presented. The design methodologies adopted for each MMIC building block—namely the HPA, LNA and SPDT—have been outlined for both technologies, and the final integrated front-end layout along with its performance has been reported. Simulation results highlight a clear performance benefit of the GaN implementation compared to the GaAs one. While both technologies provide similar gain levels in transmit (Tx) and receive (Rx) modes, the GaN design achieves a superior noise figure, with typical in-band values around 3.5 dB versus approximately 4.5 dB for the GaAs counterpart. In Tx mode, the GaN MMIC meets the 23 dBm target, whereas the GaAs version typically delivers about 21.5 dBm. Moreover, the GaAs T/R chip exhibits significantly stronger gain compression, which negatively impacts its achievable power-added efficiency (PAE).

Author Contributions: Conceptualization, G.V., A.R. and M.R.; methodology, all; validation, all; formal analysis, all; investigation, all; resources, E.L.; writing—original draft preparation, G.V.; writing—review and editing, all; visualization, all; supervision, P.E.L. and R.G.; project administration, P.E.L. and R.G.; funding acquisition, E.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by European Space Agency grant number AO/1-11802/23/NL/RK “RF transmit and receive front-end for V-band inter-satellite link” whose support is gratefully acknowledged. The views expressed in this publication can in no way be taken to reflect the official opinion of the European Space Agency.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

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