

Proceeding Paper

Best Practices from the Competence Center for Resource-Conscious Information and Communication Technology—“Green ICT @ FMD”[†]

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Abstract

The “Green ICT @ FMD” competence center brings together the expertise in resource-efficient information and communications technology from 11 Fraunhofer and two Leibniz institutes, which have joined forces to form the Research Fab Microelectronics Germany (FMD). The competence center offers industry a broad portfolio of services focused on the future development of ICT applications, infrastructures, and microelectronic components with a view on resource-efficient production, energy efficiency, and the reduction in greenhouse gas emissions. Various cooperation opportunities have been initiated to support a wide range of companies in responding to customer needs and regulatory requirements through innovative and resource-efficient ideas and developments. We now present the initial results from the success models of the “Green ICT Space” startup and SME program, as well as selected “Validation Projects” with companies that all pursue the common goal of more resource-efficient production and use of ICT.

Keywords: carbon footprint; resource efficiency; energy efficiency; information and communication technologies (ICT)

1. The “Green ICT @ FMD” Competence Center

The resource consumption of information and communication technologies (ICT) will continue to increase in the future due to advancing digitalization in everyday life and the world of work with applications such as IoT, AI, Industry 4.0 and IIoT, among others. The latest research findings assume that the electricity demand of our ICT use will increase from around 50 TWh in 2024 to around 75 TWh by 2033 in Germany. A large part of this will be consumed by data centers, but IoT in households and general telecommunications will also increasingly require higher power consumption, as research groups from the competence center recently predicted [1]. This does not include the electricity consumption required for the actual manufacture of microelectronic components. If the European Chips Act’s target of producing 20% of global microchips in Europe is achieved, the electricity demand of the European semiconductor industry will rise to 47.4 TWh in 2030, which, for instance, would correspond to half of the electricity consumption of European data centers (98.5 TWh) [2]. The chip shortage of 2021–2023 led to a loss of 102 billion euros in German gross domestic product (GDP) and underscores the fact that such bottlenecks must



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be avoided at all costs in the future through technological sovereignty and resilience in supply chains by increasing production capacities [3].

In order to drive digitalization forward, it will be particularly important to record, analyze, and minimize the ecological impact of the manufacture and use of microelectronics. The topic is currently increasingly reflected both in legal requirements for companies in the context of sustainability reporting and in their customer requirements for market advantages and general competitiveness.

The “Green ICT @ FMD” competence center brings together the know-how of 13 cooperating research institutes with expertise in green ICT to support companies in the fields of, but not only, (a) sensor, edge, and cloud systems; (b) communication infrastructures; and (c) microelectronics production in implementing resource-efficient technologies (Figure 1). This enables companies to meet their customer requirements as well as upcoming regulatory requirements, further creating a long-term competitive advantage in Europe.

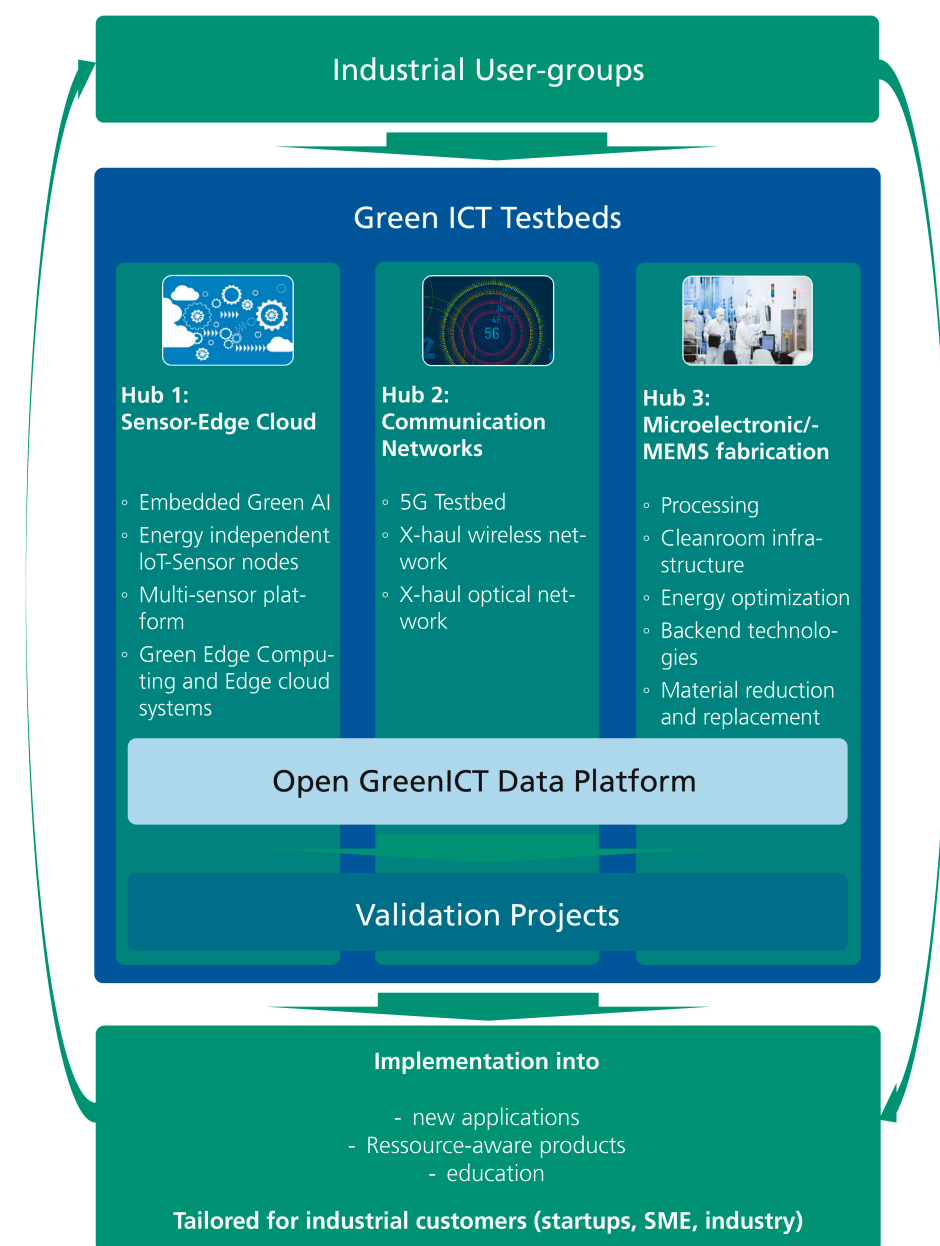


Figure 1. The three technology hubs and the specific offer for participation in validation projects within the research project “Green ICT @ FMD”.

The “Green ICT @ FMD” competence center has created a framework that enables start-ups and SMEs to incorporate green thinking into their development processes from the outset. The program supports start-ups and SMEs by improving their technological readiness level (TRL), demonstrating their technologies in real cleanroom environments, and improving transparency with regard to regulatory requirements and customer expectations by conducting environmental assessments of their technologies and products. Although companies’ exact motivations can vary, the program has already enabled numerous companies to successfully demonstrate their technologies, test and improve them, and even be acquired by others. The program has also provided them with insights to help them prepare their sustainable technologies from lab to market.

The framework focusing on industrial required assistance consists of two main parts, “Green ICT Space” and “validation projects”, which we explain in more detail as follows. Furthermore, we provide insights into some of these projects, highlighting the motivation and goals of each project and presenting initial results.

2. The “Green ICT Space” Success Model—Accelerator for the Green ICT of Tomorrow

The “Green ICT Space” allows start-ups and SMEs to benefit directly from FMD’s infrastructure and green ICT expertise. For example, they can test their technology in real cleanroom environments and assess their product’s or processes’ carbon footprint, or have microelectronics components with sustainable approaches manufactured.

In the following section we give a brief overview on two recent projects of “Green ICT Space”. One addresses the reduction in resource consumption in manufacturing of microelectronic components and the other focuses on energy savings of servers during their use phase.

2.1. A Screening Tool That Enables the Reduction in Test Wafers Used During Production

To verify the quality of individual process steps in microelectronics production, so-called control wafers are typically processed in parallel with the final target wafers. These control wafers must be evaluated and inspected to protect the entire production from potential defects or other undesirable phenomena that could destroy the entire production batch. Such inspection processes are usually time-consuming, and the additional number of test wafers required for complete process control and stability entails extra environmental and cost impacts on the final product. Therefore, it would be economically and ecologically advantageous if an inline process control were available to reduce the number of control wafers and ensure process quality directly on the target wafer. DIVE imaging systems GmbH develops innovative inspection tools that combine the advantages of optical spectroscopy with image capture. AI algorithms make the process steps in semiconductor manufacturing more comprehensively controllable. The non-destructive and high-precision inspection technology can be used for quality control of wafers and leads to the saving of control wafers. As part of the environmental potential analysis, the advantages of using DIVE technology were compared with the state of the art, with a particular focus on the energy input per wafer. For an exemplary 28 nm process (CMOS, front-end), around 700 process steps were assumed for production, including approx. 400 process steps for wafer processing (etching, lithography, deposition) and approx. 300 accompanying metrology process steps (Figure 2).

The use of 36,000 control wafers was assumed for 25,000 wafer starts/month, and the savings potential achievable through DIVE technology was initially conservatively estimated at 25% of the control wafers (9000 wafers/month). By using DIVE’s hyperspectral vision technology, it was calculated that more than 118 tons of CO₂ can be saved every

month. The reduction in the CO₂ footprint takes into account additional energy costs for the manufacture and operation of the DIVE system. This corresponds to a reduction of around 2% of the monthly Fab power consumption and CO₂ footprint. In addition to these savings, there are numerous other direct and indirect savings that have not been examined in detail. These are listed as follows:

- Early detection of process deviations and thus savings on production errors and improving the yield of the production wafers.
- Reduction in tool allocation through control wafers or operational savings from dedicated tools that are used exclusively for processing control wafers.
- Energy savings resulting from the elimination of the processing steps for control wafers.
- Reduction in the consumption of chemicals and water required for the preparation of control wafers, in particular the use of concentrated mineral acids.

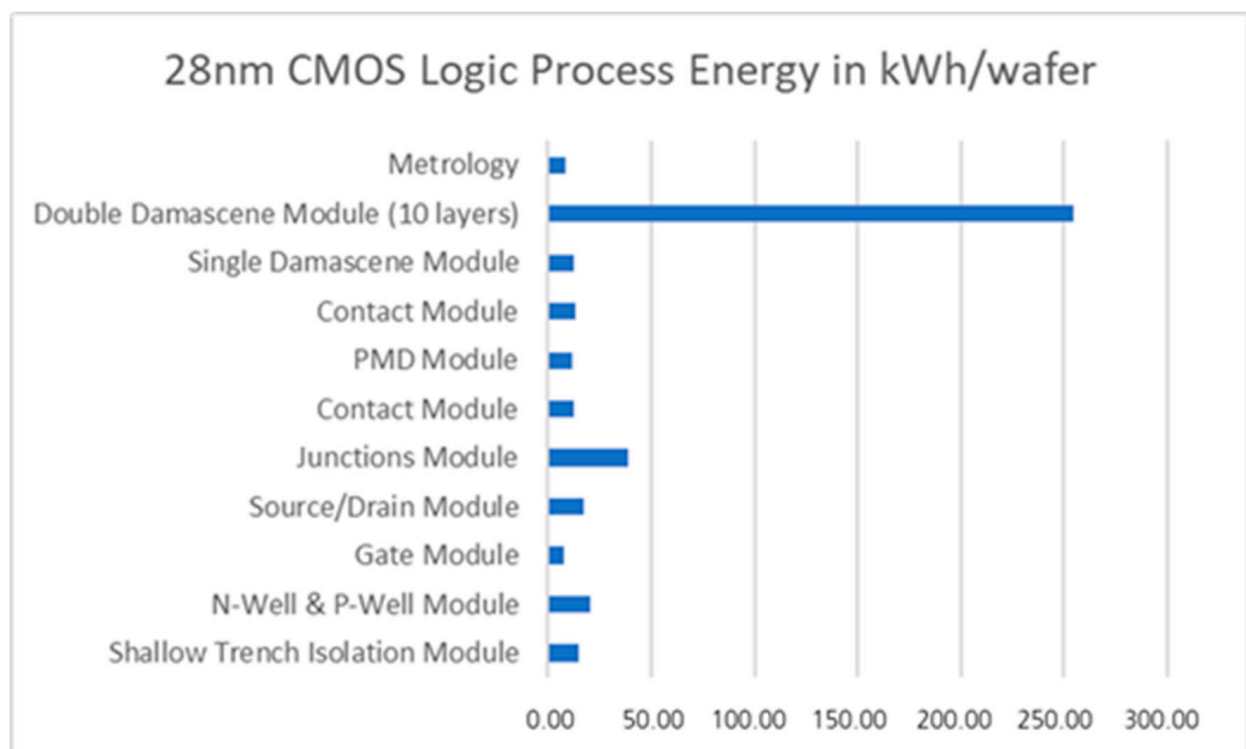


Figure 2. Consumption of electrical energy (in kWh) per wafer in the 28 nm CMOS process.

The results show that the implementation of the innovative inline inspection tool from DIVE imaging systems GmbH offers much greater scope to further reduce the environmental impact of manufacturing processes of microelectronic components. Testing and prototyping opportunities based on this tool are available in the 300 mm cleanroom of Fraunhofer IPMS in Dresden and can particularly be applied for industrial R&D purposes.

2.2. Alternative Cooling Systems for Servers That Allow for Waste Heat Utilization

In a joint collaboration, XCCES GmbH and Fraunhofer IZM demonstrated how an innovative, solder-based solution could be used to make server systems more resource-efficient and save energy. The project aimed to research and test an innovative, comprehensive solution for hot water cooling of server systems deployed in data centers. Conventional water-cooling solutions use thermal paste and place cooling units directly on the CPU. The project's innovation lies in the use of soldering technology to connect the water cooling directly to highly stressed server components such as the GPU, CPU, power supply units, and RAM. This can raise the cooling water temperature by up to 6.5 K compared to con-

ventional thermal paste without restricting the performance of the IT components. To test the innovative water-cooling system, a model depicting state-of-the-art server components was defined (see Table 1).

Table 1. Selected server component assembly for measuring the potential energy savings possible with the solder-based water-cooling solution.

Component	Type
Server Case	2HE AMD Dual-CPU RA2212-ASEPGN
CPU	2 × AMD EPYC 9274F
GPU	NVIDIA Quadro RTX A4000
RAM	16 × ECC Reg Micron DDR5 4800 RAM
Hard Drive	800 GB Kioxia CM6-V U.3 NVMe SSD

A comparison of the thermal performance of solder and thermal paste shows that temperatures are 12–23% lower when solder is used compared to thermal paste (see Figure 3). Neither material shows any signs of degradation after 1500 h of thermal cycling between -40 and 125 °C. Following the optimization and measurement of an innovative water-cooling system incorporating soldered heat sinks on a server system, a CPU-to-liquid thermal resistance of 0.040 K/W is possible, along with a minimum temperature difference of 4.9 K between the inlet and outlet at a cooling capacity of 750 W. Potential energy savings of 32% (380 kWh) per server per year are calculated by applying the solder-based water-cooling system.

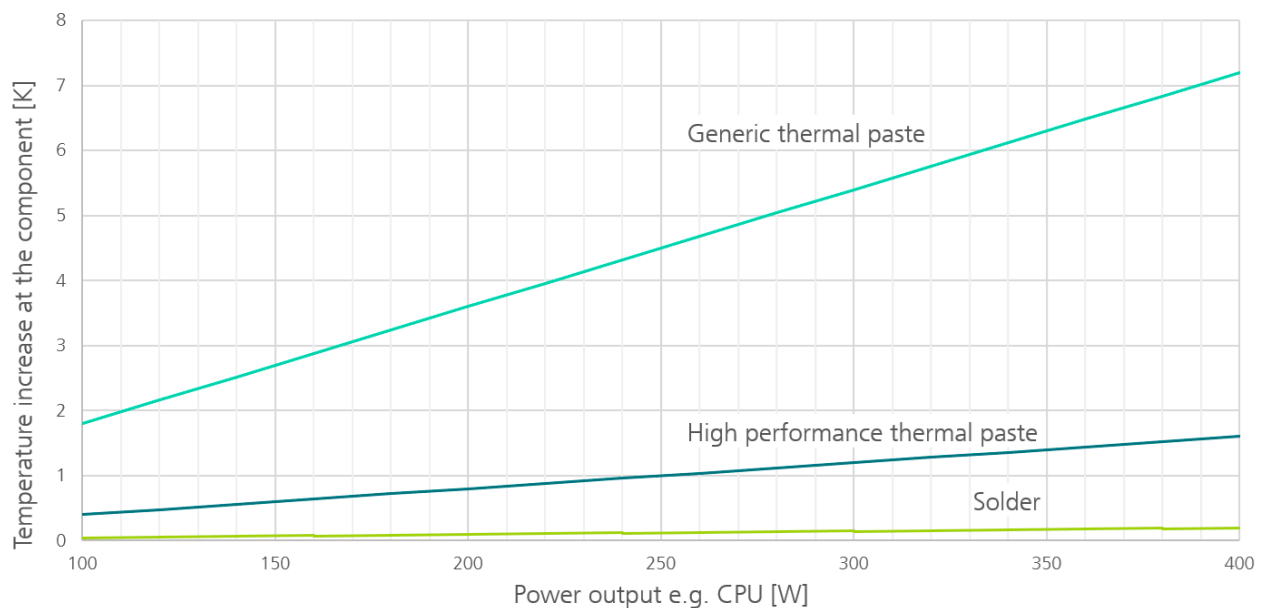


Figure 3. Comparison of temperature increase at the component depending on the power output of the server for generic and high-performance thermal paste.

2.3. Alternative Cooling Systems for Servers That Allow Waste Heat Utilization

There are currently still ongoing R&D projects, and new findings on topics, such as biofunctionalized photonic sensor chips, alternative remover solutions as substitutes for harmful substances, special die separation processes and specific circuits for controlling, e.g., microvalves in medical applications, will be published soon.

3. Successful Model: Validation Projects—Ecological Improvements to Established Products and Processes

In addition to the Green ICT Space, so-called validation projects have been assessed within the research project to enable existing products, processes and procedures to be improved and benchmarked with regard to their ecological effects and impact. Below, we provide a brief overview on various completed projects and where additional information is available.

3.1. Analysis of the Carbon Footprint of Self-Powered, Wireless Sensors

Wireless sensor nodes are typically supplied with electrical energy via batteries or, alternatively, through energy harvesting from their immediate environment. Examples of such kinds of available energy resources in the environment include light, temperature differences, deformations, or vibrations.

To answer the question of which type of energy-harvesting system has the lowest environmental impact for a particular sensor application, we investigated different scenarios and assessed the carbon footprints arising from the production of all the components of the energy supply systems. In our test scenario, data is transmitted every 15 min or every 5 min. This results in average power requirements of 400 and 790 μW , respectively, which must be provided by the energy supply system. For the energy supply, we compared a primary battery, a solar cell (PV) (500 lux over 8 h a day), and a thermoelectric generator (TEG) with a 10 K temperature difference. The components of the various sensor nodes were grouped into categories, the share of which in the overall carbon footprint is shown in Figure 4. Component categories with a share in less than 5% were combined and include capacitors, resistors, inductors, supercapacitors, LEDs, crystals, transistors, antennas, screws, transformers, and thermal interface materials (TIMs). In some cases, this also includes diodes, nylon, and the TEG.

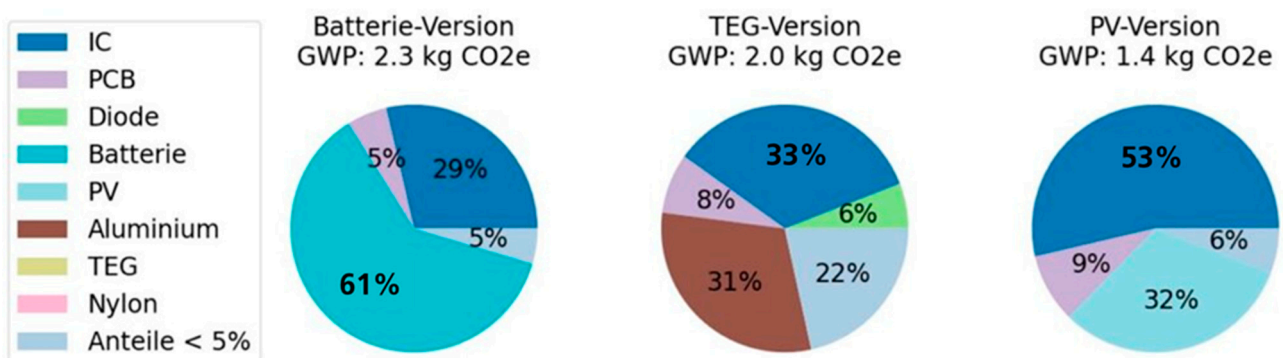


Figure 4. Carbon footprints for different energy supply technologies (15 min data transmission setup).

Figure 5 shows the carbon footprint of the two-use cases as a function of the planned lifespan. As can be seen, the battery-operated wireless sensor has a higher carbon footprint than the PV solution after approximately 3.5 years, exceeding that of the TEG solution after 7.5 years for the 15 min data transmission setup (dashed lines). The higher energy demand of the 5 min data transmission setup causes the intersection of the carbon footprints to occur approximately six months earlier for PV and about one year earlier for TEG (solid lines). This is because, in both setups, the PV module has a lower carbon footprint per microwatt of power than the TEG.

Overall, our findings show that using a solar cell instead of a primary battery for a wireless sensor with a power consumption of 800 μW and a lifespan of 10 years can reduce the carbon footprint by 50%, provided an illuminance of 500 Lux is available for 8 h per day.

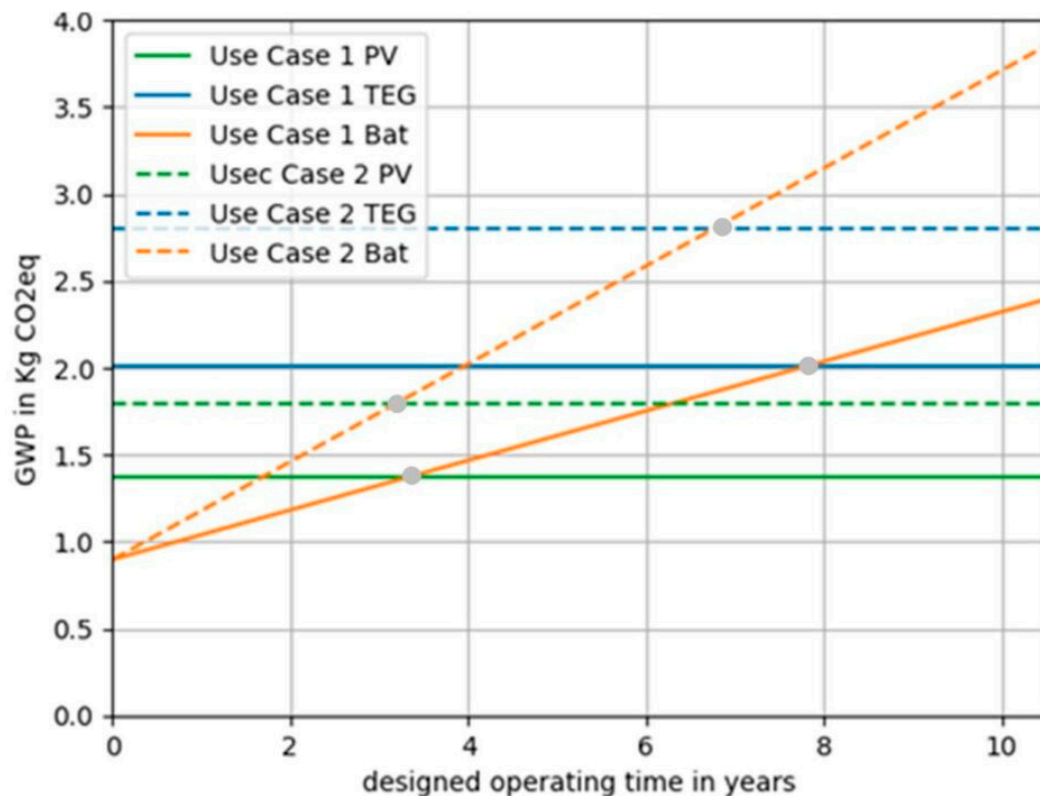


Figure 5. Carbon footprint of the use cases for each energy harvesting method compared with a battery supply.

3.2. Traffic-Forecasting-Based Dynamic Link-Capacity Adjustment for Optical Networks

The large number and variety of emerging online services, along with the resulting user- and machine-generated data traffic, are leading to an ever-increasing demand for bandwidth in the underlying optical transport infrastructure. Dynamic capacity allocation enables optical networks to efficiently adapt to constantly changing traffic demands, ensuring that resources are allocated when and where they are needed. In addition to improving network operational efficiency, dynamic allocation also contributes to cost savings by maximizing the utilization of existing infrastructure and reducing operational expenditure costs linked to the energy consumption of the underlying optical network. One promising approach to autonomously and dynamically allocating/adjusting link capacities is to forecast future traffic behavior efficiently and accurately in terms of expected intensity and variability over time. One particular technology is the Temporal Fusion Transformer (TFT), which is an attention-based deep neural network (DNN) optimized for multi-step forecasting. The ability to predict multiple steps ahead is particularly important for adjusting the capacity of optical links, given that reconfigurable optical components, such as transponders, require tens of seconds to several minutes to adapt the various hardware settings to the new link throughput. Figure 6 shows the dynamic adjustment control loop developed by Fraunhofer HHI to adjust the link capacity based on traffic forecasts, automating the provisioning of capacity for an optical transponder acting as a gateway between optical access and metro networks [4].

The transponder can be configured for network port rates between 100 G and 200 G, and feeds traffic from an aggregation switch into the optical transport network via a reconfigurable optical add-drop multiplexer (ROADM). A programmable traffic generator connected to the aggregation switch generates bursty and cyclic traffic flows, with aggregated data rates ranging from 0 to 200 G, emulating real traffic flows collected over a 12-week period. These flows exhibit the so-called daily tidal effect, manifesting as low

traffic intensity during the night and early morning, steadily increasing and peaking during the midday and afternoon, and gradually decreasing in the evening and night-time. Firstly, the generated traffic is monitored at the switch level with 3 s granularity (Figure 7a, green curve), while traffic peaks are calculated every minute to produce a traffic envelope curve (Figure 7a, yellow curve). Secondly, a TFT model was trained offline based on the traffic envelope and then integrated into the online ML pipeline for real-time traffic forecasting. As shown in Figure 7a, the traffic forecaster predicts the next five traffic maxima (based on the previous 30 maxima), which correspond to the next five minutes (more than enough time for the transponder's new capacity configuration). While the traffic forecaster can correctly predict overall traffic evolution, it still presents a challenge to foresee some traffic bursts accurately, as these are typically random and specific to traffic outliers. Thirdly, the future required capacity is computed based on the predicted traffic envelope (Figure 7a, blue curve). When the current value of the transponder's network interface capacity (Figure 7b, red curve) deviates from the planned capacity, the transponder is reconfigured to match the scheduled capacity. This value is queried through periodic telemetry. Finally, capacity overprovisioning is calculated every minute based on the difference between the current capacity value and the traffic volume/envelope (Figure 7b, blue bars).

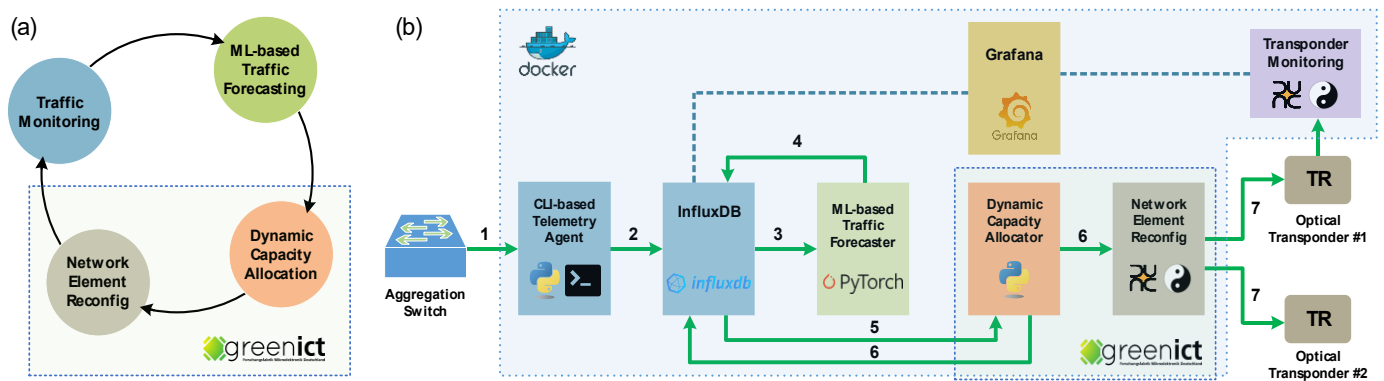


Figure 6. (a) Control loop for the dynamic link-capacity allocation/adjustment. The main steps include traffic monitoring and streaming (1) for real-time ML-based traffic forecasting (2). Based on the predicted future traffic values, the capacity is dynamically adjusted (3) and the transponder's network port-capacity is reconfigured accordingly (4). (b) The various software components of the capacity adjustment pipeline that implement the control loop functions, consisting of the telemetry framework for the extraction and storage of telemetry data, the ML module for traffic forecasting, as well as the capacity allocator/scheduler and transponder reconfiguration modules. The Grafana dashboard is used to visualize the operation of these different components in real time.

To illustrate the visual performance comparison, Figure 7c shows the overprovisioning values obtained using a dynamic link-capacity allocation scheme (blue bars), compared with conventional static link-capacity provisioning (red bars). It should also be noted that, in some cases, a short delay between the scheduled and actual capacity values may be observed due to hardware-related delays and jitter occurring during link-capacity reconfiguration.

3.3. Further Ongoing Validation Projects

Additional R&D projects will soon publish new findings, for example on the recyclability of special chemicals used in wafer production, the ecological impact of individual components in special printed circuit boards, and possible energy savings from replacing specific components in existing machines.

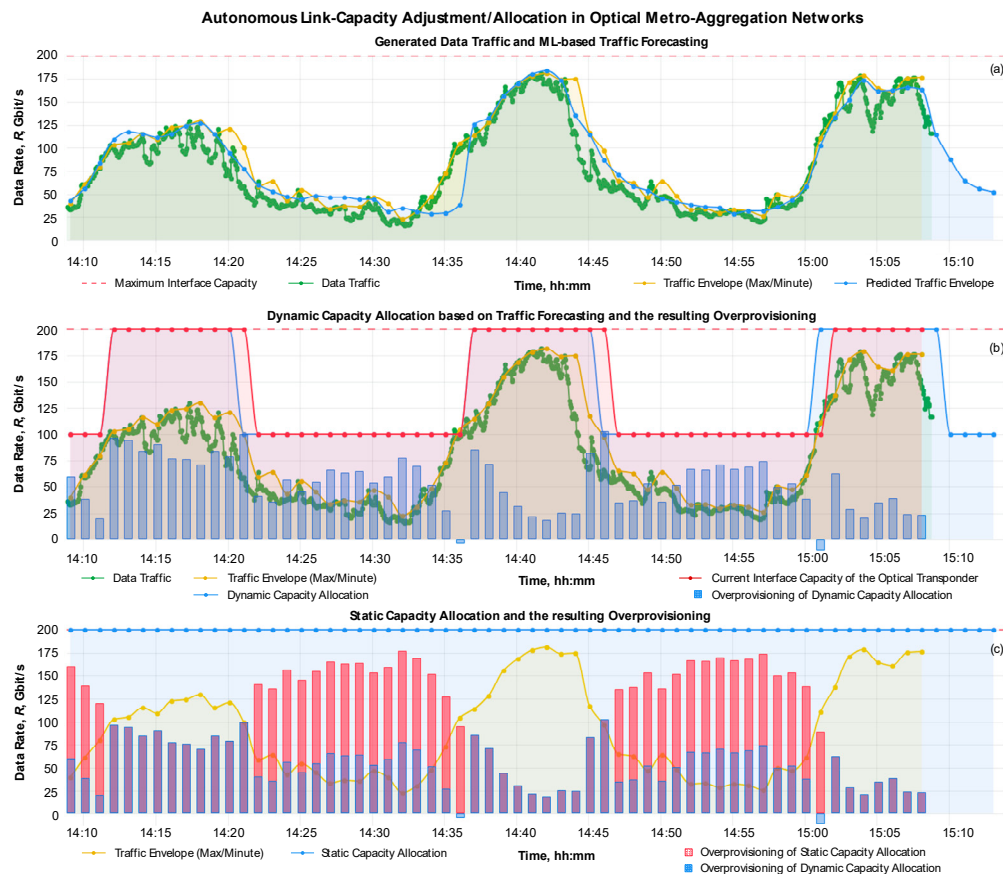


Figure 7. (a) Generated bursty and cyclic traffic with a 3s granularity of traffic sampling (green curve), computed traffic envelope (yellow curve), and forecasted envelope/traffic evolution (blue curve). (b) Dynamic adjustment of link-capacity (scheduled capacity (blue curve), and actual capacity (red curve) of the transponder's network interface), and overprovisioning values (blue bars). (c) Static/fixed link-capacity at 200G (blue curve) and the comparison of overprovisioning values for dynamic (blue bars) vs. static (red bars) capacity allocation schemes.

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