

Proceeding Paper

Cryo-PMOS Hardware Towards Energy Efficient Neuromorphic Systems [†]

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Abstract

The current work proposes a novel idea of exploration of the standard 180 nm-based bulk CMOS technology operating under cryogenic temperatures to achieve energy-efficient and high-speed computation. A PMOS chip of 180 nm technology is fabricated and is explored for synaptic memory applications by operating at 4 K temperatures. This proposed approach offers numerous advantages in terms of enhanced charge carrier mobilities, reduced power dissipation, and seamless integration with standard CMOS technology. The fabricated PMOS under cryogenic temperatures exhibits pinched hysteresis characteristics, confirming the memory retention capability with very low set and reset voltages. Next, synaptic functional measurements were performed by applying constant pulse trains at the drain terminal to understand the human brain's learning and memory retention capabilities.

Keywords: cryogenic; neuromorphic; PMOS; energy efficient; synaptic; memory; artificial intelligence

1. Introduction

With the rapid advancement of artificial intelligence (AI) and machine learning technologies, the demand for novel energy-efficient and high-speed computational capacity is drastically rising [1]. The conventional Complementary Metal Oxide Semiconductor (CMOS)-based technology is nearly approaching its physical and performance limits in terms of device scaling, reduced switching efficiency, increased leakage currents, excessive thermal dissipations, and sizing of transistors [2]. To effectively address the challenges with CMOS technology, a new emerging technology, namely, neuromorphic computing, which is inspired by the human brain, has emerged as a potential viable alternative for the implementation of next-generation computing systems [3]. These neuromorphic computing technologies typically operate in an event-driven approach and offer massive parallel processing capability analogous to the information processing in a distributed network inside the human brain [4]. On the other hand, cryogenic technology is also one of the emerging technologies to improve the overall performance of the devices, owing to the operation of the devices in cryogenic temperatures, offering enhanced carrier mobility, reduced thermal noise, and minimized leakage currents. Integration of cryogenic and neuromorphic technology enables us to achieve exceptional improvement in terms of power consumption and speed [5]. Further, this hybrid integration is compatible with the traditional CMOS technologies, offering new routes to achieve an ultra-low power, scalable,



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and energy-efficient neuromorphic hardware suitable for implementations of complex machine learning algorithms for the next generation of AI technologies.

2. Experimental Setup

The measurement platform comprised a packaged IC fabricated in TSMC 180 nm bulk CMOS that integrates a PMOS “farm” behind an on-chip serial shift register, as previously described [6,7]. Devices were addressed by shifting a serial bitstream that selects the target transistor geometry (W/L). The bitstream was routed via a micro-D connector to a cryogenic PCB mounted in a pulse-tube cryostat, and DC characteristics were acquired with a source–measure unit (SMU). For pulsed experiments at 4 K, the gate was driven by a pulsed SMU channel while the drain–source path was monitored on a second channel. We investigated a short-channel, narrow-width device ($W/L = 0.22 \mu\text{m}/0.18 \mu\text{m}$), quantifying hysteresis under different voltage-step sizes (see Section 3). Neuromorphic characterization used fixed-count pulse trains with variable pulse width to probe the device’s behavior.

3. Results and Discussion

Fine-tuning the gate voltage of the PMOS strongly affects the charge trapping in the defects of the oxide layer and is crucial to achieving neuromorphic behaviour. A bidirectional sweep signal of voltage (absolute) varying from 0 to 1.8 V is applied to the gate terminal of the PMOS device for different step sizes, such as 0.1 mV, 0.5 mV, 1 mV, and 10 mV. Figure 1 illustrates the variation in the absolute drain current (I_D) vs. gate-to-source (V_{GS}) voltage characteristics of the PMOS with a transistor with a width-to-length (W/L) ratio of $0.22 \mu\text{m}/0.18 \mu\text{m}$ under different voltage step sizes. The devices exhibit pinched hysteresis characteristics at a gate voltage of 0.6 V at a step size of 0.5 mV, showing the fingerprint of the memory retention characteristics. This type of hysteresis behavior may be due to the charge trapping and detrapping of charge carriers (holes) owing to defects in the oxide interface at cryogenic temperatures (3 K), showing a slight shift in the threshold voltages [8]. Further, for a smaller step size of 0.1 mV, the trap occupancy is slower due to gradual filling of the traps with long time constants of the carriers, resulting in a wider pinched hysteresis [9]. Conversely, for a higher step size of 10 mV, the device exhibits linear characteristics, showing a nullified analog hysteresis behavior due to faster saturation of the traps.

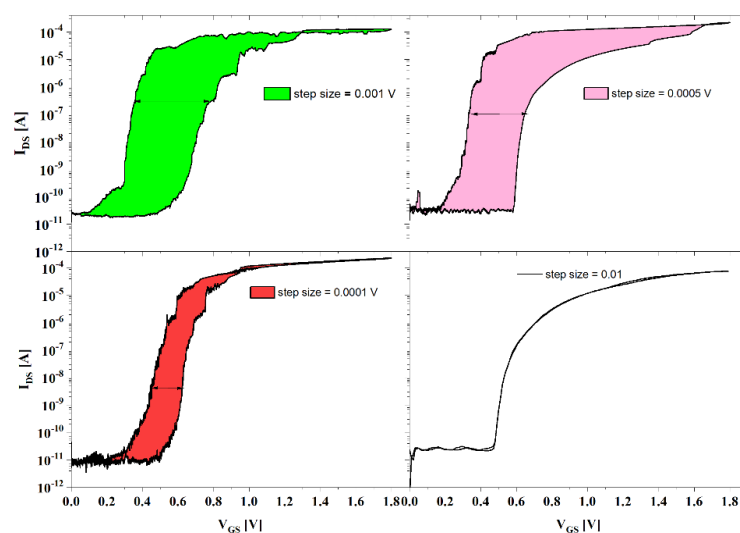


Figure 1. Pinched hysteresis I_D – V_{GS} characteristics for PMOS devices with the width-to-length ratios as $0.22 \mu\text{m}/0.18 \mu\text{m}$ under various step sizes varying from 1 mV, 0.5 mV, 0.1 mV, and 10 mV, respectively, at cryogenic temperatures (3 K).

To further understand the electrical behavior of the fabricated PMOS devices under different input and output excitation, current vs. voltage measurements were performed.

Figure 2 shows the input and output DC response characteristics of the PMOS device under different drain-to-source voltages (V_{DS}) of 0.05 V and 1.8 V at room temperature. The transfer characteristics of the transistor exhibit an exponential increase in the drain current with a linear increase in the gate-to-source voltage for both low and high V_{DS} voltages. At higher drain voltage (red curve), there is a significant increase in the drain current attributed to the stronger inversion channel formation and enhanced charge carrier (holes) transport.

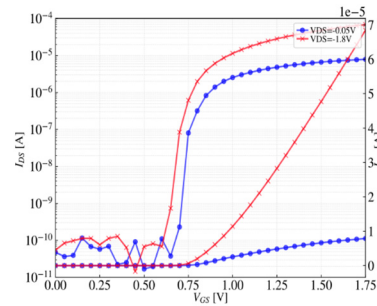


Figure 2. Input and output response DC characteristics of the fabricated PMOS transistor.

The pinched hysteresis of the as-fabricated device shows a very good data storage capacity and can further be useful as a capacitorless storage memory [9,10]. Figure 3a,b shows the variation in the threshold voltage, followed by the variation in the drain current with respect to time for different pulses applied at the gate. Figure 3c,d shows efficiency and variation in the post-synaptic current (PSC) with different pulses. The PMOS device shows greater efficiency and an increase in the synaptic current with the pulses, and is crucial for neuromorphic behaviour.

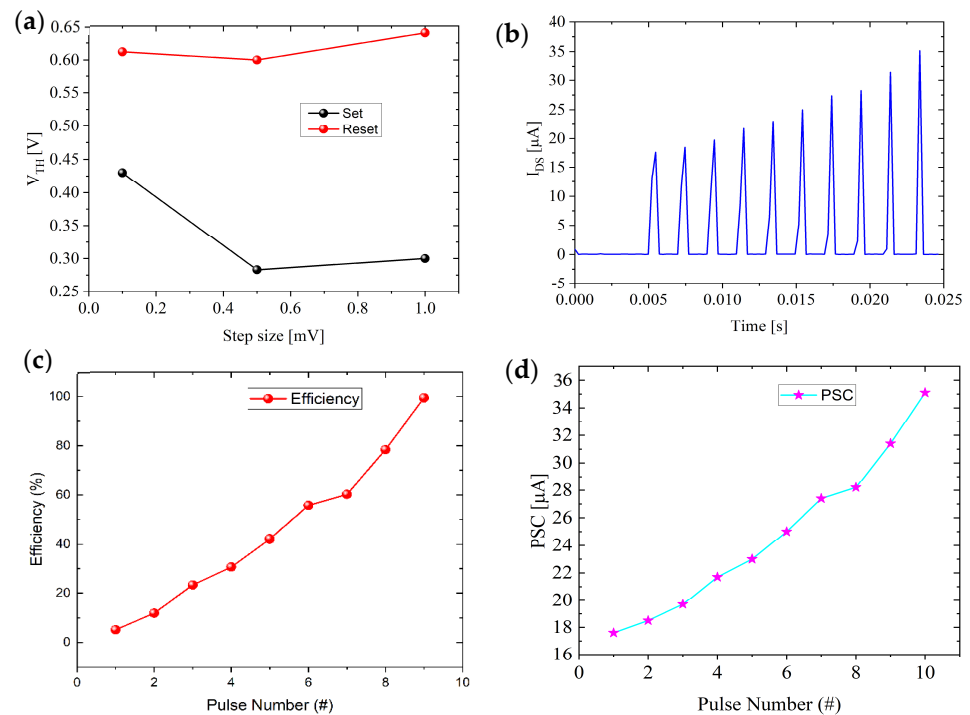


Figure 3. (a) Variation in the set and reset voltage with respect to step size (b) response post-synaptic current by the appliance of the pre-synaptic excitations at the gate terminal of the device (c) Synaptic plasticity efficiency of the PMOS device under different pulses and (d) post-synaptic current response showing the learning phenomenon of the device under the appliance's various numbers of pulses.

4. Conclusions

In conclusion, we proposed a novel approach of exploring standard FET technology for cryogenic-based synaptic memory applications to meet the growing demands of the next generation of high-performance computing for various applications, including signal processing, biomedical, and memory. This type of novel synaptic characteristic proposes a significant step toward the transformation of next-generation artificial intelligence, offering superior computational speeds and better energy efficiency.

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